

A Novel architecture of 64 bit MAC unit using Dadda multiplier

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ABSTRACT:

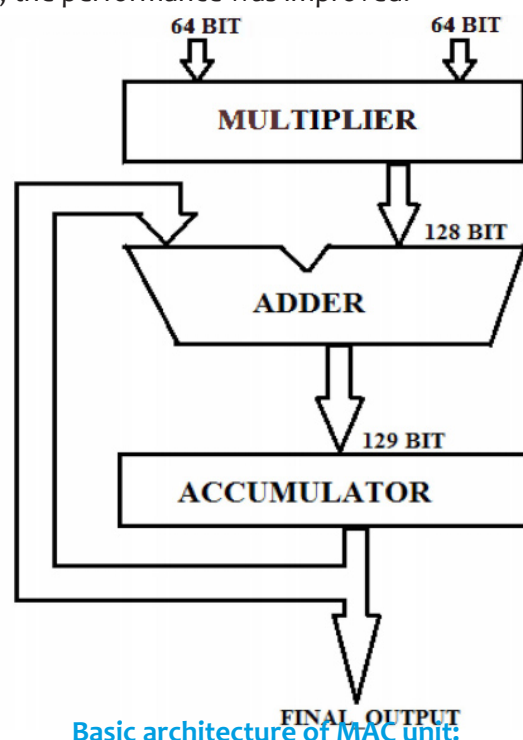
MAC unit is an inevitable many digital signal processing (DSP) applications involving multiplications and/or accumulations. MAC unit is used for high performance digital signal processing systems. The DSP applications include filtering, convolution, and inner products. Most of digital signal processing methods use nonlinear functions such as discrete cosine transform (DCT) or discrete wavelet transforms (DWT). Because they are basically accomplished by repetitive application of multiplication and addition, the speed of the multiplication and addition arithmetic determines the execution speed and performance of the entire calculation[1].

The Multiplication-and-accumulate(MAC) operations are typical for digital filters. Therefore, the functionality of the MAC unit enables high-speed filtering and other processing typical for DSP applications. Since the MAC unit operates completely independent of the CPU, it can process data separately and thereby reduce CPU load. The application like optical communication systems which is based on DSP, require extremely fast-processing of huge amount of digital data. The Fast-Fourier Transform (FFT) also requires addition and multiplication. 64 bit can handle larger bits and have more memory.

1.INTRODUCTION:

With the recent rapid advances in multimedia and communication systems, real-time signal processing like audio signal processing, video/image processing, or large-capacity data processing are increasingly being demanded. The multiplier and multiplier-and-accumulator (MAC) are the essential elements of the digital signal processing such as filtering, convolution, transformations and Inner products. There are different entities that one would like to optimize when designing a VLSI circuit.

These entities can often not be optimized simultaneously, only improve one entity at the expense of one or more others. The design of an efficient integrated circuit in terms of power, area, and speed simultaneously, has become a very challenging problem. Power dissipation is recognized as a critical parameter in modern the objective of a good multiplier is to provide a physically compact, good speed and low power consuming chip. This paper proposes a new architecture of multiplier-and-accumulator (MAC) for high speed and low-power by adopting the new SPST implementing approach. This multiplier is designed by equipping the Spurious Power Suppression Technique (SPST) on a modified Booth encoder which is controlled by a detection unit using an AND gate. The modified booth encoder will reduce the number of partial products generated by a factor of 2. The SPST adder will avoid the unwanted addition and thus minimize the switching power dissipation. By combining multiplication with accumulation and devising a low power equipped carry save adder (CSA), the performance was improved.

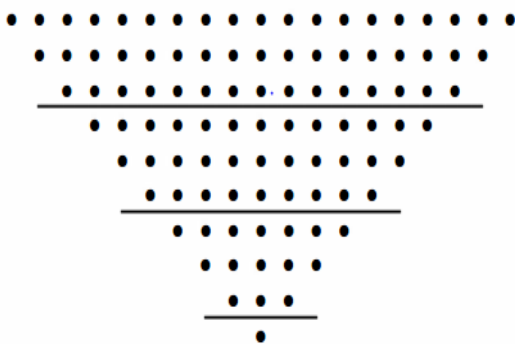


Basic architecture of MAC unit:

I.CONVENTIONAL MODIFIED :

Wallace tree multiplier consists of three steps. In the first step, the bit product terms are formed after the multiplication of the bits of multiplicand and multiplier. In the second step, the bit product matrix is reduced to a lower number of rows using half and full adders. This process continues until the last addition remains. In the final step, the final addition is done using adders to obtain the result. The benefit of the Wallace tree is that there are only $O(\log n)$ reduction layers, and each layer has $O(1)$ propagation delay. As making the partial products is $O(1)$ and the final addition is $O(\log n)$, the multiplication is only $O(\log n)$, not much slower than addition (however, much more expensive in the gate count). Naively adding partial products with regular adders would require $O(\log^2 n)$ time. In perspective, the Wallace tree algorithm puts multiplication in class. These computations only consider gate delays and don't deal with wire delays, which can also be very substantial.

Architecture of the Wallace Tree Multiplier:



MODIFIED 4*4 WALLACE TREE MULTIPLIER:

The basic multiplication principle is two fold i.e. evaluation of partial products and accumulation of the shifted partial products. It is performed by the successive additions of the columns of the shifted partial product matrix. The 'multiplier' is successively shifted and gates the appropriate bit of the 'multiplicand'.

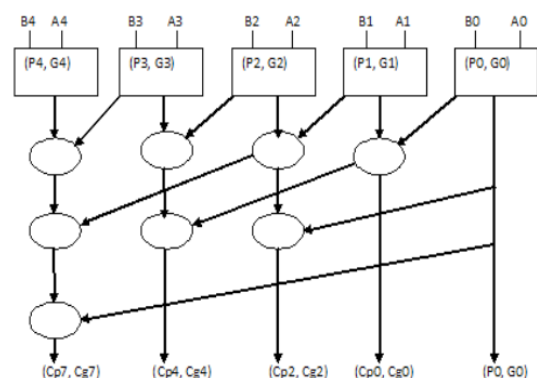
The delayed, gated instance of the multiplicand must all be in the same column of the shifted partial product matrix. They are then added to form the product bit for the particular form. Multiplication is therefore a multi operand operation. To extend the multiplication to both signed and unsigned.

4.parallel prefix adder:

The binary adder is the critical element in most digital circuit designs including digital signal processors (DSP) and microprocessor data path units. As such, extensive research continues to be focused on improving the power delay performance of the adder. In VLSI implementations, parallel-prefix adders are known to have the best performance.

Parallel-prefix adders (also known as carry-tree adders) are known to have the best performance in VLSI designs. However, this performance advantage does not translate directly into FPGA implementations due to constraints on logic block configurations and routing overhead. This paper investigates three types of carry-tree adders (the Kogge-Stone, sparse Kogge-Stone, and spanning tree adder).

Fig. parallel prefix adder:

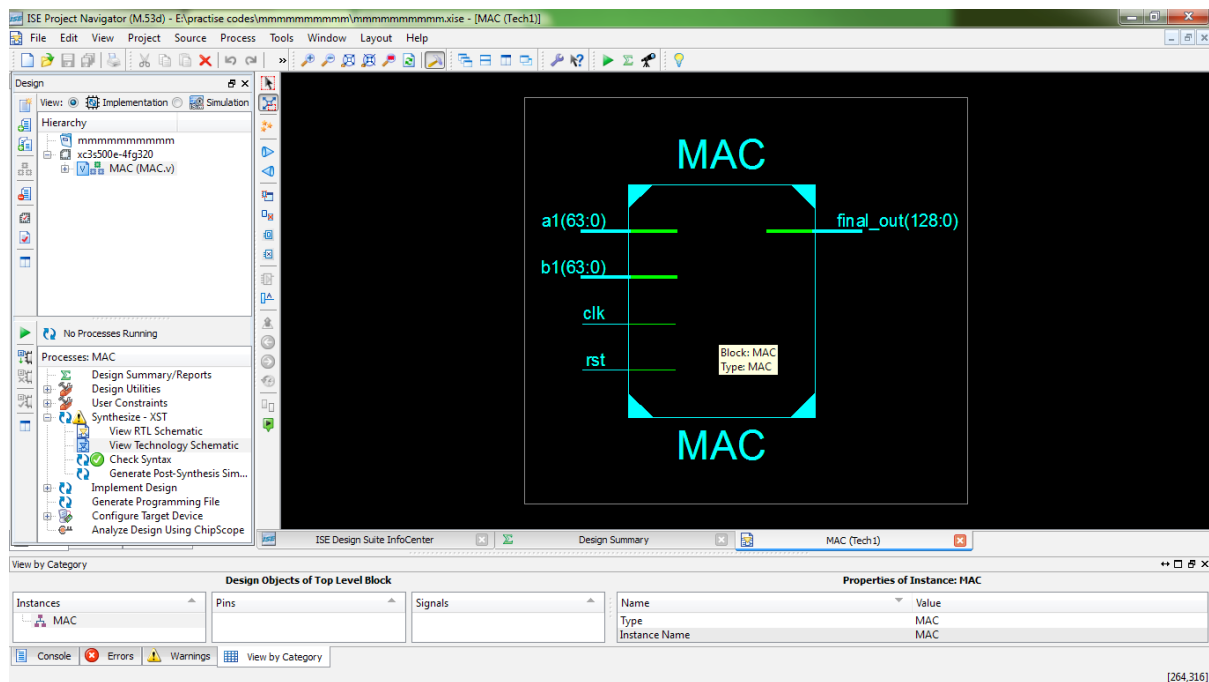


Proposed multiplier:

The present Modified Booth Encoding (MBE) multiplier and the Baugh-Wooley multiplier perform multiplication operation on signed numbers only. The array multiplier and Braun array multipliers perform multiplication operation on unsigned numbers only. Thus, the requirement of the modern computer system is a dedicated and very high speed unique multiplier unit for signed and unsigned numbers.

Therefore, this paper presents the design and implementation of SUMBE multiplier. The modified Booth Encoder circuit generates half the partial products in parallel. By extending sign bit of the operands and generating an additional partial product the SUMBE multiplier is obtained.

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(c) Fig: Simulation results

V. CONCLUSION:

In this paper, we present a 64 bit mac that was implemented using booths multiplier.the adder circuit that was used is a parallel prefix adder.in the multiplier design to add the partial products we use carry select adder and carry look ahead adder.the delay of the proposed system is very less when compared to the previous design.

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