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# Design and Analysis of Diode Free Adiabatic Logic Circuits for Dynamic Loss Reduction

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## Abstract:

Frequency dividers are crucial circuits that are employed in PLLs and high-speed serialize/deserializers. The flip-flop-based frequency dividers are comprised of two D latches in cascade, and in a negative feedback configuration. The digital operation of this type of dividers provides the advantage of suppressing the sensitivity to waveform distortions. Furthermore, the flip-flop-based dividers achieve a wide bandwidth than other types of frequency dividers at low-to-medium range of frequencies. This paper presents a high-speed DFAL flip-flop-based frequency divider incorporating a new high-speed latch topology, which provides satisfactory performance for frequencies up to 17 GHz. This circuit is designed and simulated in a standard 0.18µm CMOS process.

**Keywords:** Frequency Divider, D Latches, DFAL

## I.INTRODUCTION:

In the past few decades ago, the electronics industry has been experiencing an unprecedented spurt in growth, thanks to the use of integrated circuits in computing, telecommunications and consumer electronics. We have come a long way from the single transistor era in 1958 to the present day ULSI (Ultra Large Scale Integration) systems with more than 50 million transistors in a single chip. The ever-growing number of transistors integrated on a chip and the increasing transistor switching speed in recent decades has enabled great performance improvement in computer systems by several orders of magnitude. Unfortunately, such phenomenal performance improvements have been accompanied by an increase in power and energy dissipation of the systems. Higher power and energy dissipation in high performance systems require more expensive packaging and cooling technologies, increase cost, and decrease system reliability. Nonetheless, the level of on-chip integration and clock frequency will continue to grow with increasing performance demands, and the power and energy dissipation of high-performance systems will be a critical design constraint. For example, high-end microprocessors in 2010 are predicted to employ billions of transistors at clock rates over 30GHz to achieve TIPS (Tera Instructions per seconds) performance [1]. With this rate, high-end microprocessor's power dissipation is projected to reach thousands of Watts. This thesis investigates one of the major sources of the power/energy dissipation and proposes and evaluates the techniques to reduce the dissipation.Digital CMOS integrated circuits have been the driving force behind VLSI for high performance computing and other applications, related to science and technology. The demand for digital CMOS integrated circuits will continue to increase in the near future, due to its important salient features like low power, reliable performance and improvements in the processing technology.

## II.NEED FOR LOW POWER DESIGN:

There are various interpretations of the Moore's Law that predicts the growth rate of integrated circuits. One estimate places the rate at 2X for every eighteen months. Others claim that the device density increases ten-fold every seven years. Regardless of the exact numbers, everyone agrees that the growth rate is rapid with no signs of slowing down. New generations of processing technology are being developed while present generation devices are at very safe distance from the fundamental physical limits. A need for low power VLSI chips arises from such evolution forces of integrated circuits. The Intel 4004 microprocessor, developed in 1971, had 2300 transistors, dissipated about 1 watts of power and clocked at 1 MHz. Then comes the Pentium in 2001, with 42 million transistors, dissipating around 65 watts of power and clocked at 2. Another factor that fuels the need for low power chips is the increased market demand for portable consumer electronics powered by batteries. The craving for smaller, lighter and more durable electronic products indirectly translates to low power requirements.

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Battery life is becoming a product differentiator in many portable systems. Being the heaviest and biggest component in many portable systems, batteries have not experienced the similar rapid density growth compared to the electronic circuits. The main source of power dissipation in these high performance battery-portable digital systems running on batteries such as note-book computers, cellular phones and personal digital assistants are gaining prominence. For these systems, low power consumption is a prime concern, because it directly affects the performance by having effects on battery longevity. In this situation, low power VLSI design has assumed great importance as an active and rapidly developing field.Another major demand for low power chips and systems comes from the environmental concerns. Modern offices are now furnished with office automation equipments that consume large amount of power.

## III.OVERVIEW OF POWER DISSIPATION:

It is more convenient to talk about power dissipation of digital circuits at this point. Although power depends greatly on the circuit style, it can be divided, in general, into static and dynamic power. The static power is generated due to the DC bias current, as is the case in transistor-transistor-logic (TTL), emitter-coupled logic (ECL), and N-type MOS (NMOS) logic families, or due to leakage currents. In all of the logic families except for the push-pull types such as CMOS, the static power tends to dominate. That is the reason why CMOS is the most suitable circuit style for very large scale integration (VLSI). CMOS is the logic family preferred in many designs due to following reasons:

(a)Impeccable noise margins.
(b)Perfect logic levels.
(c)Negligible static power dissipation.
(d)Gives good performance in most cases.
(e)Easy to get a functional circuits.
(f)Lot of tools available to automate the design process.

### 3.1STATIC POWER:

The static or steady state power dissipation of a circuit is expressed by the following relation [1]
Pstat = IstatVDD
where, Istat is the current that flows through the circuit when there is no switching activity.

Ideally, CMOS circuits dissipate no static (DC) power since in the steady state there is no direct path from VDD to ground as PMOS and NMOS transistors are never on simultaneously. Of course, this scenario can never be realized in practice since in reality the MOS transistor is not a perfect switch. Thus, there will always be leakage currents and substrate injection currents, which will give to a static component of CMOS power dissipation.

### 3.2DYNAMIC POWER:

The dynamic component of power dissipation arises from the transient switching behavior of the CMOS device. At some point during the switching transient, both the NMOS and PMOS devices will be turned on. This occurs for gate voltages between Vtn and VDD- Vtp . During this time, a short-circuit exists between VDD and ground and the currents are allowed to flow. A detailed analysis of this phenomenon by Veendrick reveals that with careful design of the transition edges, this component can be kept below 10-15% of the total power [2]; this can be achieved by keeping the rise and fall times of all the signals throughout the design within a fixed range (preferably equal). Thus, although short circuit dissipation cannot always be completely ignored, it is certainly not the dominant component of power dissipation in well-designed CMOS circuits. Instead, dynamic dissipation due to capacitance charging consumes most of the power.

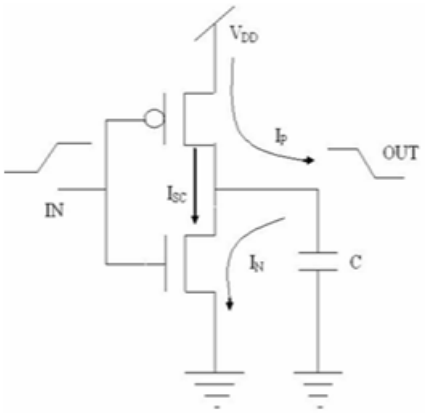


**Fig1. CMOS Inverter for Power Analysis**

A novel class of logic circuits called ADIABATIC LOGIC offers the possibility of further reducing the energy dissipated during the switching events and the possibility of recycling or reusing some of the energy drawn from the power supply [3]. To accomplish this goal, the circuit topology and the operating principle have to be modified, sometimes drastically.

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The amount of energy recycling achievable using adiabatic techniques is also determined by the fabrication technology, switching speed and the voltage swing.

## IV. DIODE FREE ADIABATIC LOGIC:

It shows the circuit diagram and simulated waveforms verifying the operation of an inverter based on DFAL circuit. The attractive feature of proposed topology is that it is diode free; there is not any diode in its charging or discharging path. In our proposal,split level sinusoidal power clock supply PC and PC areused. One clock is in phase while the other is inverted.The voltage level of PC exceeds that of PC by a factor ofPC/2, this will minimize the voltage difference between theelectrodes and consequently power dissipation is reduced.Split level clock charges/discharges the load capacitancecomparatively slowly than the other adiabatic power clocks.Since the efficiency of adiabatic logic circuits depends uponhow slowly the load capacitance is charged or discharged sopower dissipation is minimized further.

The schematic of DFAL resembles the static CMOS logic; however circuit operates in adiabatic manner. The nMOS transistor (M3) in the pull down network adjacent to the M2 is used to replace the diode for the discharging. Power clock (PC) controls the turning ON and OFF of this transistor (M3). The main power dissipation in reported adiabatic circuits in their discharging path occurs at the (MOS) diodes.Due to the threshold voltage drop (non-adiabatic loss) whereas in our proposed circuit it is due to the ON resistance (adiabatic loss) of channel of MOS transistor M3.

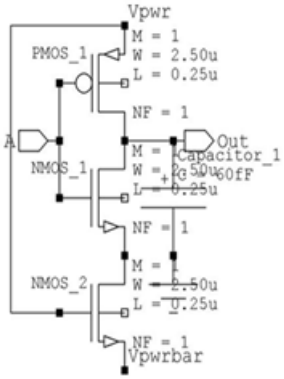


Fig2: DFAL Inverter Design

## Circuit Operation:

Depending on the supply clock signal phases, circuit operation is divided into two stages, evaluation and hold. In evaluation phase PC swings up while PC swings down; however in hold phase PC swings down and PC swings up as shown in Figure 1(b). In evaluation phase, when the output node is LOW and pMOS tree is turned ON, load capacitance is charged through pMOS transistor (M1) resulting in the HIGH state at the output. Further when output node is HIGH and nMOS tree turns ON, discharging and recycling of charges to the power clock (PC) via nMOS transistor (M2 and M3) occurs, resulting in the output logic state to be LOW In hold phase, when output node is LOW and nMOS tree is ON, no transitions occur at the output. The same process happens when the output node is HIGH and pMOS tree is ONThis DFAL based was applied to a Frequency divider circuit inorder to reduce the dynamic power in the Circuit.A frequency divider, also referred to as a clock divider, produces an output signal whose frequency is a fraction of the input frequency.

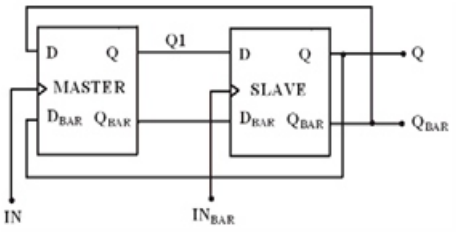


Fig3: Divide by 2 frequency divider using D Flip-Flop

## V. COUNTER USING FREQUENCY DIVIDED BY 2 AND 4 AND 8 USING DFAL FREQUENCY DIVIDER:

The counter consists of 3 stages of cascaded D Flip-flops. The D Flip-flop design has been implemented using DFAL and two D latch with one clock and one input. The clock input is applied to subsequent flip flop comes from the output of its immediately preceding flip flop. For first or instance the output of the first register acts as the clock input to the second register and the output of the second register feed the clock input of third register. The second register can change state only after the output of first register can change its state. That is the second fact that it gets its own clock input from output of the first and not from the input clock.

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This time delay here the sum of propagation delay of two flip flops. So in this counter four register will change state only after a delay equal to four times the propagation delay of one flip-flop.

## Simulation:

The DFAL based divided by 2 frequency divider was designed using S-EDIT and these simulations are carried out in T-Spice using TSMC018 Technology.

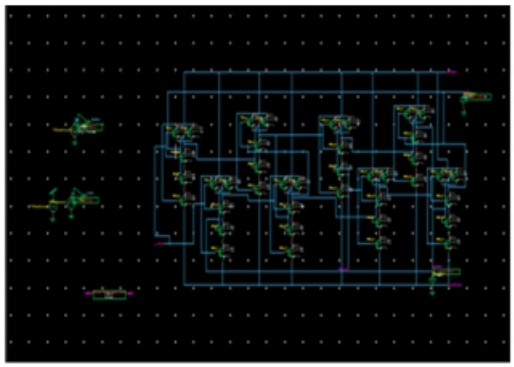

Fig4: Schematic design of Frequency Divider Circuit

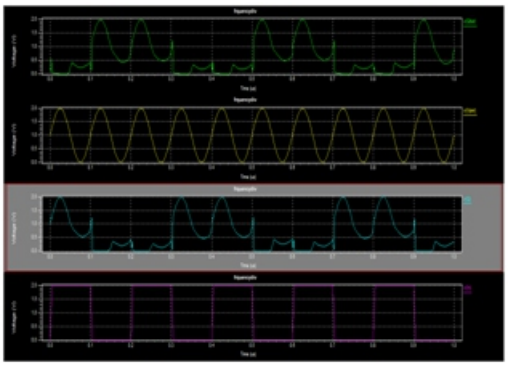

Fig5: Simulation of Frequency Divider Circuit

In this counter four register will change state only after a delay equal to four times the propagation delay of one flip-flop.

| Circuit | 20pf | 40pf | 60pf |
|---|---|---|---|
| Conventional Frequency Divider | 1.447677e - 005 (watts) | 1.485725e - 005 (watts) | 1.523528e - 005 (watts) |
| 2PASCL | 2.701592e - 006 (watts) | 2.826447e - 005 (watts) | 2.984332e - 006 (watts) |
| DFAL | 1.999676e - 006 (watts) | 2.164064e – 006 (watts) | 2.270024e - 006 (watts) |

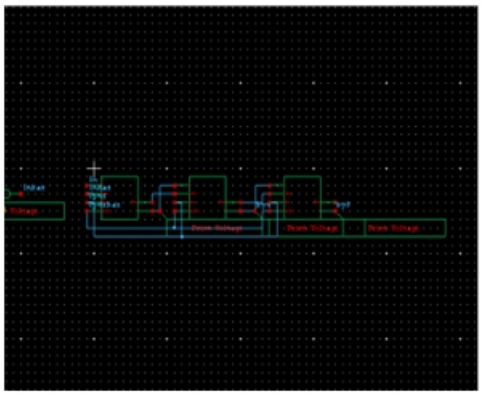

Fig6: Schematic design of frequency divided by 2 and 4 and 8

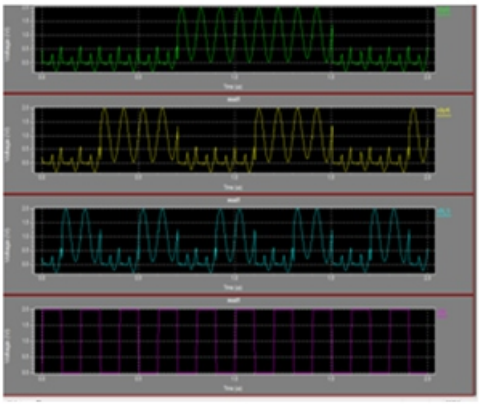

Fig7: Simulation of frequency divided by 2 and 4 a nd 8

## Tabulation:

The below tabulation consists of Power Consumption of the frequency divider with different loads.

## CONCLUSION:

DFAL technique was the efficient technique in order to reduce the dynamic losses in the flip-flop. This method was extended to apply on the frequency divider circuit. The mechanism effectively causes the output to toggle between one and zero at a rate half that of the input clock. Thus frequency division is achieved. The designed circuit and the verification can be done in TANNER EDA.

## FUTURE WORK:

Future work on this project is designing of Jitter Programmable Clock Multiplier Based on a Pulse Injection-Locked Oscillator with a Highly-Digital Tuning Loop.

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