

## **A Novel Switched Capacitor Based Cascaded H Bridge Inverter Using Symmetrical Modulation**

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### **ABSTRACT:**

This paper review analysis of the performance of a DC energy source based Multi Level Inverter topology. Multi Level Inverter topologies are suitable in high power application due to their ability to synthesize waveforms with better harmonic spectrum. The Multilevel inverter circuit analysis and selection of proper references discussed based on the formulation switching patterns. A Eleven level cascaded inverter is used to explain the methods. The method can be easily extended to an m-level inverter. The cascaded inverter is subjected to a new modulation scheme, which uses multiple modulating signals with a single carrier. In order to justify the merits of the proposed modulation scheme, harmonic analysis for and measured THD and output voltages are compared and discussed.

### **Index Terms:**

Cascaded H-bridge multilevel inverter (CHB), multicarrier pulse-width modulation, phase shifted modulation, total harmonic distortion (THD).

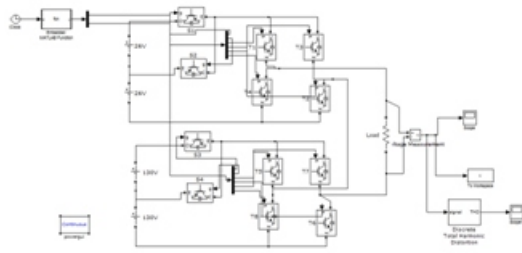
### **I. INTRODUCTION:**

Multilevel power conversion has become increasingly popular in recent years due to advantages of high power quality waveforms, low electromagnetic compatibility (EMC) concerns, low switching losses, and high-voltage capability. However, it increases the number of switching devices and other components, which results in an increase of complexity problems and system cost. There are different types of multilevel circuits involved. The first topology introduced was the series H-bridge design. This was followed by the diode clamped converter, which utilized a bank of series capacitors.

A later invention detailed the flying capacitor design in which the capacitors were floating rather than series-connected. Another multilevel design involves parallel connection of inverter phases through inter-phase reactors. In this design, the semiconductors block the entire dc voltage, but share the load current. Several combinational designs have also emerged some involving cascading the fundamental topologies. These designs can create higher power quality for a given number of semiconductor devices than the fundamental topologies alone due to a multiplying effect of the number of levels. The multilevel inverters are mainly classified as diode clamped, Flying capacitor inverter and cascaded multilevel inverter. The cascaded multilevel control method is very easy when compare to other multilevel inverter because it doesn't require any clamping diode and flying capacitor. In this paper, we are using a new topology of cascaded H-bridge multilevel inverter for producing Eleven output voltage levels and for that we are using multicarrier modulation technique.

### **II. PROPOSED SYSTEM: ELEVEN-LEVEL CASCADED H-BRIDGE MULTILEVEL INVERTER:**

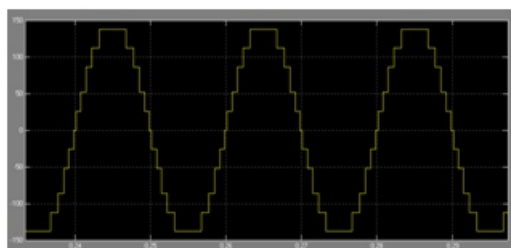
The main disadvantage of the conventional cascaded H-bridge is that when the voltage level increases, the number of semiconductor switches increases and also the source required increases. In order to overcome this introduced a new topology of cascaded H-bridge. The main advantage of this topology is that the number of switches required is reduced and also the number of sources. Figure 1 shows the new cascaded Eleven level H-bridge multilevel inverter. It has additional one bidirectional switch connected between the first leg of the H-bridge and the capacitor midpoint, enabling five output voltage levels.



**Fig. 1. Circuit topology of cascaded Eleven-level inverter.**

### A.Circuit Topology:

Fig. 1 shows the circuit topology of Eleven -level inverter ( $N_1 = 2, N_2 = 2$ ), where  $S_1, S_2, S_{1_1}, S_{2_2}$  as the switching devices of SC circuits (SC1 and SC2) are used to convert the series or parallel connection of  $C_1$  and  $C_2$ .  $S_{1a}, S_{1b}, S_{1c}, S_{1d}, S_{2a}, S_{2b}, S_{2c}, S_{2d}$  are the switching devices of cascaded H-Bridge.  $V_{dc1}$  and  $V_{dc2}$  are input voltage.  $i_{out}$  and  $v_o$  are the output current and the output voltage, respectively. It is worth noting that the backend circuit of the proposed inverter is cascaded H-Bridges in series connection. It is significant for H-Bridge to ensure the circuit conducting regardless of the directions of output voltage and current. In other words, H-Bridge has four conducting modes in the conditions of inductive and resistive load, i.e., forward conducting, reverse conducting, forward freewheeling, and reverse freewheeling.



**Fig.2. 11-level wave form**

### III.CONTROL STRATEGY CAPACITOR VOLTAGE REGULATION:

In the proposed topology of H-bridge Cascaded multilevel inverter, the dc sources are replaced by capacitors. These replaced capacitors must be regulated to a certain voltage in order to have the required voltage level in the output voltage of the converter. However, the power system operation and modulation scheme together have different effects on each capacitor so that they are not charged and discharged evenly leading to different voltages in each leg of each phase.

To achieve a high quality output voltage waveform, the voltages across all DC capacitors should maintain a constant value. One challenging problem of the cascade multilevel inverter with a single DC source is the imbalance of the DC capacitor voltages. The imbalance is caused by:

- 1) Different switching patterns for different H-bridges.
- 2) Parameter variations of active and passive components inside H-bridges.
- 3) Control resolution.

To achieve higher voltage quality, the switching patterns are usually different for different H-bridges in a phase. The differences of switching patterns mean that H-bridges cannot equally share the exchanged power with the power system. This causes uneven charging of DC capacitors. The parameter variations of components inherently cause different power losses of H-bridges. The imbalance of DC capacitor voltages will degrade the quality of the voltage output. In severe cases, this could lead to the complete collapse of the power conversion system. Moreover, it will cause excessive voltages across the devices and an imbalance of switching losses. An adequate control strategy for avoiding the imbalance of DC capacitor voltages must meet the following requirements.

- 1) The impact on voltage quality should be as small as possible.
- 2) It can balance voltages when components of H-bridges have parameter variations.
- 3) It can balance voltages when H-bridges switch with different switching patterns.

In the previous topologies, to balance the capacitor voltages, redundant state selection (RSS) is an effective tool in balancing the DC capacitor voltages. In this method the capacitor balancing is going to be achieved by using the proper capacitor in each level in order to get the desired level dictated by SPWM. In each level if the current direction of the phase is tending to charge the capacitors the least charged ones should be used to maintain the desired level and if the current direction tends to discharge the capacitors the most charged capacitors come into play. However, the output current of the inverter and the time duration of the redundant switching states greatly impact the charging or discharging patterns of the replacement capacitors.

### CAPACITOR VOLTAGE REGULATION:

This paper proposes a control method applicable to single dc- source cascaded H bridge multilevel inverters to improve their capacitor voltage regulation. The proposed method, phase shift modulation, is robust and does not incur much computational burden. In this method, using embedded function block the coding done as per the main inverter switches at the fundamental frequency, and the auxiliary inverter switches at the PWM frequency. The switching pattern as follows:

```

3 - a=mod(u,0.02);
4 - b=abs(sin(2*pi*50*a));
5 - d=sin(2*pi*50*a);
6 - if d>0
7 -     c=1;
8 - else
9 -     c=0;
10 - end
11 - if b<0.5/10    % Level 0
12 -     s1=0;
13 -     s2=0;
14 -     t1=1;
15 -     t2=0;
16 -     t3=1;
17 -     t4=0;
18 -     s3=0;
19 -     s4=0;
20 -     p1=1;
21 -     p2=0;
22 -     p3=1;
23 -     p4=0;
24 - elseif b<2.5/10    % Level 1
25 -     s1=0;
26 -     s2=0;
27 -     t1=1;
28 -     t2=1;
29 -     t3=0;
30 -     t4=0;
31 -     s3=0;
32 -     s4=0;
33 -     p1=1;
34 -     p2=0;
35 -     p3=1;
36 -     p4=0;

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Fig.3. Switching Pattern

Regulating the capacitor voltage in the auxiliary H-bridge cell is a challenging task. In the method proposed here, capacitor voltage regulation is achieved by adjusting the active power that the main H bridge cell injects into the system. By shifting the voltage waveform generated by the main H-bridge cell to the left or right, one can inject more (or less) active power, which can be used to charge (or discharge) the capacitor on the auxiliary cell.

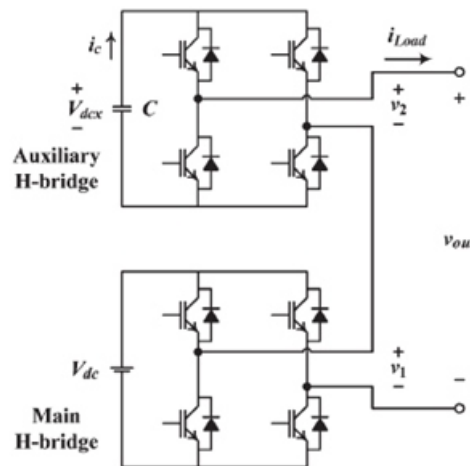


Fig.4. Block diagram of a cascaded H-bridge inverter.

The main H-bridge cell, which is supplied by  $V_{dc}$ , generates a rectangular waveform ( $v_1$ ), the frequency of which equals that of the desired output voltage. Furthermore, the width of this rectangular waveform is chosen in such a way that the amplitude of its fundamental harmonic also equals that of the desired output voltage. In other words,

$$\alpha = \cos^{-1}(\pi V_m / 4V_{dc})$$

Where  $\alpha$  is the conduction angle of the main H-bridge cell. From the phase shift modulation of cascaded multilevel inverter, the real power flow capacitor voltages are balanced by adjusting the phase of the waveform.

### IV.SIMULATION RESULTS:

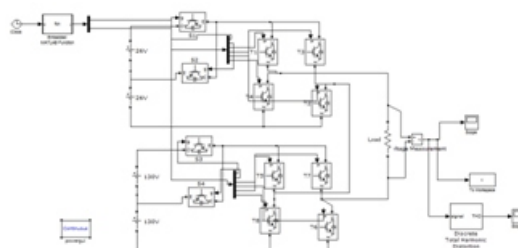


Fig.5. Circuit topology of cascaded Eleven-level inverter.

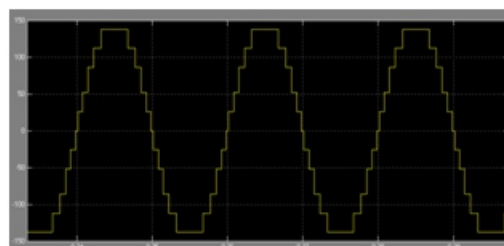


Fig.6. 11-level wave form

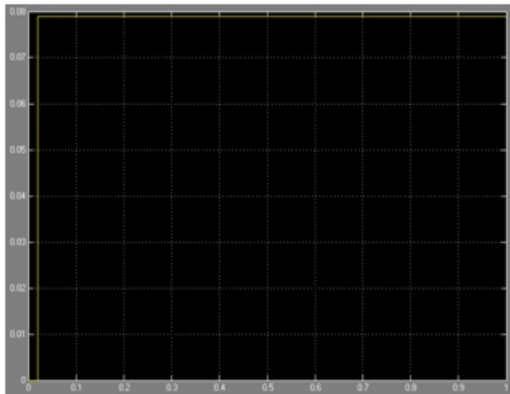


Fig.7. Output Voltage THD wave form

## V. CONCLUSION:

“Multi Level Converter”. After a brief overview of the background information, design considerations presented multilevel voltage source converters that synthesize the converter voltage by equally divided capacitor voltages. All these converter have been completely analyzed and simulated. Multilevel converters The application on which the multilevel voltage source converter may have the most impact is the adjustable speed drive. Using multilevel converters not only solves harmonics and EMI problems, but also avoids possible high frequency switching dv/dt induced motor failures. With a balanced voltage stress in devices and utility compatible features, the multilevel converters have shed a light in the power electronics arena and are emerging as a new breed of power converters for high-voltage high-power applications.

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