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Three-Phase Four-Wire VSI Parallel Connected Using Fuzzy Logic Controller

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Abstract:
This work approaches Fuzzy Logic based control strategy with communication for three-phase vfour-wire VSI parallel connected, which is based on distributed control. The work presents details of implementation of one control strategy that employs two loops, one voltage control and one parallelism control, all system is done on instantaneous values and the parallelism control shares only a voltage reference signal among the VISs. The strategy ensures power load shared among the inverters in steady-state and a fast dynamic response during connection or disconnection of VSI and load step.

*IndexTerms—**VSI, fuzzy controller, PWM***

I INTRODUCTION

Three-phase four-wire voltage source inverter (VSI) shown in Fig. 1 is usually applied in UPS, due to supply single and three-phase loads in balance or in unbalanced conditions, what is required in a typical UPS. When reliability and redundancy is necessary in a UPS, the parallel operation of units is an option; however a control strategy is required to ensure its operation. Therefore, strategies that ensure the parallel operation of three-phase four-wire VSI applied in UPS are still a need, mainly in the industry. A traditional solution for parallel operation of VIS is the control strategy based on the frequency and voltage droop.

This strategy controls the average active and reactive power flow from the VSI to the load and it does not require communication among the inverters. It provides increased reliability and redundancy but it has errors associated with load sharing, poor transient response, reduced voltage regulation and it does not control the division of the harmonic currents. The industry does not these drawbacks and thus prefers the strategies with communication, which can be subdivided in central control master-slave control and distributed control. Strategies with communication are most effective in terms of load sharing, but high reliability and redundancy are not available due to the communication between units. The distributed control strategy has been applied in recent publications in the literature and demonstrated better dynamic response in the parallel connection among power converters. Hence, any converter can be removed or inserted in the system and the others will still in operation supplying the load. Thus, n + 1 or even n + 2 power converters can supply n_P total power in the load. Moreover, the communication link between power modules can be implemented with redundancy ways as demonstrated in.

Therefore, high reliability and redundancy can be achieved with distributed control strategy. Hence, this control strategy becomes very interesting in UPS applications, due to (i) the power converters are closely located; (ii) UPS applications require high reliability and redundancy and (iii) the power converters removal or insertion can be done in transparent way in load point of view, and hence the supplied power system capability can be increased. This paper approaches the implementation of a distributed control strategy for three-phase four-wire VSI parallel connected for UPS applications. Therefore, control strategy, implementation of the

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digital controllers, implementation of the communication among the inverters, implementation of the prototypes, simulation tests and set of experimental tests to verify the strategy are presented in the text.

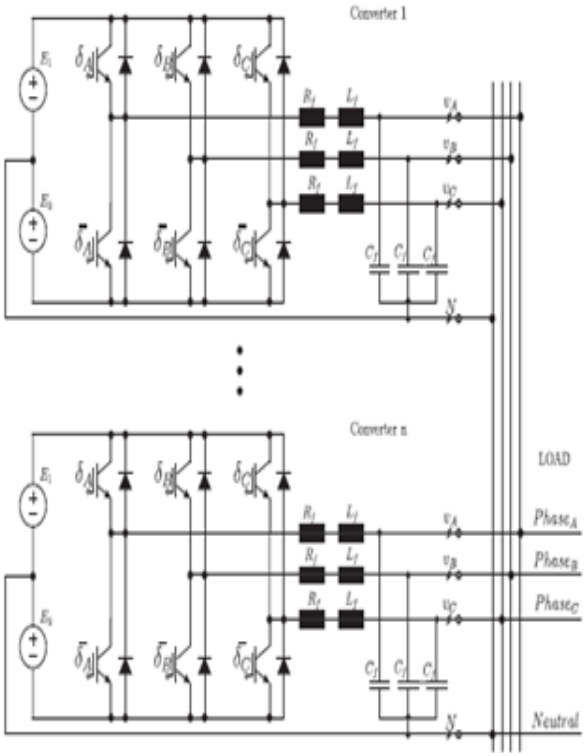

Fig. 1. *n* four-wire VSI topologies parallel connected.

II CONTROL STRATEGY TO VSI PARALLEL CONNECTED

The control strategy employ a common reference between power converters which one guarantees the synchronism between them as demonstrated in Fig.2. The necessity of this communication link could represent low reliability and redundancy to the system.

However, as demonstrated in redundant channels and strategies can be implemented to guarantee this link between power converters. Hence, when a failure to happens, other communication link begins to operate. In this context, Controller Area Network – CAN interface, power grid synchronism, Phase–Locked–Loop – PLL synchronism algorithms are examples that could be implemented to improve reliability and redundancy of this communication system and also of power supply system.

The Fig. 2 demonstrates the main signals employed in the proposed control strategy considering n VSI parallel connected. The control structures are composed by two loops. Hence, there are: (i) The voltage control loop, which reference is resultant of communication link between power converters, and it regulates the voltage applied to the load; (ii) current control loop, which one is responsable to balances the currents sharing between n connected power converters, in others words, this loop implement the parallelism action. In this case, because the converter has four wires, hence, is necessary to read VA, VB and VC, as well, iA, iB and iC.

The line voltage control loop employs a PID controller, while the current control loop uses just a proportional controller K as proposed in. According that there are four–wires is necessary to employ a control structure (both control loops) to each phase, as demonstrated in Fig.3.(b).

The parallelism control employs the feedback of the inductor currents from the output filter to modify the input voltages of the same filter and thereby control the power flow of each VSI to the load. The voltage control is responsible for controlling the output voltages of the LC filter, which coincides with the output voltages of the VSI. The proposed control strategy ensures the proper sharing of the load current and avoids current circulation among the inverters during transient and steady-state operation. One advantage of this control strategy is that the VSI only needs to receive an external signal (synchronism reference), in order to be connected in parallel. The control strategy does not have to exchange information among the VSIs regarding their operation points. Information flow occurs only in one direction, from a communication bus to the VSI. Furthermore, the parallelism control does not modify the reference voltages used for the voltage control.

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This characteristic keeps the output voltages of the VSI in synchronism with the reference voltages in the whole range of operation. Implementation cost of this control strategy in relation to other strategies is more one advantage. The proposed control does not have to do complex calculations, it does not add extra sensors and it does not need a complex communication system.

Therefore, its implementation is easier, cheaper and it can be done either with analog circuits as or digital circuits as. Nevertheless, before connecting the VSIs in parallel they need to receive the synchronism reference signal, as show in Fig.2.

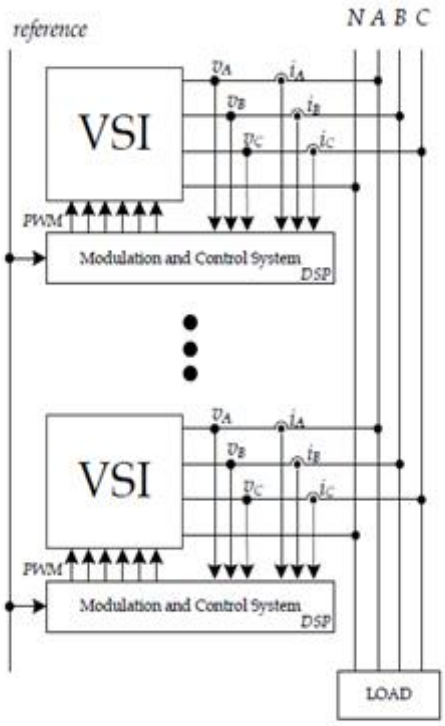

Fig. 2. Block diagram representation of proposed parallelism control strategy with n converters connected.

III Discrete-time control system design

In this moment the static and dynamic models are determined in space-state approach. Considering the average model of a single-phase of power converter, due to the three-phase has four wires, as demonstrated in Fig.3.(a) follows expressions are determined:

$$L_f \frac{d}{dt} i_f = u V_{dc} - v_f \quad (1)$$

$$C_f \frac{d}{dt} v_f = i_f - \frac{v_f}{R_o} \quad (2)$$

Hence, the state space representation $[\dot{x}]=[A][x]+[B]u$ *as:*

$$\frac{d}{dt}\begin{bmatrix} i_f \\ v_f \end{bmatrix} = \begin{bmatrix} 0 & \frac{-1}{L_f} \\ \frac{1}{C_f} & \frac{-1}{R_o C_f} \end{bmatrix} \begin{bmatrix} i_f \\ v_f \end{bmatrix} + \begin{bmatrix} \frac{V_{dc}}{L} \\ 0 \end{bmatrix} \quad (3)$$

The transfer function, in s domain, can be determined as:

$$\frac{i_f}{u} = \frac{V_{dc}(sR_oC_f+1)}{L_fC_fR_oS^2+L_fs+R_o} \quad (4)$$

$$\frac{v_f}{u} = \frac{V_{dc}R_o}{L_fC_fR_oS^2+L_fs+R_o} \quad (5)$$

The discrete-time PID project to regulates the line voltage and designed in classic form, which results as:

$$PID_k[z] \rightarrow \frac{u[z]}{e[z]} = \frac{12,81Z^2-23,64Z+10,91}{Z^2-1,025Z+0,02455} \quad (6)$$

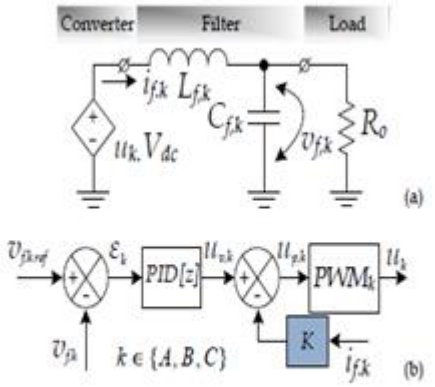

Fig. 3. (a) Equivalent circuit to determine the control transfer function. (b) Block diagram representation of control structure with current feedback.

This PID controller is equal for all phase, and in its design was considered the discrete-time effects, i.e. sampling, ZOH effect, computation delay and so. In the parallelism control loop, the controller K is determined as a virtual impedance that to limit the line current, as demonstrated in Fig.3.(b). This control loop

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is only employed because the n converters are slightly different, because, theoretically, the voltage supplied by them is equal. Hence, is necessary to design a control loop that ensures the proper sharing of the load current and avoids current circulation among the inverters during transient and steady state operation. This control loop design employs the Per Unit representation (PU), which is frequently used in Power System analysis. Hence, assuming that the independent base values are power (Sb) and voltage (Vb). In this ways, the base impedance is determined:

$$Z_b = \frac{V_b^2}{S_b}, \quad (7)$$

and, the gain K is defined as 0:1 pu of Zb. The action of the parallelism loop is similar a virtual impedance series connected of inductor in filter stage of power converter, as demonstrated in fig.4.

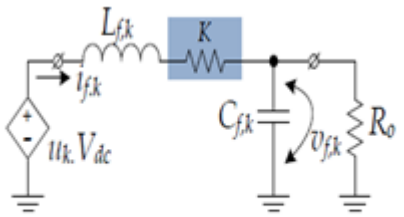

Fig. 4. A virtual impedance K guarantess the current sharing between power converters with fast dynamic response.

$$\frac{v_f}{u} = \frac{k_M R_o}{L_f C_f R_o S^2 + (L_f + C_f k_M K)S + R_o + k_M K} \quad (8)$$

$$\text{Where: } k_M = \frac{V_{dc}}{k_{PWM}}$$

The expression (5) and (8) were compared as depicted in Fig.5. As demonstrated the gain K in current feedback provides a damping in the system.

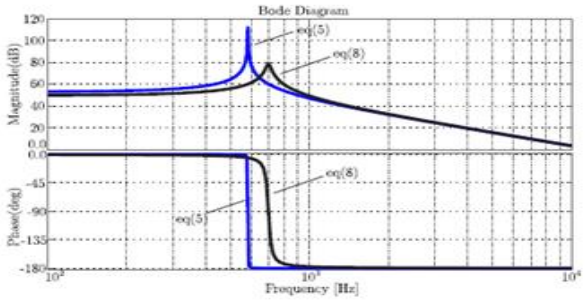

Fig. 5. Frequency response of both transfer function.

IV Synchronism Reference Implementation

The synchronism reference bus can be fulfilled by an analog or digital signal shared among the inverters or even a digital communication such as: Controller Area Network, universal asynchronous receiver/transmitter, Inter-Integrated Circuit or parallel communication. The analog reference may be a sine signal, which is the voltage reference used in control system, or the phase reference. In both cases the signals are converted by an analog to digital converter. Systems using analog references are proposed in. The digital reference contains the information of frequency and the zero crossing of the voltage reference which are detected by the falling and rising edge of the signal. The analog and digital references are shown in the Fig. 6. The analog reference provides the exact point of operation in each sampling instant, while using the digital reference this information is only available twice in a cycle, in the falling and the rising edge. Using a digital communication to synchronize the inverters is more complex and the system may lose reliability due to the communication dependency, in this case it is necessary to take into account the transmission time of the data. A strategy for VSI parallel operation using CAN protocol is proposed in.

V Digital Signal Controller Implementation:

The control strategy is implemented in Digital Signal Controller – DSC, TMS320F28069, with floating-point unit. This device has several resources to implement the control strategy: (i) 16 ADC channels with 12 bits numeric resolution; (ii) 16 PWM channels, which 8 can be set to operates in high resolution mode; (iii) clock frequency is 90 MHz, which is sufficiently for all algorithms of control strategy, communication link, as well the protection system. Therefore this processor has the pertinent processing capability and also the peripheral resources required in proposed application. The firmware control and synchronism routine flowchart is shown in Fig. 7. The control routine is executed once in each switching period, and it is started by a PWM interrupt (PWM) at minimum carrier values. The synchronism routine (XINT) is

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started by an external interrupt which is generated by the falling and the rising edge of the digital reference.

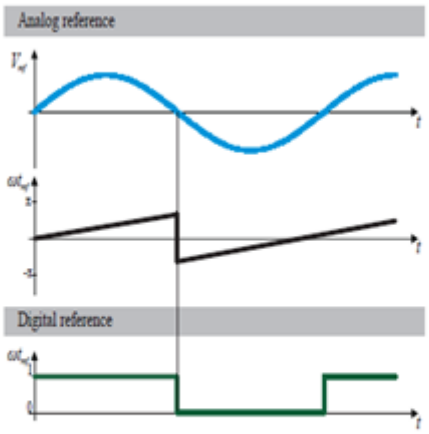

Fig. 6. Analog and digital reference.

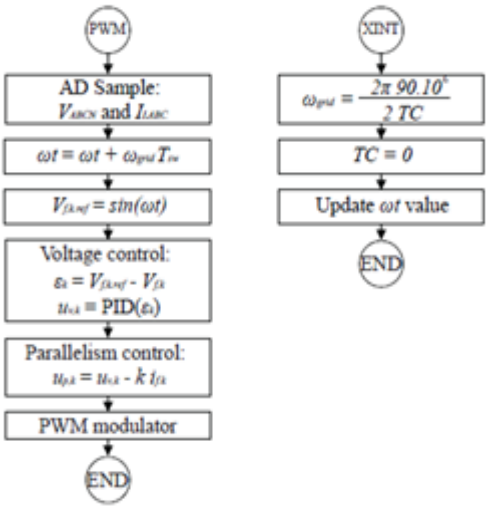

Fig. 7. Firmware control and synchronism routine flowchart.

The PWM interrupt routine is responsible for the control, it is sampled the control variables, incremented the phase reference and calculated the voltage reference used in the control. Afterward it is executed the voltage control and the parallelism control. The external interrupt is responsible for the synchronism the reference frequency is calculated based on a timer counter (TC), when this interrupt occurs it is also updated the phase reference value (!t) to synchronize the internal reference with the external digital reference.

VI SIMULATION RESULTS

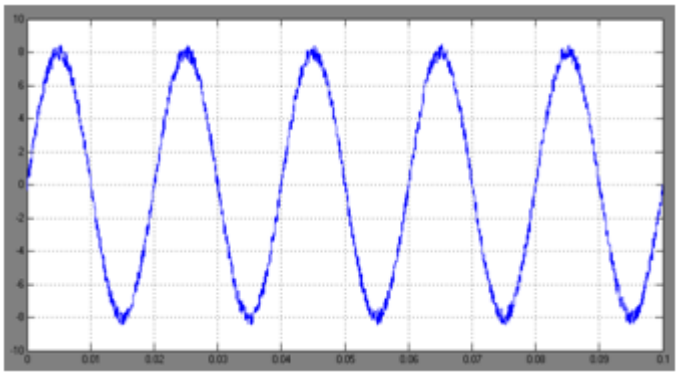

FIG 8 LOAD CURRENT USING PI CONTROLLER

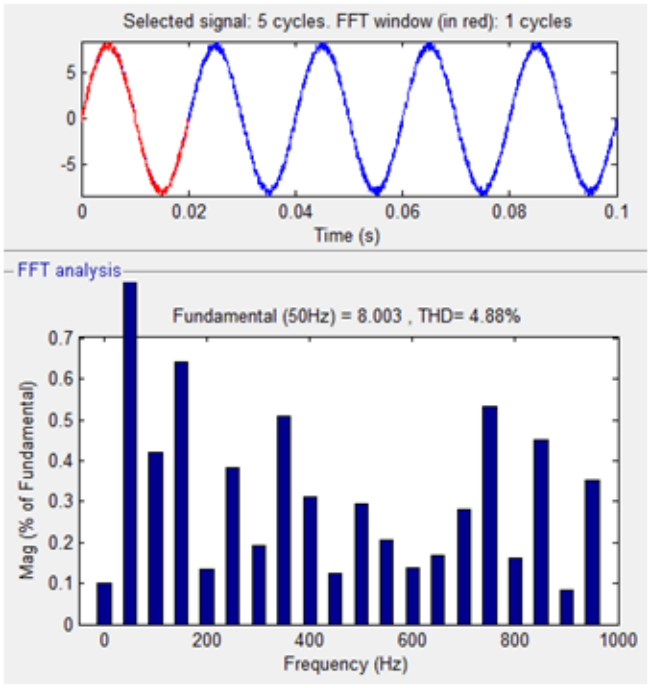

FIG 9 THD LOAD CURRENT USING PI CONTROLLER

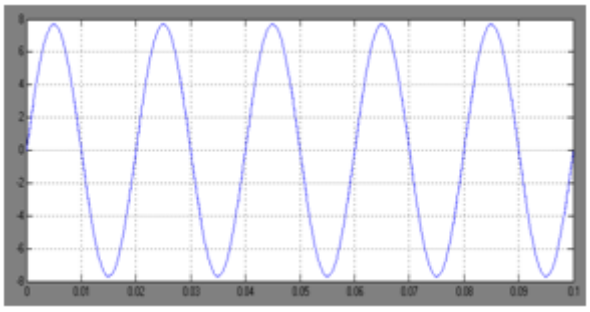

FIG 10 LOAD CURRENT USING FUZZY CONTROLLER

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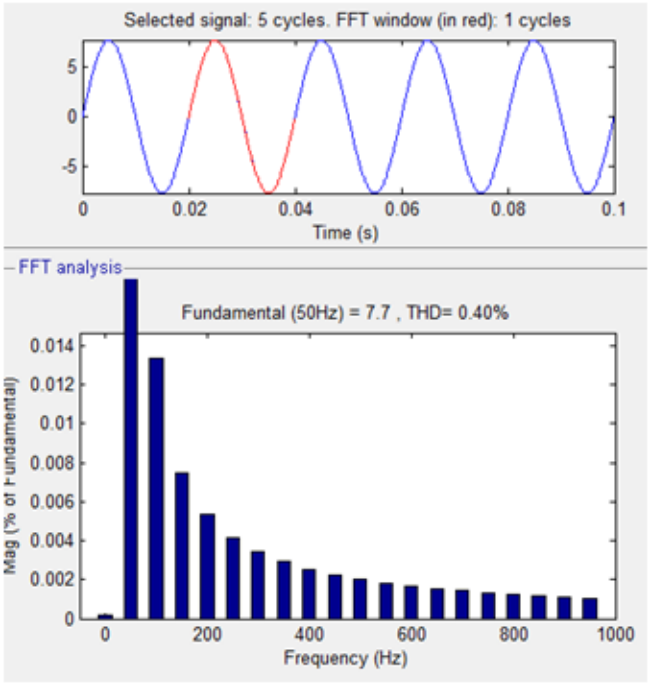

FIG 11 THD LOAD CURRENT USING FUZZY CONTROLLER

VII CONCLUSION

This paper proposes a technique for the parallel operation of four-wire voltage source inverter, which is digitally implemented in DSP. The proposed control strategy ensures the proper sharing of the load current and avoids current circulation among the inverters during transient and steady state operation. In the control structure is based on two control loops: a line voltage control loop and a parallelism control loop. There is also a communication bus among the inverters, in which a reference voltage is shared among the inverters. The paper approaches details on implementation of power circuit, digital control system and tests. Simulation and experimental results are reported herein to verify the proposed strategy and they show that strategy is robust, it presents high-reliability and can be used to obtain redundant systems, what becomes proposed control strategy appropriate for UPS applications.

The future work is to replace a conventional PID controller with fuzzy PID controller and simulations are done in MATLAB 2009.the results of both conventional and fuzzy PID controller will be compared and the comments will be given.

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