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Soft Switching Scheme for Three Phase Three Level Dc-Dc Converter with Asymmetrical Duty Cycle Control

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ABSTRACT:

Thispaperproposes development of soft switching scheme for three phase three level DC-DC converter for different duty cycles to achieve ZVS for all switches.The ZVS is achieved with output inductor and leakage inductor of transformer. This paper describes the main operational modes of proposed converter for different duty cycle and simulation results are observed and compare the switching losses of proposed converter with and without ZVS.

KEYWORDS:

Zero Voltage Switching (ZVS), Three Phase Three Level (TPTL),DC-DC converter ,Pulse width modulation ,Duty cycle ,Soft switching.

I.INTRODUCTION:

In high voltage high power applications the ordinary converters exists many problems like stress on switches, switching losses, EMI etc…. These problems can be eliminated by using ZVS and ZCS converters. In ZVS, the switches are turned on and off at zero voltages and in ZCS, the switches are turned on and off at zero currents. As a result power reduces almost to a least value, by which the stress onthe switchescan be reduced .Full-bridge dc/dc converters have been widely used in medium to high power applications to further reduce the stress on switches for high power application TPTL was proposed. With three phase architecture the converter has the superior features including lower current rating of switches reducing input output current ripple allowing small size filter requirement.Although predominant characteristics exist in TPTL soft switching has not been achieved which limits the switching frequency and power loss. The use of Asymmetrical duty cycle in the three phase three level dc/dc converter was proposed in order to achieve ZVS commutation over a wide load range.

II. PROPOSED TPTL DC/DC CONVERTER FOR DIFFERENT DUTY CYCLES:

Fig. 1 shows the circuit configuration of TPTL converter-in which, a three-phase transformer with Δ–Y connection is employed for the smaller turn's ratios and transformer VA rating. As shown, Lra, Lrband Lrcare the additional resonant inductances to widen the ZVS commutation load range. Llka, Llkb, and Llkcare the equivalent primary leakage inductances of each phase. Df1 and Df2 are freewheeling diodes. Cssis the flying capacitor, which is in favor of decoupling the switching transition of Q1,Q3,Q4, and Q6.DR1− DR6arerectifier diodes. The output filter is composed of Lfand Cf,andRLdis the load.Fig. 2 shows the control strategy of proposed converter.To realize the soft-switching for switches, the original interleaved switches should be designed in a complementary manner, and a short delay time td is necessary to be introduced between the two complementary switches to provide an interval for the ZVS commutation, which is similar to the control strategy of asymmetrical half-bridge converter .Accordingly, the duty cycles of Q1,Q3 , and Q5 are served to regulate the output voltage, while thedrive signals of Q4,Q6 , and Q2 are complementary to that of the Q1,Q3 , and Q5, respectively.

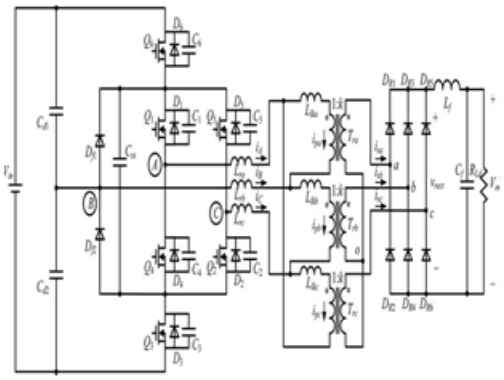

Fig 1: Topology configuration of TPTL dc/dc converter.

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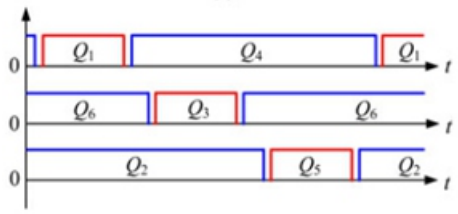

Fig 2: Asymmetrical duty cycle control.

III. OPERATION OF PROPOSED TPTL CONVERTER:

This section will analyze the operation principles of the TPTL converter under the modified control scheme. The following assumptions are made for the simplicity before the analysis:

1) all power devices and diodes are ideal;
2) all capacitors and inductances are ideal;
3) the output filter inductance is large enough to be treated as a constant current source during a switching period; its value equals to output current
4) the inductances of each phase are identical, i.e., Llka=Llkb= Llkc= Llk, Lra= Lrb= Lrc= Lr;
5) C1 = C2 = C3 = C4 = C5 = C6 = Cp.

Fig. 3 shows the key waveforms of the TPTL converter with asymmetrical duty cycle control, as seen, the operation of the TPTL converter can be classified by different modes, according to the duty cycle range and the load current. The corresponding operation modes are defined as the small duty cycle mode (SDCM), and the large duty cycle mode (LDCM).

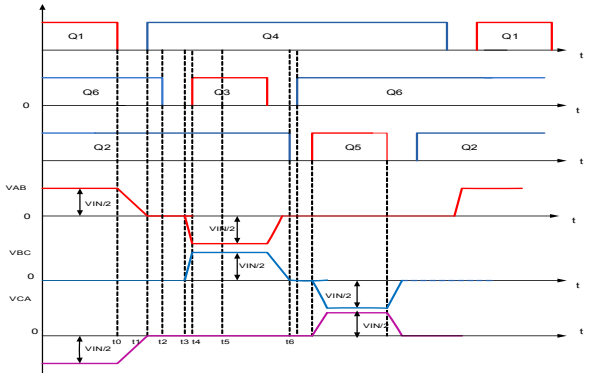

Fig 3: Key waveforms of the TPTL converter with asymmetrical duty cycle control with SDCM.

The basic equations of the voltages and currents of the transformer are listed as follows:

$$V_{AB}+V_{BC}+V_{CA}=0 \quad (1)$$

$$i_{sa}+i_{sb}+i_{sc}=0 \quad (2)$$

$$\frac{dia}{dt}=k\frac{(disa)}{dt}=\frac{vLlka}{Llk},\frac{dipb}{dt}=k\frac{(disb)}{(dt)}$$

$$=\frac{vLlkb}{Llk},\frac{(dipc)}{dt}=k\frac{(disc)\_VLlkc}{dt\quad Llk} \quad (3)$$

Where k represents the secondary-to-primary turns ratios of the transformer. The voltage across the leakage inductance of transformer can be derived from (2) and (3) and is given as follows

$$V_{Llka}+V_{Llkb}+V_{Llkc}=0. \quad (4)$$

Stage1[0 -t0]:

Fig.4(a)ShowsQ1,Q2,Q6,andDf2are conducting at the primary side, and DR1 and DR6are conducting at the secondary side. VAB= Vin /2, VBC= 0,and VCA= −Vin /2. From (1), (2), (4), and other constraints between voltages and currents of transformers, the following expressions can be obtained.

$$Vpa=\frac{Vin}{2},Vpb=0,Vpc=-\frac{Vin}{2} \quad (5)$$

$$Vrect=Vsa-Vsc.k.Vin \quad (6)$$

Where VpiandVsiare the primary voltage and secondary voltage of transformers, I represents the subscripts a, b, and c.

Stage 2[t0- t1]:

Fig.4 (b)ShowsAtt0,Q1is turned off, the line current iAchargesC1 and discharges C4 linearly, and the rectified voltage decreases. As C1 limits the rising rate of the voltage across Q1,Q1is zero-voltage turn-off. The voltages across C1 and C4 are

$$Vc1(t)=\frac{1}{Cp}kIo(t-to) \quad (7)$$

$$Vc4(t)=\frac{Vin}{2}-(\frac{1}{cp}k.Io(t-to)) \quad (8)$$

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At t1, vC1 rises to VIN /2, and VC4 decays to zero; therefore,D4conducts naturally, and Vrect decreases to zero.

Stage 3[t1- t2]:

Fig.4(c)ShowsafterC1 is fully charged, the current flowing through C1 transfers to Cssand begins to charge Css. The voltage across Csswill increase and block Df2 to be off. During this stage, VAB= VBC= VCA= 0. D4 conduct sand clamps the voltage across Q4 at zero, so Q4 can be turned on at zero-voltage condition. DR1 and DR6 conduct, and Vrectis still zero.

Stage4[t2- t3]:

Fig.4 (d) Shows At t2,Q6is zero-voltage turned-off and VABincreases reversely. If vpakeepsconstant,the polarity of the voltage applied on Llkawill be non associated with the current flowing through Llka; as a result, ipawill decrease and cannot provide the load current, then DR3 begins to conduct, and the current commutation between DR1 and DR3occurs. In the primary stage, C3 and C6 resonate with the leakage inductances and the resonant inductances, and the following expressions will be obtained.

$$Vc3(t) = \frac{Vin}{2} - (\frac{1}{2}k.Io.Zr.\sin[\omega r(t-t2)]) \quad (9)$$

$$Vc6(t)=(\tfrac{1}{2}k.Io.Zr.\sin[\omega r(t-t_2)] \quad (10)$$

$$i_{A(t)} = \frac{3}{2}k.Io + \frac{1}{2}k.Io\cos[\omega r(t-t2)] \quad (11)$$

$$i_{B(t)} = -k.Io\cos[\omega r(t-t2)] \quad (12)$$

$$i_{C(t)} = -\frac{3}{2}k.Io + \frac{1}{2}k.Io.\cos[\omega r(t-t2)] \quad (13)$$

During this stage, V_{rect} remains at zero. When V_{c3} decays to zero, D_3 conducts naturally.

Stage5[t3-t4]:

Fig.4 (e) Shows As D3 is conducting, the voltage across Q3 is clamped at zero; therefore, Q3 is turnedon at zero-voltage condition. During this stage, Q2,Q3, and Q4 conduct in the primary stage, VAB= −Vin /2, VBC= Vin /2, and VCA= 0. DR1,DR3, and DR6 conduct in the secondary stage, and Vrect= 0. From (1), (2), (4), and other constraints between voltages and currents of transformers, the expressions of the phase currents are given in (14)–(16)

$$i_{pa(t)} = i_{pa(t3)} - \frac{Vin}{2Lp}.(t-t3) \quad (14)$$

$$i_{pb(t)} = i_{pb(t3)} + \frac{Vin}{2Lp}.(t-t3) \quad (15)$$

$$i_{pc(t)} = -kIo \quad (16)$$

Therefore, the line currents can be obtained from (14) to (16)

$$i_{A(t)} = i_{A(t3)} - \frac{Vin}{2Lp}.(t-t3) \quad (17)$$

$$i_{B(t)} = i_{B(t3)} + \frac{Vin}{Lp}.(t-t3) \quad (18) \quad i_{c(t)} = i_{C(t3)} - \frac{Vin}{2Lp}.(t-t3) \quad (19)$$

At the secondary stage, Isaflows through DR1 and decreases with ipafrom (14).When Isadecreases to zero, DR1 turns off and DR2 conducts. It should be noted that the rectified voltage is lost during the interval t34, compared with the primary line voltage. Therefore, the duty cycle loss in SDCM is defined as

$$Dloss1 = \frac{t34}{\frac{Ts}{3}} = \frac{6k.Io.Lp}{Vin.Ts} \quad (20)$$

Where Tsis the switching period.

Stage 6 [t4-t5]:

Fig.4 (f) Shows During this stage, VAB=−Vin /2, VBC= Vin /2, VCA= 0.

Iscflows through DR6, iscand decreases with ipc. When iscdecreases to zero, DR6 turns off, the primary and secondary currents of transformer Trcare both zero. The time interval of this stage is given by

t45=(4k.Io.Lp)/Vin (21)

Stage 7[t5- t6]:

Fig.4 (f) ShowsQ2,Q3, and Q4 conduct at the primary side, while DR2 and DR3 conduct at the secondary side, and the rectified voltage is kVin, whichissimilartothestage1.

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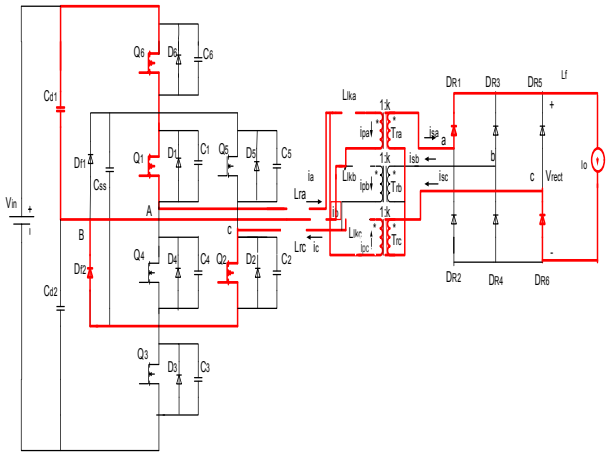
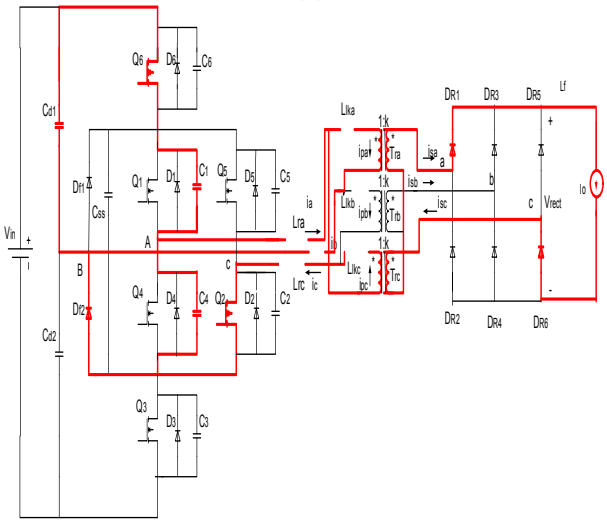


4 (a)



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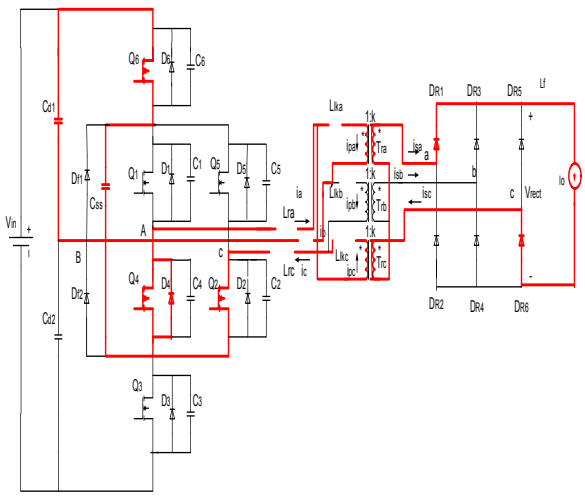
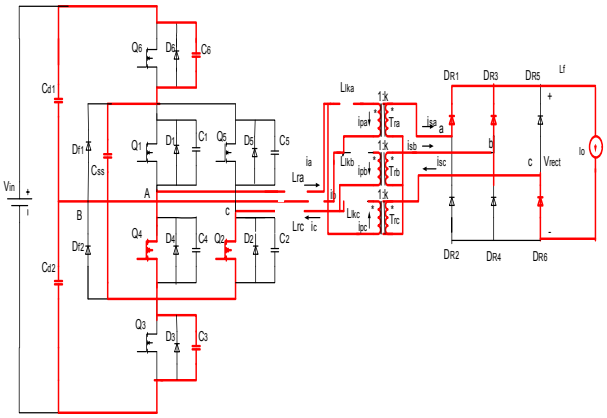
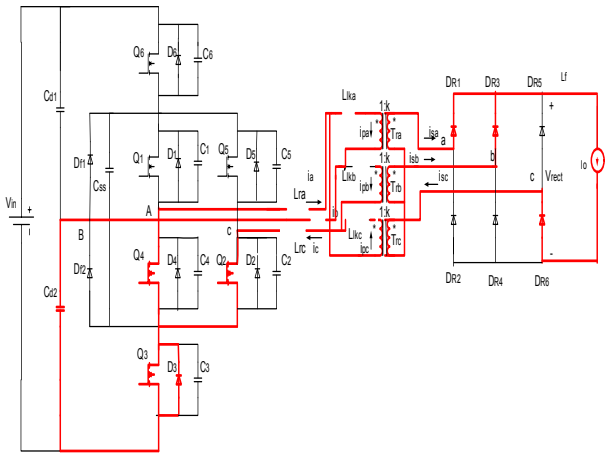


4 (c)

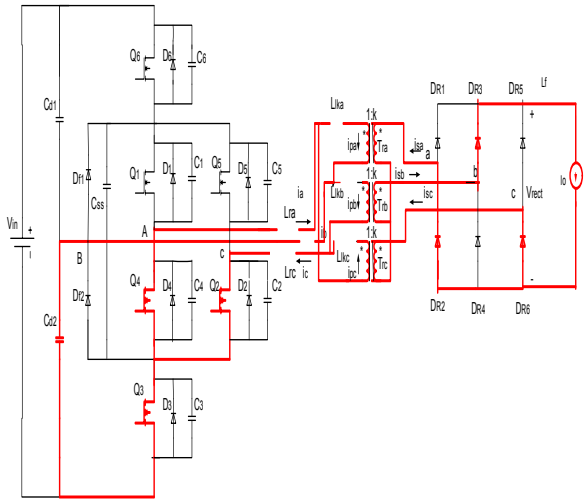
Fig 4: Equivalent circuits under different operation stages. (a) Prior to[0 t0] . (b) [t0, t1]. (c) [t1, t2]



4 (d)



4 (e)



4 (f)

Fig 4: Equivalent circuits under different operation stages (d) [t2, t3]. (e) [t3, t4]. (f) [t4, t5]

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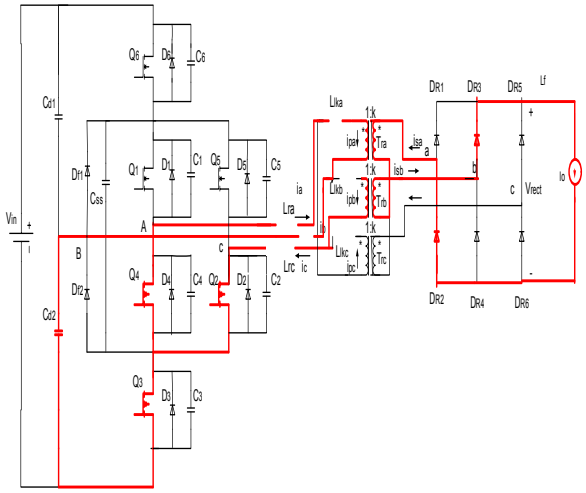

4 (g)

Fig 4: Equivalent circuits under different operation stages (g) [t5, t6]

IV.SIMULATION RESULTS FOR THREE PHASE THREE LEVEL DC/DC CONVERTER:

In fig.5 Simulink modelof a 200V/16V DC-DC converter has been proposed. In fig.6.output waveforms of the proposed converter is shown. In the proposed converter there is total six switches out of it Q1,Q3,Q5 are given with same duty cycle and Q2,Q4,Q6 are same having same duty cycle.

Though the switches have same duty cycle all the switches not on for the same time In the proposed converter there are total six switches in which all are under goes soft switching for different duty cycles Fig.7 & Fig.8 shows the simulation results for D=20%.

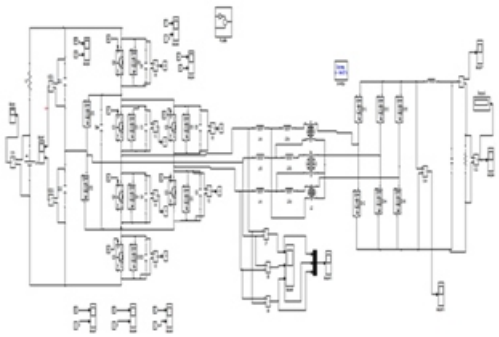

Fig 5: Simulink diagram of three phase Three-Level DC-DC converter

As the duty cycle increases the output voltage will increasesis shown in Table 1 .In which the output voltage will increases form D=20% to 46% and efficiency also increases.Fig6 represents output waveforms of the converter and three phase output voltage also observed in which all the phases are shifted by 120°.Fig7 represents soft switching of the proposed converter for Q1 and Q4 switches .Which is also same for Q2,Q3,Q5,Q6.Fig.7a showsvoltage across Q1,fig 7b.shows the ZVS for Q1 from off to on &fig7c shows on to off of Q1 under the ZVS. Fig 8a shows voltage across Q4,fig 8b.shows the ZVS for Q4 from off to on &fig 8c.shows on to off of Q4 under the ZVS.Fig9 shows graph between efficiency and load current at duty cycle D=20%,which will also represents the efficiency is high for with soft switching than without soft switching.

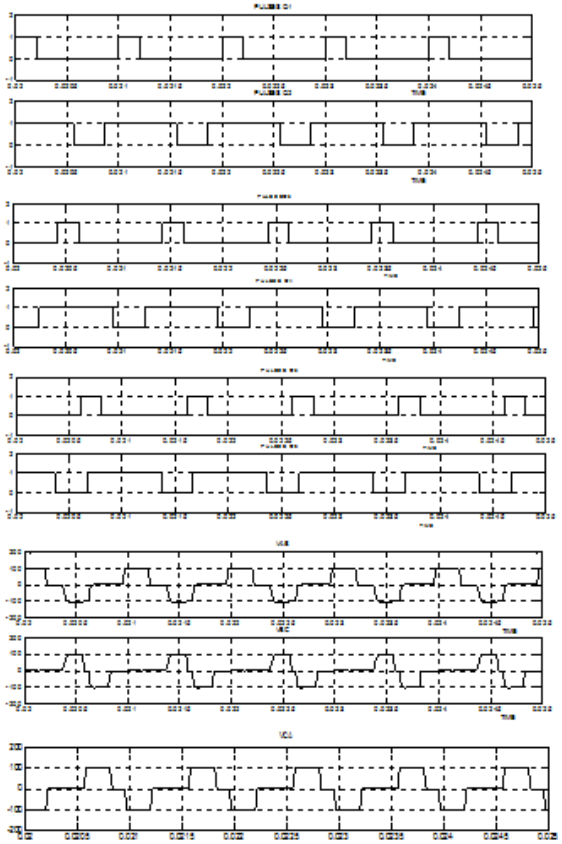

Fig 6: output waveform
Simulation results for Duty cycle 20%
Voltage across Q1

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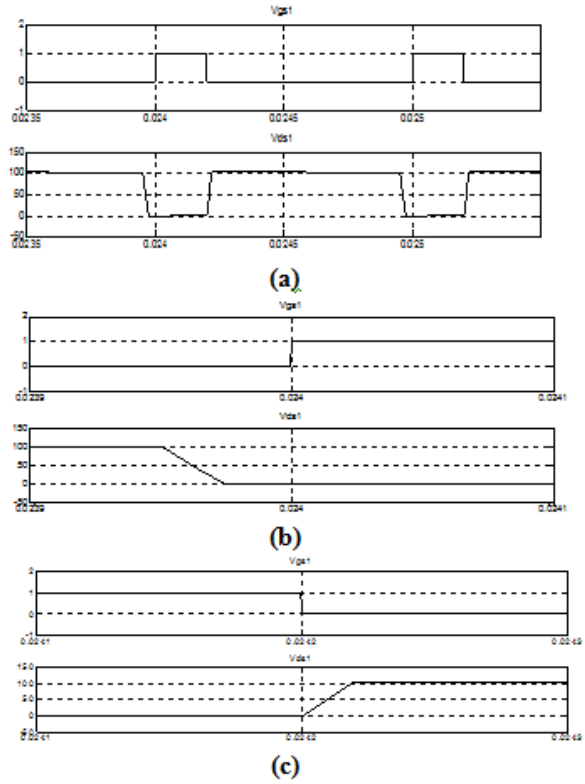

Fig7: for 20% duties cycle (a) voltage across switch Q1, (b). zvs turn off-on Q1(c)zvs turn on-off Q1.

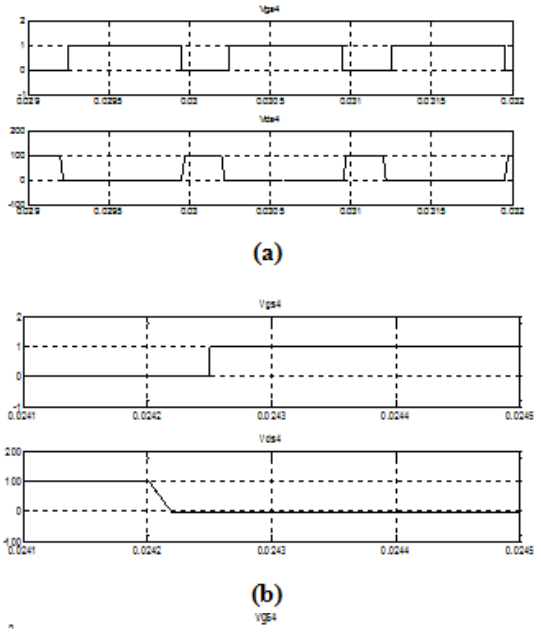

Fig8: for 20% duty cycles (a) voltage across switch Q4, (b). zvs turn off-on Q4(c) zvs turn on-off Q4.

TABLE1:

Duty cycle (%)	Output voltage (V)	Efficiency with soft switching (%)	Efficiency without soft switching (%)
15	6.56	51.78	38.29
20	11.7	64.67	44.1
30	13.95	69.81	50.36
40	15.33	71.45	54
48	15.8	81.87	57.77

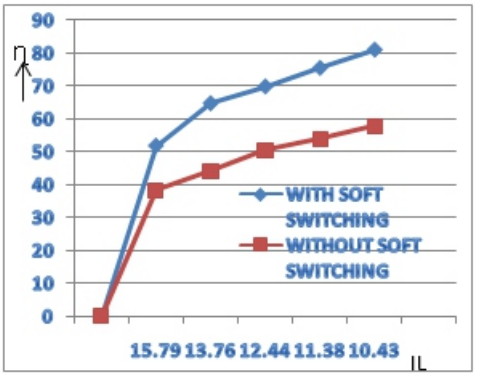

Fig 9: Load current Vs Efficiency at D=20%

IV. CONCLUSION:

Soft switching scheme is achieved in each and every switch. Voltage stress across each switch was reduced. By increasing the voltage levels the size of the filter elements may also reduce. The switching losses in the proposed converter are reduced. The proposed control scheme features the following characteristics:

1) Compared with the hard switching technique the losses in switches predominately reduced

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2) The input capacitors can realize automatic and inherent voltage balancing, which ensures that all the switches sustain only one-half of the input voltage.3)The TPTL converter will operate in different duty cycles.

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