ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Gaussian Pulse Shaped QPSK Modulator

J.Lingaiah, M.E
Associate Professor & HoD
Department of ECE
Arjun College of Technology & Science.

Mrs.K.Sridevi, M.Tech (ECE)
Assistant Professor
Department of ECE
Arjun College of Technology & Science.

Kasula Ajay Kumar
M.Tech (VLSI)
Department of ECE
Arjun College of Technology & Science.

Abstract:

This paper work proposes a new technique of parameterization and present a programmable baseband modulator (PBM) that perform the QPSK modulation schemes and as well as its other three commonly used variants to satisfy the requirement of several established 2G and 3G wireless communication standards as an example of the proposed technique. The pulse shaping root raised cosine (RRC) filter will be implemented to with stand a peak inter-symbol interference (lSI) distortion of -41 dB using distributed arithmetic (DA) technique in order to reduce the computational complexity, and to achieve appropriate power reduction and enhanced throughput.

The architecture will be developed in VHDL. The Modelsim Xilinx Edition tool will be used for functional simulation and Xilinx ISE tools will be used for synthesis. Xilinx FPGA board will be used to test the developed architecture.

INTRODUCTION

Introduction to Software Defined Radio (SDR)

With the exponential growth in the ways and means by which people need to communicate - data communications, voice communications, video communications, broadcast messaging, command and control communications, emergency response communications, etc. - modifying radio devices easily and cost-effectively has become business critical. Software defined radio (SDR) technology brings the flexibility, cost efficiency and power to drive communications forward, with wide-reaching benefits realized by service providers and product developers through to end users.

Software Defined Radio is a radio communication technology that is based on software defined wireless communication protocols instead of hardwired implementations. In other words, frequency band, air interface protocol and functionality can be upgraded with software download and update instead of a complete hardware replacement. SDR provides an efficient and secure solution to the problem of building multi-mode, multi-band and multifunctional wireless communication devices.

Traditional hardware based radio devices limit cross-functionality and can only be modified through physical intervention. This results in higher production costs and minimal flexibility in supporting multiple waveform standards. By contrast, software defined radio technology provides an efficient and comparatively inexpensive solution to this problem, allowing multi-mode, multi-band and/or multi-functional wireless devices that can be enhanced using software upgrades.

Quadrature Phase Shift Keying (QPSK)

$$S(t) = S_I(t)\cos(2\pi fct) - S_Q(t)\sin(2\pi fct)$$

Where $S_I(t)$ is the in-phase component of the modulated wave, and $S_Q(t)$ is the quadrature component. The Cosine and Sin waves of the carrier wave are in-phase quadrature with each other.

This modulation scheme is characterized by the fact that the information carried by the transmitted wave is contained in the phase. In QPSK, the phase of the

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

carrier takes on one of four equally spaced values, such as π/4, 3π/4, 5π/4 and 7π/4.

Signal Space Characteristics of QPSK

Table 11.1: Signal Space Characteristics of QPSK

Input di bit 0≤t≤T	Phase of QPSK signal (radians)	Coordinates of message points S_i1 S_i2	
10	π/4	+√E/2	-√E/2
00	3π/4	-√E/2	-√E/2
01	5π/4	-√E/2	+√E/2
11	7π/4	+√E/2	+√E/2

Accordingly, a QPSK signal is characterized by having a two dimensional signal constellation (i.e. N=2) and four message points (i.e. M=4).

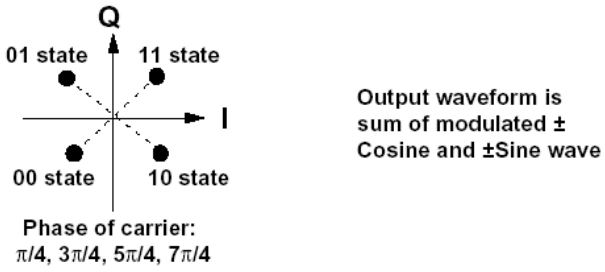

Figure 1: Constellation Diagram for QPSK

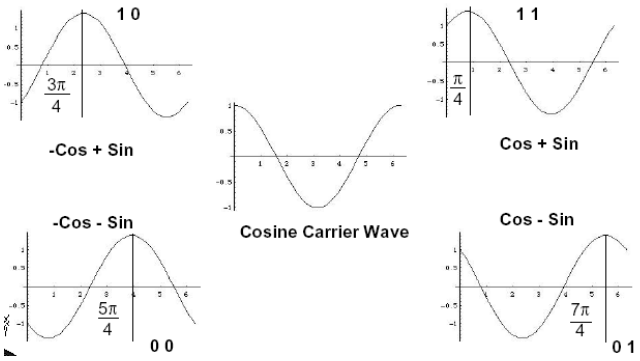

Figure 2: Waveform Representation of QPSK

Offset Quadrature Phase Shift Keying (OQPSK)

OQPSK signaling is similar to QPSK signaling except for time alignment of the even and odd bit streams. In QPSK signaling the bit transitions of the even and the odd bit streams occur at the same time instance, but in OQPSK signaling, the even and odd bit streams, $m_I(t)$ and $m_Q(t)$,are offset in their relative alignment by one bit period (half symbol period). To prevent the regeneration of side lobes and spectral widening, it is imperative that QPSK signals that use pulse shaping be amplified only using linear amplifiers, which are less sufficient.

π/4 Quadrature Phase Shift Keying(π/4 QPSK)

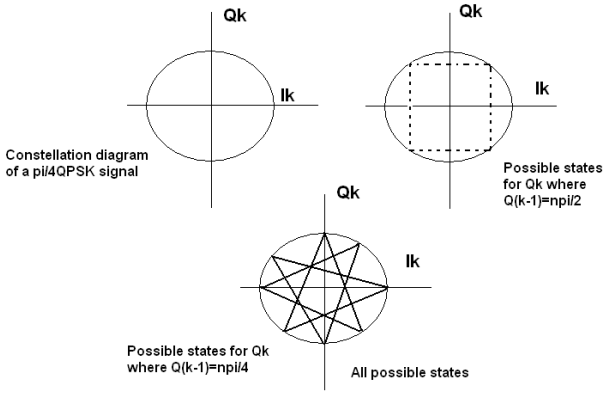

Figure 3: Constellation Diagram of π/4QPSK Signal

Can be non-coherently detected, thus greatly simplifies the receiver design. π/4 QPSK can be differentially encoded to facilitate easier implementation of differential detection with phase ambiguity in the recovered carrier. In a π/4 QPSK modulator, signaling points of the modulate signal are selected from two QPSK constellations which are shifted by π/4 with respect to each other.

The in phase and in quadrature bit streams I_k and Q_k are then separately modulated by two carriers, which are in quadrature with one another to produce π/4 QPSK waveforms given by :

$$\pi/4 \text{ QPSK } (t) = I(t) \text{ Coswct} - Q(t) \text{ Sinwct}$$

Both I_k and Q_k are usually passed through Raised Cosine roll off pulse shaping filters before modulation, in order to reduce bandwidth occupancy.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

I_k and Q_k and the peak amplitudes of waveforms I (t) and Q (t) can take one of the five possible values. 0, 1, -1, $1/\sqrt{2}$, $-1/\sqrt{2}$.

Up Sampling

If the information source is analog, the information must be transformed into a digital format. Through use of the sampling process, an analog signal is converted into a corresponding sequence of samples that are usually spaced uniformly in time.

To recover original information from sampled waveform, we must satisfy sampling theorem. The sampling theorem is that a band limited signal of finite energy, which has no frequency components higher than ω Hz, is completely described by specifying the values of the signal at instants of time separated by 1/2ω Seconds.

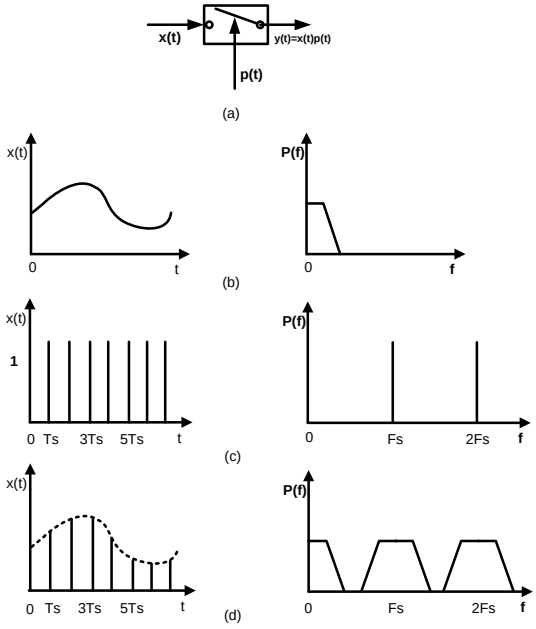

Figure 4: (a) sampling process (b) information signal (c) sampling function (d) sampled signal

Often a signal with sampling frequency fs needs to be sampled to a higher sampling frequency of β1fs, where β_1 is the interpolation ratio. The interpolation process involves inserting zeros in between each sample while not changing the frequency spectrum of the baseband signal. This process is shown through figure

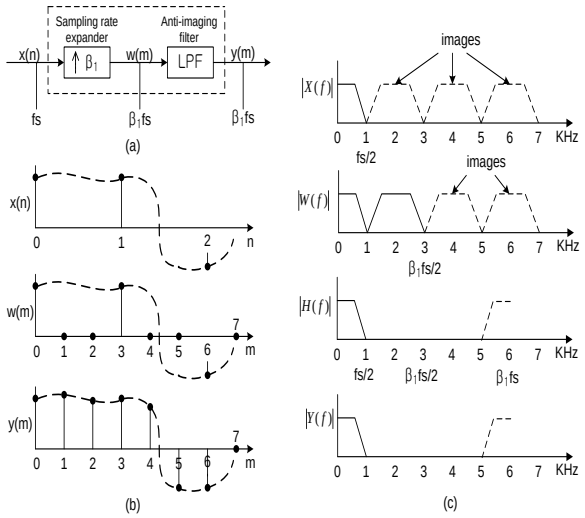

Figure 5: (a) Interpolator (β_1 =3) (b) Time domain (c) Frequency domain (f_S =2 KHz)

Then, what are advantages of oversampling? The main reason of over sampling is that analog filters have two undesirable characteristics. First, they can exhibit distortion due to narrow bandwidths. Second, the cost can be expensive because a sophisticated analog filter with a narrow bandwidth requires a large number of high-quality components. However, we want to use a low-cost, less sophisticated analog filter with a wide bandwidth.

Root Raised Cosine Filters\

The raised-cosine filter is a filter frequently used for pulse-shaping in digital modulation due to its ability to minimize intersymbol interference (ISI). Its name stems from the fact that the non-zero portion of the frequency spectrum of its simplest form (α = 1) is a cosine function, 'raised' up to sit above the f (horizontal) axis. The roll-off factor, α, is a measure of the excess bandwidth of the filter.

Filter Solutions provides analog, IIR and FIR raised cosine filters. FIRs are the most accurate and are best to use. However, if it is not possible to use an FIR filter, analog filters may approximate the raised cosine response. The higher the order of the filter is the

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

greater the raised cosine approximation. High order raised cosine filters also produce longer time delays.

IMPLEMENTATION

The proposed architecture focuses on the hardware multiplexing technique, where the hardware can be efficiently shared and utilized between different operations. This in turn leads to reduced area and power consumption at a reasonable data rate. By integrating several of modulation schemes in one common structure, and reusing the hardware for different standards one can minimize the amount of program memory in the processor, can save valuable development time, and reduce the development costs.

However in a reprogrammable multi-standard baseband processor, hardware multiplexing can often achieve comparable power consumption and lower silicon area than a fixed function circuit [14-15]. The architecture of the proposed programmable multi-standard baseband processor using hardware multiplexing technique is as depicted in Figure 2.1

Explanation on Working of Blocks

The key component of the multi-standard baseband processor, as shown in Figure 2.1 includes the (A) Serial to Parallel converter (shown as DG), (B) Symbol Mapper, (C) Upsampler, (D) Root Raised Cosine Filter as a pulse shaping filter, and (E) Carrier Generator (shown as CG) block.

Data Generator (DG)

A dummy data acquisition module accepts the digitized data from the Analog to Digital Converter (ADC) and then passes through a serial to parallel converter for dividing the incoming message bit stream into the even and odd bit stream. To accommodate the OQPSK scheme a delay of one bit period has been placed in the quadrature data stream path.

Symbol Mapper

Symbol Mapper block contains the four different IQ mapper blocks for four different modulation schemes for generating the carrier signal. It takes the even and the odd bit stream from the data generator block and generates a stream of mapped I and Q bit streams each of 3-bit length. The symbol mapper block consists of four blocks described below which can be chosen by the MOD_SEL parameter.

QPSK Mapper:

This block accepts the even and odd bit stream and generates a phase of the current bit sequence according to the TABLE I which causes the carrier to shift by 90^0 or 180^0. The shift in the carrier generates the symbols belonging to the set {-I, 0, I} for both I and Q data streams. The block diagram of the QPSK mapper block is as shown in Figure.

Table 22.1: Phase shift information of QPSK

Information Bits		Phase Shifts (Radians)
I	*Q*	
0	0	0
0	1	Π/2
1	0	Π
1	1	3Π /2

DQPSK Mapper:

The block schematic of the differential encoder is shown in Figure. The differentially encoded symbol is derived from the present and one of the last encoded symbols. Suppose the nth symbol, (n_l)th encoded symbol and the nth encoded symbol be represented as {In Qn), {I'n-I Q'n -I } and {I'n Q'n} respectively then the encoding scheme for the DQPSK modulation is carried out according to equations below:

$$I'_n = I_n\bar{I}_{n-1}\bar{Q}'_{n-1} + Q_n\bar{I}'_{n-1}Q_{n-1} + \bar{I}_nI_{n-1}Q_{n-1} + \bar{Q}_nI_{n-1}\bar{Q}'_{n-1}$$

$$Q'_n = Q_n\bar{I}_{n-1}\bar{Q}'_{n-1} + \bar{I}_n\bar{I}'_{n-1}Q_{n-1} + \bar{Q}_nI_{n-1}Q_{n-1} + I_nI_{n-1}\bar{Q}'_{n-1}$$

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

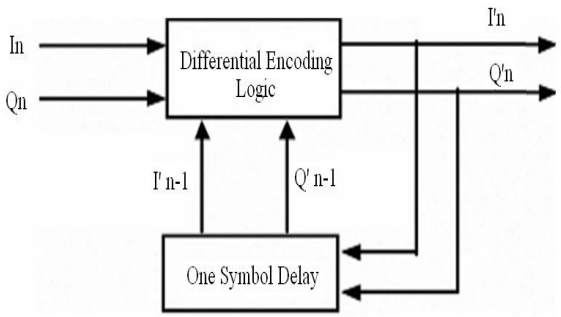

Figure 6: Block Schematic of Differential Encoding Pi/4 DQPSK Mapper

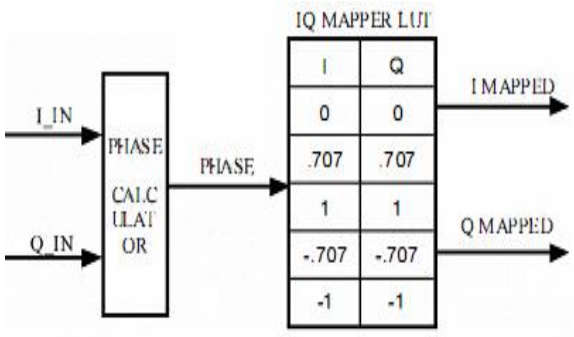

Figure 7: Block Diagram of IQ Mapper for QPSK, Π/4 DQPSK, OQPSK

It takes two bit at a time and assigned to one of the four possible differential phases as shown in TABLE . The actual information is placed into the differential phase of two successive symbols. The symbols corresponding to the possible state space of {-I, -0.707, 0, 0.707, I} will be generated for both of I and Q signal set. The block diagram of the pi/4DQPSK mapper block is as shown in Figure

Table 32.2: Phase Shift Information of Π/4 DQPSK

Information Bits		Phase Shifts (Radians)
I	*Q*	
0	0	Π/4
0	1	3Π/2
1	0	5Π/2
1	1	7Π /2

OQPSK Mapper

In OQPSK mapper the even and the odd signals are offset in their alignment by one bit period (half symbol period). For, due to the transition in the input symbol at any time only one of the two bit streams can change the value. Therefore the maximum phase difference of 90° can occur with the possible state space of {-0.707, 0.707} for I and Q component. The block diagram of the OQPSK mapper block is as shown in Figure.

Up sampler

Up sampler block takes the mapped data stream input from the previous block and will generate the up sampled I and Q data by a factor of 4. This up sampler block consists of ,a chain of registers connected serially which acts as a shift register. The seven prior symbols are loaded into the shift register and generate the addresses for the RRC filter.

Filter

The FIR filter is standard linear convolution, which described the output as convolution of input and impulse response of the filter.

Where c[n] values represent filter coefficients, and x[n] represents the input samples. The following figure shows the direct form FIR structure

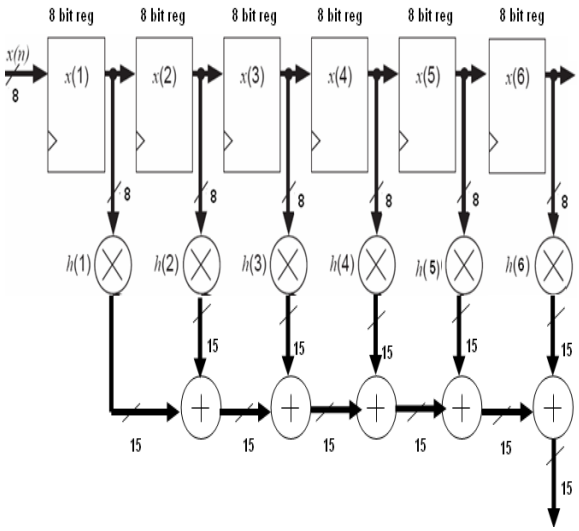

Figure 8: Direct form 6-tap FIR filter

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Carrier Generation

The basic block diagram of DDFS implemented is shown in the below Figure. All the blocks are connected with common clock and reset signals. The delta phase value decides the phase increment for each clock pulse. Hence decides the resulting signal frequency. The Frequency modulating instantaneous value is added to the delta phase value which causes instantaneous change in frequency. Due to the digital nature of the modulator only at each clock tick the modulating signal value shall affect the resulting frequency.

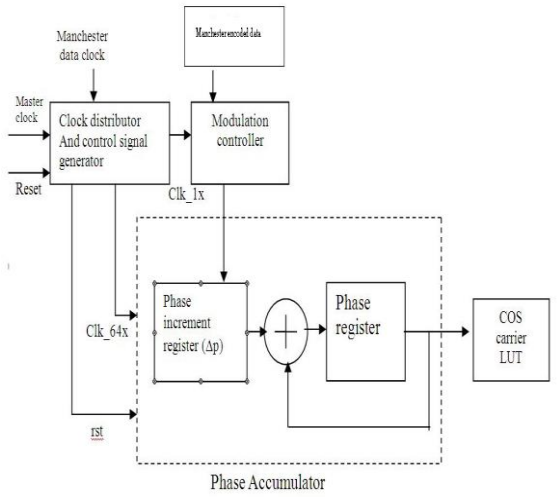

Figure 9: Basic Block Diagram of Direct Digital Frequency

Synthesizer implemented in this project

The phase accumulator produces accumulated phase value for each clock pulse. In case if the DDFS is used for phase modulation then instantaneous phase modulating signal value is added to the phase output of phase accumulator. This resulting phase value is given to the four Look Up Tables. Each Look Up Table is configured to produce a specific waveform.

The ModelSim tool from Mentor Graphics is used, for simulation and functional verification of DDFS. VHDL has been used as design entry method for all these blocks. Xilinx ISE (Integrated Software Environment) XST (Xilinx Synthesis Tool) is used as a synthesis tool to implement the design on Spartan-3E FPGA. Chipscope pro is used for analyzing the implemented design.

PIPO n bit generic register

The Parallel in Parallel Out shift register cells are required in phase accumulator block to hold frequency and phase values. Synchronization is required between the phase increment register and phase register. This is achieved by connecting a common clock signal.

SIMULATION AND SYNTHESIS REPORT

Top Level Simulation Results

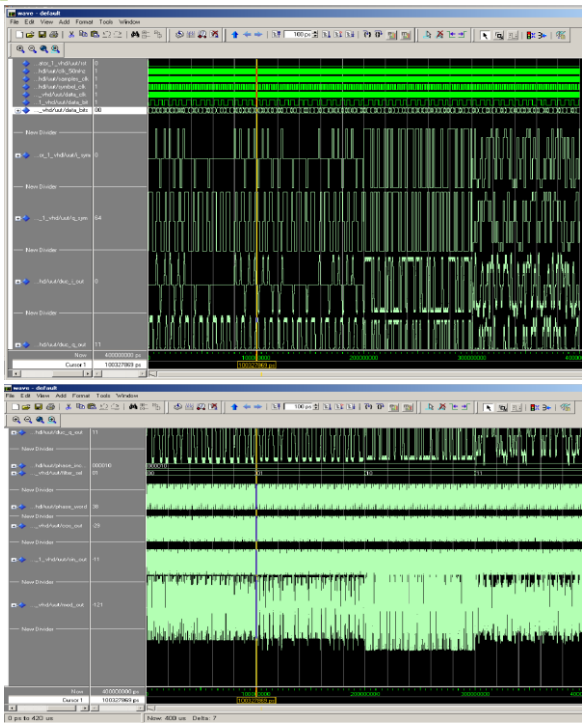

Figure 10: Top Level Simulation Results

Different Modulation Schemes Results

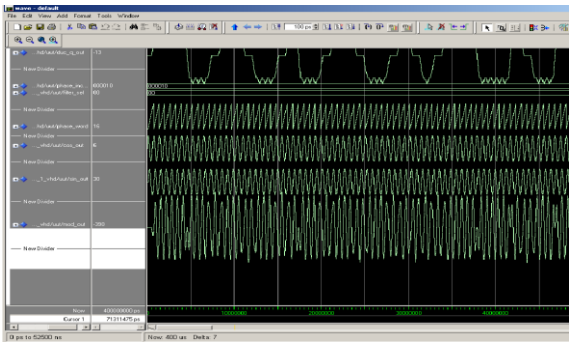

Figure 11: QPSK Modulation

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

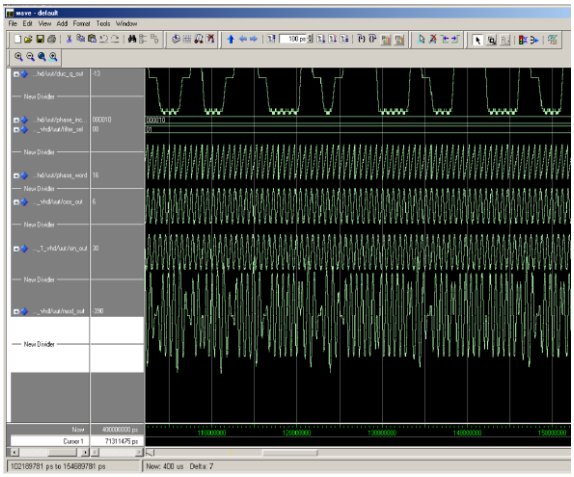

Figure 12: OQPSK Modulation

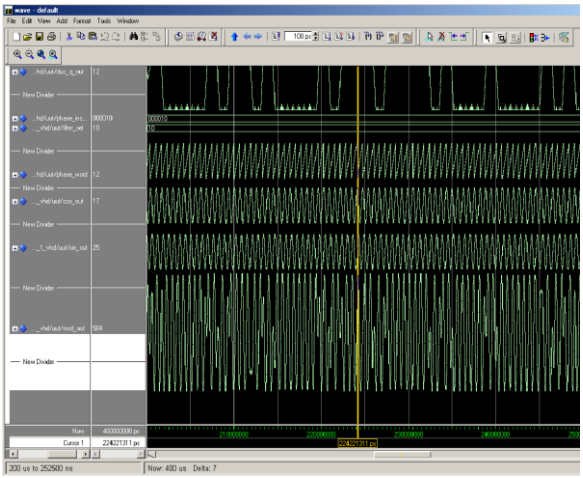

Figure 13: DQPSK Modulation

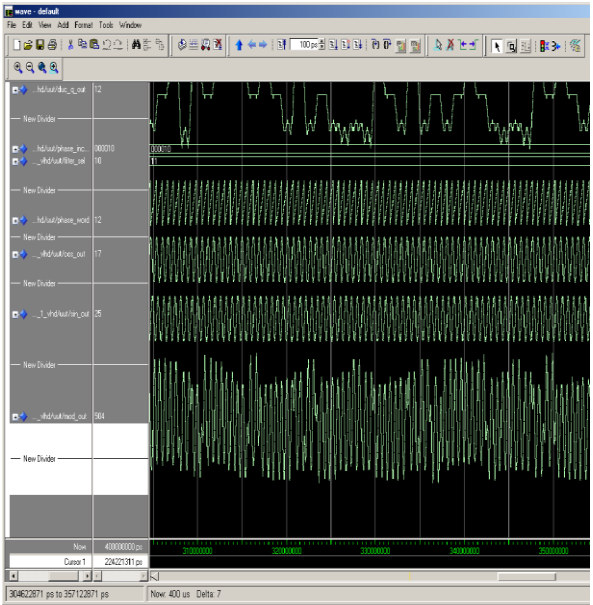

Figure 14: pi/4 QPSK Modulation

CONCLUSION

The proposed QPSK modulators successfully simulated on Xilinx ISE 12.4 software platform and the results obtain shows the correct functionality of the modulator as with the conventional architecture. While the power analysis tools used to estimate the power consumption on the proposed modulator shows that the proposed architecture consumes less power when compared with the conventional architecture. The power reduction can be achieved due to less usage of input/output logic block in FPGA in conjunction with the elimination of DDS in the new design.

REFERENCES

1. Aspel, D.T., 2004. Adaptive multilevel quadrature amplitude radio implementation in programmable logic. M.Sc. Thesis, University of Saskatchewan, Saskatoon, Saskatchewan.
2. Boerstler, D.W., 1999. A low-jitter PLL clock generator for microprocessors with lock range of 340-612 MHz. IEEE J. Solid-State Circ., 34: 513-519.
3. Burr, A.G., 1992. Comparison of coherent and noncoherent modulation in the presence of phase noise. IEE Proc. Commun. Speech Vision, 139: 147-155.
4. Chattopadhyay, S. and S.K. Sanyal, 2010. Evaluation of performance metrics for QPSK modulated mobile communication system using root raised cosine and raised cosine pulse-shaping filters. Proc. Int. J. Recent Trends Eng. Technol., 3: 25-29.
5. Chen, K.Z. and A.Q. Hu, 2008. MPSK demodulation algorithm based on pattern recognition. Proceedings of the IEEE International Conference on Neural Networks and Signal Processing, June 7-11, 2008, Nanjing, pp: 182-186.
6. Elamary, G., G. Chester and J. Neasham, 2009. A simple digital VHDL QPSK modulator designed using CPLD/FPGAs for biomedical devices applications. Proceedings of the World Congress on Engineering, Volume 1, July 1-3, 2009, London, UK., pp: 1-6.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

7. Kang, C.M., 2009. High performance PSK demodulator in FPGA for wireless communication receivers. White Papers, Innovative Integration.
8. Kao, C.H., 2002. Performance of the IEEE 802.11a wireless LAN standard over frequency-selective, slow, ricean fading channels. M.Sc. Thesis, Naval Postgraduate School, Monterey, California.
9. Kuon, I. and J. Rose, 2006. Measuring the gap between FPGAs and ASICs. Proceedings of ACM/SIGDA 14th International Symposium on Field Programmable Gate Arrays, February 22-24, 2006, Monterey, California, USA., pp: 21-30.
10. Langton, C., 2002. Unlocking the phase lock loop-part 1. http://www.complextoreal.com/chapters/pll.pdf.
11. Misra, D.K., 2004. Radio-Frequency and Microwave Communication Circuits: Analysis and Design. 2nd Edn., John Wiley and Sons Inc., New York, pp: 1-10.
12. Roddy, D., 2006. Satellite Communications. 4th Edn., McGraw Hill, New York.

Author Details

J.Lingaiah, M.E
Associate Professor & HoD
Department of ECE
Arjun College of Technology & Science.

Mrs.K.Sridevi, M.Tech (ECE)
Assistant Professor
Department of ECE
Arjun College of Technology & Science.

Kasula Ajay Kumar
M.Tech (VLSI)
Department of ECE
Arjun College of Technology & Science.