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VHDL Implementation of Optimized Cascaded Integrator Comb (CIC) Filters For Ultra High Speed Wide Band Rate Conversion

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Abstract:

Cascaded Integrator Comb (CIC) filters are widely used in Multirate signal processing as a filter in both decimator (decrease in the sampling rate) and interpolator (increase in the sampling rate). This paper discusses the architecture, design and implementation aspects of decimator and interpolator using CIC filter and comparison between the results in hardware and simulations. The hardware is implemented in FPGA and verified with Modelsim & Lab VIEW simulation results. CIC filters serve as powerful anti aliasing agents before decimation and anti imaging agents for interpolated signals. This paper also discusses about the method to improve the CIC attenuation. CIC Decimator and Interpolator were coded in Verilog, simulated using Modelsim simulator and Lab VIEW and implemented using Xilinx FPGA device.

Index Terms- ***CIC Filter, Decimator, Interpolator, Multirate, Modelsim, Lab VIEW, FPGA.***

Introduction

The advent of larger and faster FPGA's has opened up new avenues in the field of digital signal processing. The large array of configurable logic blocks within the FPGA gives great hardware flexibility together with speed. Once configured, the FPGA as a system is not as flexible as a general purpose processor system but is much faster. For manyDSP applications speed is important, especially for the initial processing of the data, after which thedata rate reduces and becomes easier for processing.

In many applications, the signal of interest may not be at the optimum part of the spectrum for processing, for example in a communications system the signal band may be narrow, only KHz wide, but the signal band could be centered at RF frequencies, at many MHz. If the signal is sampled according to the Nyquist criteria, i.e. twice the highest frequency, then the data rate for the RF signal will be very high. Processing the data at this high rate is both difficult and expensive in terms of the amount of hardware required. Also, data transfer between two systems working at different rates requires rate change between them. The rate change process is done by using a decimator (for decreasing the rate) or interpolator (for increasing the rate) along with a filter.

In decimation or interpolation applications where the rate change factor is large (typically 8 or greater), an FIR filter implementation might be prohibitively costly due to the large number of filter taps that would be required. Cascaded Integrator Comb (CIC) filters are apt for anti-aliasing filtering prior to decimation and for anti-imaging filtering for interpolated signals. Both applications are associated with very high-data rate filtering. CIC filter is an optimized class of finite impulse response filters. First introduced by Hogenauer [1], CIC filters provide a very efficient means of implementing decimation and interpolation functions without using multipliers. This paper discusses the basics, architecture and implementation aspects of decimation and interpolation process using CIC filter and comparison between the results from Modelsim and Lab VIEW.

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CIS Filter Structure

Cascaded integrator–comb filters are multirate filters developed for creating large sample rate changes in digital systems. CIC filters consist of adders, subtractors and registers, and hence are multiplier void structures[2]. CIC filters originate from the standard moving averager which is a simple form of filter.

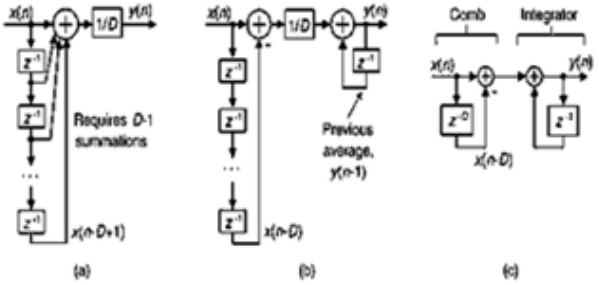

Fig.1 (a) Standard moving average filter (b) Recursive running sum filter
(c) CIC version of a D-point averaging filter

The time domain equation and the z-domain transfer function H(z) of a standard moving average filter depicted in Fig.1(a) is

$$y(n) = 1/D\,[x(n)+x(n-1)+x(n-2)+\ldots+x(n-D+1)]$$
$$H(z) = 1/D\,[1+z^{-1}+z^{-2}+\ldots+z^{-D+1}]$$

An equivalent, but more computationally efficient form of the moving averager is the recursive running sum filter depicted in Fig.1(b) which is a direct form 2 representation of standard moving averager, whose time domain equation and z-domain transfer function H(z) are

$$y(n) = 1/D\,[x(n) - x(n-D)] + y(n-1)$$
$$H(z) = 1/D\,(1-z^{-D})\,/\,(1-z^{-1})$$

The recursive running sum filter has an advantage that it requires only two additions per output sample.

The classic form of a first-order CIC filter is obtained by condensing the delay line representation and ignoring the 1/D scaling in Fig.1(b). The cascade structure is shown in Fig.1(c). The feed-forward portion of the CIC filter is called the comb section, whose differential delay is D, while the feedback section is typically called an integrator. The comb stage subtracts a delayed input sample from the current input sample, and the integrator is simply an accumulator to which the next sample is added at each sample period. The time domain equation and z-domain transfer function H (z) are

$$y(n) = [x(n) - x(n-D)] + y(n-1)$$
$$H(z) = (1-z^{-D})/(1-z^{-1})$$

Figure 2 shows the time domain impulse response of a single stage CIC filter. The positive impulse from the comb filter starts the integrator's all-ones output. Then D samples later the negative impulse from the comb filter arrives at the integrator to zero all further filter output samples. Although recursive, CIC filter has a finite impulse response.

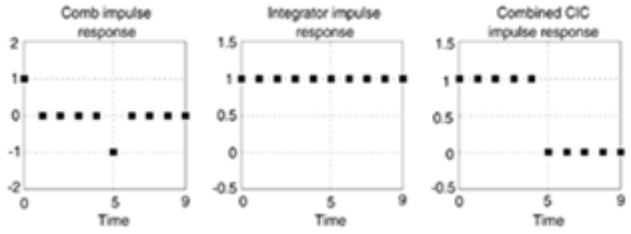

Fig.2 Single-stage CIC filter time-domain responses when D = 5

The magnitude and linear-phase response of a D = 5 CIC filter is shown in Fig.3 where the frequency axis is normalized to'fs', the input signal samplerate.

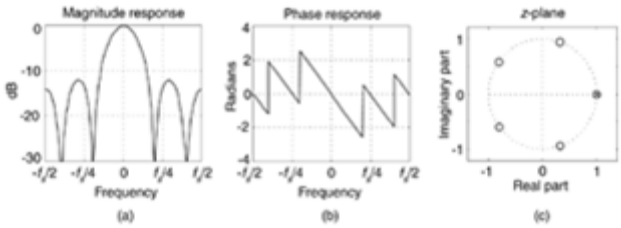

Fig.3 Characteristics of a single-stage CIC filter when D = 5. (a) Magnitude response (b) Phase response; (c) Pole/zero locations.

CIC filters are based on the fact that perfect pole/zero cancelling can be achieved. This is only possible with exact integer arithmetic. The z-plane pole/zero characteristics of a D=5 CIC filter are provided in Fig.3(c) where the comb filter produces D zeros, equally spaced around the unit-circle, and the integrator produces a single pole canceling the zero at z=1

The frequency response of a CIC filter can be obtained from the z-domain transfer function by setting $z=e^{j\omega}$ resulting in a sin(x)/x like lowpass filter centered at 0 Hz

$$H(e^{j\omega}) = (1-e^{j\omega D})\,/\,(1-e^{j\omega})$$
$$= e^{j\omega(D-1)/2}\,\sin(\omega D/2)\,/\,\sin(\omega/2)$$

The magnitude of $H_{cic}(e^{j\omega})$ at 0 Hz gives the DC gain of the CIC filter

$$|H_{cic}(e^{j\omega})|_{\omega=0} = |\sin(0)\,/\,\sin(0)| = 0/0$$

Using Marquis de L'Hospital's rule

$$|H_{cic}(e^{j\omega})|_{\omega=0} = (D/2)\cos(\omega D/2)\,/\,(1/2)\cos(\omega/2)$$

So,theDC gainofa CICfilter isequaltothecombfilter delay D[3].

CIC DECIMATOR

CIC filters are used for anti-aliasing filtering prior to decimation. Decimation is the process of reducing the sampling rate at the output of one system so a system

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operating at a lower sampling rate can input the signal. It consists of a digital anti-aliasing filter and a sample rate compressor. CIC decimator isobtained byswappingtheorder of the integrator and comb stages in the CIC filter structure and then including decimation bysample rate changefactor R.Itispermitted toswaptheorderofthecomband integrator sections because the operations are linear. Comb section must beon thesideofthefilter operating atthe lowersample rate toreduce thestorage requirements[4].

Fig.4 shows thestructureofa CIC decimator

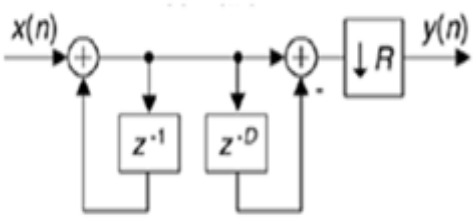

Fig.4 CIC Decimator

Thedecimation operation "!Rmeansdiscarding R-1 samples for every R samples of the filtered signal resulting in an output sample rate of fsout = fsin/R. To prevent aliasing at the lower rate, the digital filter is used tobandlimit theinput signal to lessthan fsin/2Rbeforehand [5].

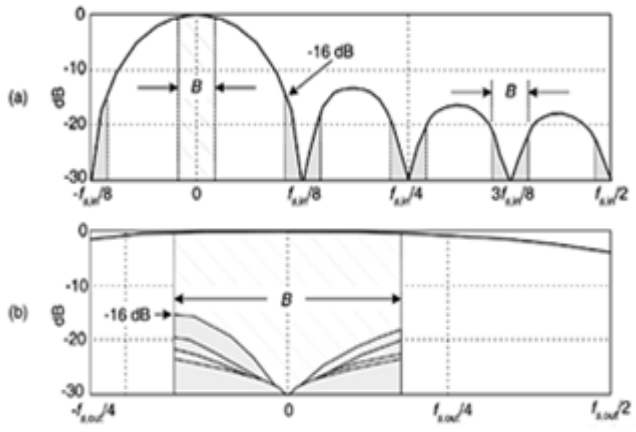

Fig.5 Frequency magnitude response of a first-order, D = 8, decimating CIC filter. (a) Response before decimation (b) Response and aliasing after R = 8 decimation

Fig.5(a) shows the frequency magnitude response of a D = 8 CIC filter prior to decimation. The spectral band, of width B, centered at 0 Hz is the desired pass-band of the filter. The B-width shaded spectral bands centered about multiples of fsin/R in Fig.5(a) will alias directly into our desired pass-band after decimation by R = 8, as shown in Fig.5(b). The largest aliased spectral component, in this example, is approximately 16 dB below the peak of the band of interest.

CIC INTERPOLATOR

CIC filters are used for anti-imaging filtering for interpolated signals. Interpolation is the process of upsampling followed by filtering[2]. Upsampling is the process of inserting zero-valued samples between original samples to increase the sampling rate.Upsampling createsin the original signal unwanted spectral images centered on multiples of the original sampling rate. The filtering removes theseundesired spectral images. In theCIC interpolator the comb section comes before the integrator. Fig.6 shows the structureofa CIC interpolator.

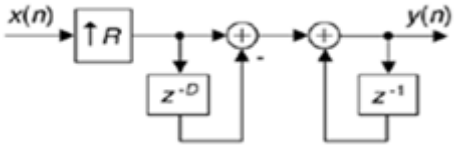

Fig.6 CIC Interpolator

Theinterpolation operation Rsymbol meansinserting (R-1) zeros between each x(n) sample, yielding a y(n) output sample rateoffsout = R*fsin.

Fig.7 Single Stage, D = R = 8, interpolating CIC filter spectra. (a) Input spectrum before interpolation (b) Output spectral images

After interpolation, unwanted images of the spectral bandwidth 'B' ofthebaseband spectrum reside near thenull centers, located at integer multiples of fsout/R as shown in Fig 7.(a). Theseimagesarerejected astheyresidein thestop band oftheCIC filter.

IMPROVING CIC ATTENUATION

TheCIC filter anti-aliasingand image-reject attenuation can be improved byincreasing the order M ofthe CIC filter using multiple stages. Fig.8 shows the structure and fre-quency magnitude response of a third-order (M = 3) CIC decimating filter. The combsection operatesat

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thelowsam-pling rate fsin/3. Thecombstageshavea differential delayof Dsamplesper stage. The differential delay controls the filter's frequency response. Since the 3 CIC stages are in cascade, the overall frequency magnitude response will be the prod-uct of their individual responses. Hence, the largest aliased spectral component here is approximately48 dB below the peak of the band of interest.

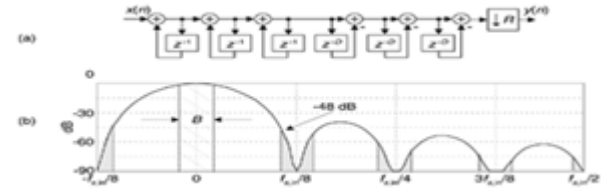

Fig.8 Third-order (M = 3), D = R = 8 CIC decimation filter. (a) Structure (b) Magnitude response before decimation

ANALYSIS FOR IMPLEMENTATION

In CIC filters, thecombsection canprecede,or follow, the integrator section. However, it is sensible to put the comb section on thesideofthe filter operating at the lower sample ratetoreducethestoragerequirements in thedelay. Henceit is better to use the structure as shown in Fig.9.

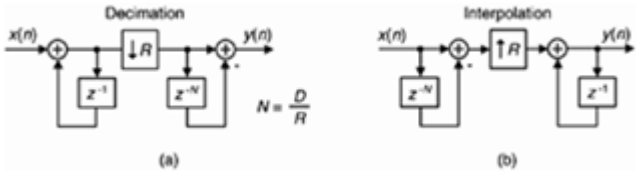

Fig.9 Single-stage CIC filters implementations: (a) For decimation (b) For interpolation

The comb section's new differential delayis decreased toN = D/R, reducing data storage requirements and the comb section now operates at a reduced clock rate. Both of these effects reduce hardware power consumption.

The DC gain ofan M stage CIC decimator is (NR)M and that of CIC interpolator is (NR)M/R. Hence there is a register growth phenomenon at the output. So the output bit width should be kept big enough so as to accommodate this growth[3].

The maximum output data width B_{max} of CIC decimator is

$$B_{max} = \log_2 (RN)^M + B$$

The maximum output data width B_{max} of CIC interpolator is

$$B_{max} = \log_2 (RN)^{M/R} + B$$

where B is the input data width.

Theother major issues with CIC are pass-band drooping and wide transition regions[6]. In typical decimation/ interpolation filtering applications, it is desired to have a reasonablyflat pass-band and narrowtransition region filter performance. This is achieved by using compensation and pre-conditioning FIR filters. The compensation FIR filter's frequencymagnitude responseisideallyan inverted version ofthe CIC filter pass-band response asshown in Fig.10. The compensated responsewill havea flat pass-band and narrow transition region. Compensation filters are used after CIC decimatorsand pre-conditioning filters areused before CIC interpolators as shown in Fig.11.

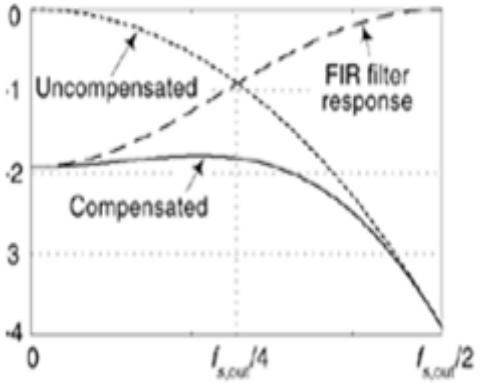

Fig.10 Compensation FIR filter magnitude Responses with a first-order decimation CIC filter

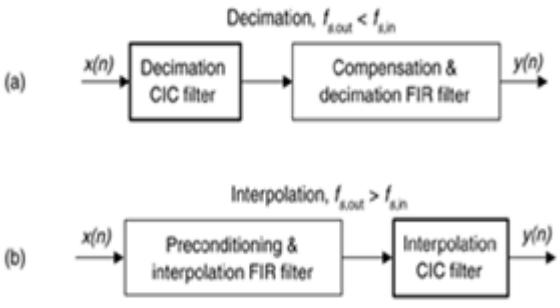

Fig.11 (a) decimation (b) interpolation

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Final results of CIC based DDC

The following two figures show the simulation results obtained for CIC based DDC. Detailed labels are written below each waveform.

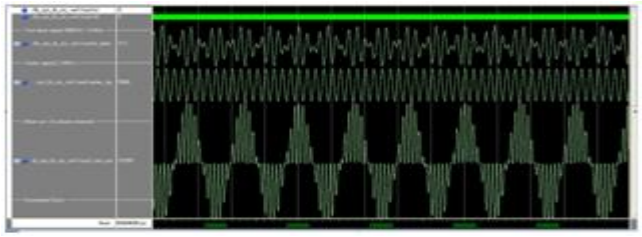

Fig. 12: DDS core and mixer outputs

In the above figure 12 the test input signal is a mixed signal with 300KHz and 2 MHz. This signal is obtained by multiplying two DDS's outputs. This is the first waveform (after rst and clk signals) in the above figure. The second waveform is 2 MHz carrier which is generated with another DDS. Next waveform is mixer output for in phase (I) channel.

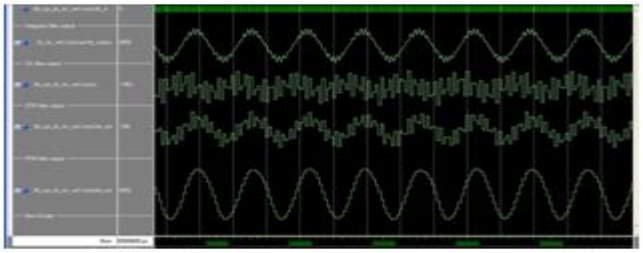

Fig. 13: CIC, CFIR and PFIR outputs

In the above figure 13 first the decimated clock is shown. This is decimated with a factor of 8. The second figure in above figure is the integrator stage output of CIC architecture. The next waveform is the complete CIC output. We can notice the CIC output is coming with decimated clock. Next in the figure compensating FIR filter (CFIR) output is shown. This becomes input to programmable FIR (PFIR) filter. The last waveform shows the output of PFIR filter. As expected the 300KHz base band signal with decimated clock is recovered.

CIC based DDC - Chipscope results

The CIC after porting on FPGA is tested with chipscope. Because of memory limitations on FPGA each stage output is not capture on chipscope. Only the input and output are connected to chipscope data port. The below figure 6.3 shows the test input signal for DDC which is 300KHz mixed with 2 MHz carrier. We can notice that the in_data check box is selected in the bus plot.

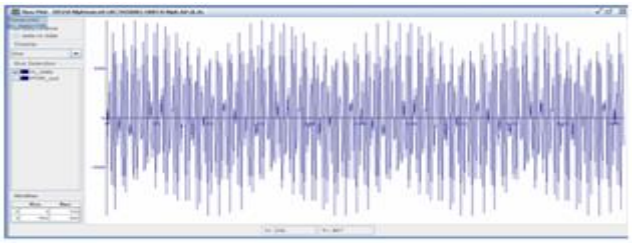

Fig. 14: Final input chipscope result

The below figure 14 shows the output of the DDC. Note that the PFIR_out check box is selected in the bus plot. It can be see that the output is 300 KHz sin wave.

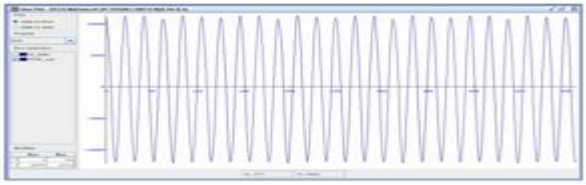

Fig. 15: Final output chipscope result

Synthesis of CIC based DDC

Table 1.2: Device utilization summary

Selected Device : XC3s500efg320-4			
Number of IOs : 50			
S.no	Logic utilization	Used	Utilization
1	Number of Slices	3986 out of 4656	87%
2	Number of Slice Flip Flops	2635 out of 9312	28%
3	Number of 4 input LUTs	5322 out of 9312	57%
4	Number of bonded IOBs	26 out of 232	11%
5	Number of MULT18X18SIOs	9 out of 20	45%
6	Number of GCLKs	3 out of 24	12%
7	Number of DCMs	1 out of 4	25%

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Table 1.3: Timing summary

Speed grade : -4	
1	Minimum period :16.196ns(Maximum Frequency:61.744MHz)
2	Minimum Input Arrival time before clock: No path found
3	Maximum output required time after clock:7.245ns
4	Maximum combinational path delay:4.733ns

Inference of CIC based DDC

A decimating CIC filter is merely a very efficient recursive implementation of a moving average filter, with NR taps, whose output is decimated by R. Likewise, the interpolating CIC filter is insertion of R-1 zero samples between each input sample followed by an NR tap moving average filter running at the output sample rate fs,out. The cascade implementations result in total computational workloads far less than using a single FIR filter alone for high sample rate change decimation and interpolation. CIC filter structures are designed to maximize the amount of low sample rate processing to minimize power consumption in high-speed hardware applications. Again, CIC filters require no multiplications; their arithmetic is strictly additions and subtractions. Their performance allows us to state that, technically speaking, CIC filters are lean, mean filtering machines.

The simulation results of CIC based DDC conclude that a input of 300kHz and 2MHz which is generated from DDS ip core is mixed and given to CIC decimation filter, the input signal is down converted by a factor 8with respect to the decimation clock and the output of CIC filter as pass band droop. So the output of the CIC filter is fed to compensation FIR filter (CFIR) and then fed to programmable FIR filter (PFIR) which reduces the transition band. The CFIR and PFIR filters are designed in MATLAB FDA tool, which generates the filter coefficients. These filter coefficients are used in VHDL package (user defined package) and the package is used in the project.

CONCLUSION

The CIC filter structure is analyzed and is used in the design and implementation ofdecimator and interpolator.A rate change of32 is taken and 3 stage and 4 stage filters are analyzed. The number of stages and rate factor are made programmable and thecircuit isreconfigurable for different hardwareparameters. Thedesignsaresimulated and verified between Modelsim simulator and Lab VIEW. The device utilization summary for decimator and interpolator with different stages are implemented in Xilinx Spartan 3 FPGA and verifiedin hardware.

ACKNOWLEDGEMENT

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