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Simulation of loopback virtual channel router

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Abstract: ***Network on chip or network on a chip (NoC or NOC) is a communication subsystem on an integrated circuit (commonly called a "chip"), typically between intellectual property (IP) cores in a system on a chip (SoC). NoCs can span synchronous and asynchronous clock domains or use unclocked asynchronous logic. NoC technology applies networking theory and methods to on-chip communication and brings notable improvements over conventional bus and crossbar interconnections. NoC improves the scalability of SoCs, and the power efficiency of complex SoCs compared to other designs. In his paper we attempt to give a networking solution by applying VLSI architecture techniques to router design for networking systems to provide intelligent control over the network. Networking routers today have limited input/output configurations, which we attempt to overcome by adopting bridging loops to reduce the latency and security concerns. Other techniques we explore include the use of multiple protocols. We attempt to overcome the security and latency issues with protocol switching technique embedded in the router engine itself.***

The approach is based on hardware coding to reduce the impact of latency issues as the hardware itself is designed according to the need. We attempt to provide a multipurpose networking router by means of Verilog code, thus we can maintain the same switching speed with more security as we embed the packet storage buffer on chip and generate the code as a self-independent VLSI Based router. Our main focus is the implementation of hardware IP router. The approach enables the router to process multiple incoming IP packets with different versions of protocols simultaneously, e.g. for IPv4 and IPv6. The approach will results in increased switching speed of routing per packet for both current trend protocols, which we believe would result in considerable enhancement in networking systems.

Keywords: ***NoC, Router, System On Chip, Latency, Performance, Simulation.***

Introduction:

Multiprocessor system on chip is emerging as a new trend for System on chip design but the wire and power design constraints are forcing adoption of new design methodologies. Researchers pursued a scalable solution to this problem i.e. Network on Chip (NOC). Network on chip architecture better supports the integration of SOC consists of on chip packet switched network. Thus the idea is borrowed from large scale multiprocessors and wide area network domain and envisions on chip routers based network. Cores access the network by means of proper interfaces and have their packets forwarded to destination through multichip routing path. In order to implement a competitive NOC architecture, the router should be efficiently design as it is the central component of NOC architecture. In this paper we implement a parallel router which can support five requests simultaneously. Thus the speed of communication can be increased after reducing communication bottleneck by using simplest routing mechanism, flow mechanism and decoding logic.

In this paper we attempt to give a networking solution by applying VLSI architecture techniques to router design for networking systems to provide intelligent control over the network. Networking routers today have limited input/output configurations, which we

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attempt to overcome by adopting bridging loops to reduce the latency and security concerns. Other techniques we explore include the use of multiple protocols. We attempt to overcome the security and latency issues with protocol switching technique embedded in the router engine itself.

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A system on a chip or system on chip (SoC or SOC) is an integrated circuit (IC) that integrates all components of a computer or other electronic system into a single chip. It may contain digital, analog, mixed-signal, and often radio-frequency functions—all on a single chip substrate. SoCs are very common in the mobile electronics market because of their low power consumption. A typical application is in the area of embedded systems.

A SoC consists of both the hardware, described above, and the software controlling the microcontroller, microprocessor or DSP cores, peripherals and interfaces. The design flow for a SoC aims to develop this hardware and software in parallel. Most SoCs are developed from pre-qualified hardware blocks for the hardware elements described above, together with the software drivers that control their operation. Of particular importance are the protocol stacks that drive industry-standard interfaces like USB. The hardware blocks are put together using CAD tools; the software modules are integrated using a software-development environment. Chips are verified for logical correctness before being sent to foundry. This process is called functional verification and it accounts for a significant portion of the time and energy expended in the chip design life cycle. With the growing complexity of chips, hardware verification languages like SystemVerilog, SystemC, e, and OpenVera are being used. Bugs found in the verification stage are reported to the designer.

Existing System

Several asynchronous NoC solutions have been proposed recently. the NoCs provide high-throughput on-chip communication for specific topologies, such as cross bar and a mesh-of-trees. Especially, it is designed based on 2-phase channel communication and 2-phase router based on mouse-trap in a bundled-data logic style. General-purpose routers are designed based on a four-phase bundled-data logic style and support quality-of-service guarantees These routers are designed simply because of the use of the bundled-data logic style; however they are weak against timing variations. NOCs are also designed based on four-phase encoding. This provides timing robustness for highly reliable NOC systems because of the QDI logic style. How ever, these approaches lower the throughput because of the large number of communication steps.

Proposed System

The overall structure of the proposed asynchronous NOC router, which consists of five Input Units and five Output Units. The Input Unit includes two stage Pipe latches (PLs), Shifter (SH), and Routing controller(RC). The Output Unit includes two-stage PLs, Arbitration Controller (AC), and Multiplexer (MX). Each Input Unit is connected to other four Output Units except its corresponding Output Unit. This router has five input and output ports. Flits are transmitted from one port to one of other ports. Every signal is a 2-phase signal except sel signals for PLs. Initially, the first- and the last-stage PLs are transparent

Router:

A router is a device that forwards data packets across computer networks. Routers perform the data "traffic direction" functions on the Internet. A router is a microprocessor-controlled device that is connected to two or more data lines from different networks. When a data packet comes in on one of the lines.the router

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reads the address information in the packet to determine its ultimate destination. Then, using information in its routing table, it directs the packet to the next network on its journey.

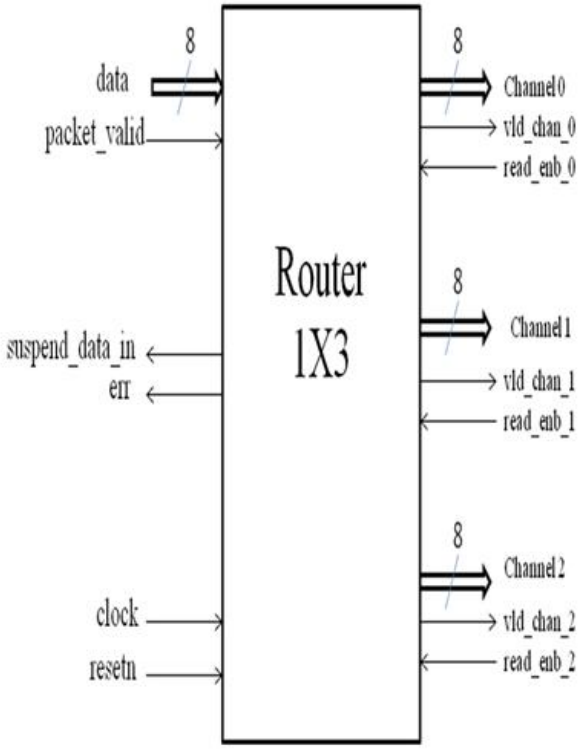

Fig Block Diagram Of Router_1X3

The router is a " **Four Port Network Router**" has a one input port from which the packet enters. It has three output ports where the packet is driven out. Packet contains 3 parts. They are Header, data and frame check sequence. Packet width is 8 bits and the length of the packet can be between 1 bytes to 63 bytes. Packet header contains three fields DAand length.Destination address(DA) of the packet is of 8 bits. The switch drives the packet to respective ports based on this destination address of the packets. Each output port has 8-bit unique port address. If the destination address of the packet matches the port address, then switch drives the packet to the output port, Length of the data is of 8 bits and from 0 to 63. Length is measured in terms of bytes. Data should be in terms of bytes and can take anything.

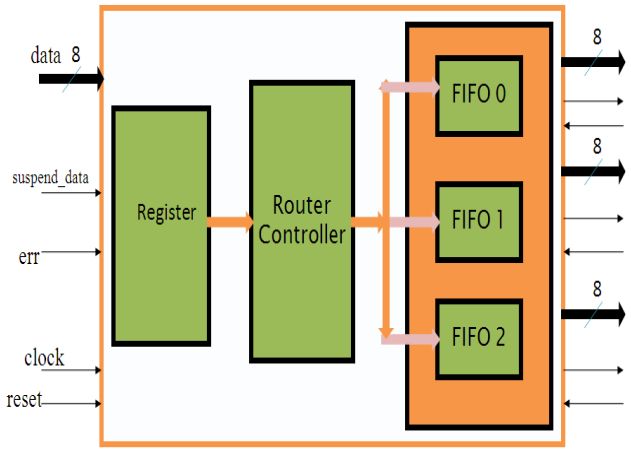

Figure : Four Port Router Architecture

Environment

The environment (env) is the top-level component of the SVC. It contains one or more agents, as well as other components such as a bus monitor. The env contains configuration properties that enable you to customize the topology and behavior and make it reusable. For example, active agents can be changed into passive agents when the verification environment is reused in system verification.

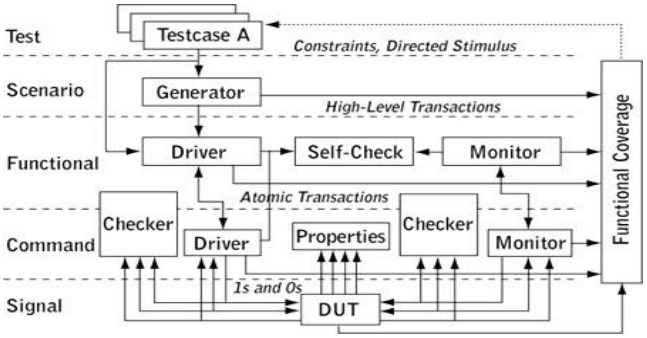

Figure : Typical SVC Environment

Verification Plan:

The Verification Plan is the focal point for defining exactly what needs to be tested, and drives the coverage criteria. Success of a verification project relies heavily on the completeness and accurate implementation of a verification plan. A good plan contains detailed goals using measurable metrics, along with optimal resource usage and realistic schedule estimates. Verification plan gives an opportunity to present and review the strategy for

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functional verification before the verification engineer have gone into detail to implement it. It also establishes proper communication.

How to Verify?

After defining what exactly need to be verified, define how to verify them.

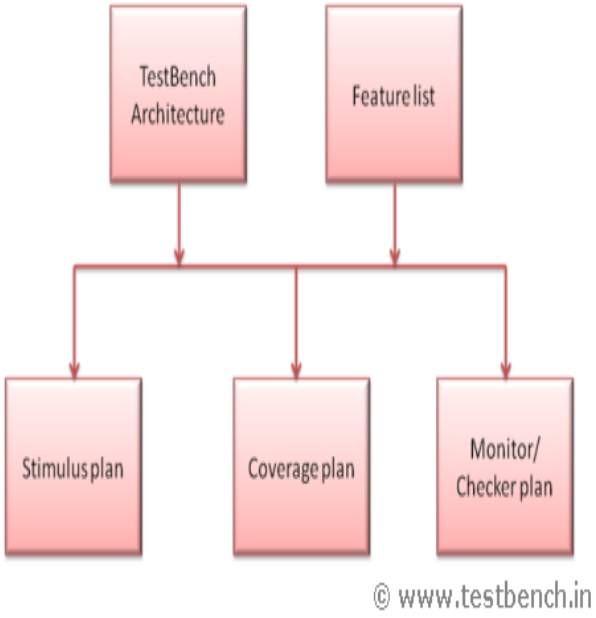

Figure : Complete Verification Plan of Test Bench Environment

Components Required For The Test Bench

There are six components in the test bench. They are listed below

- Driver Interface
- Receiver Interface
- Monitor
- 3 Mail Boxes

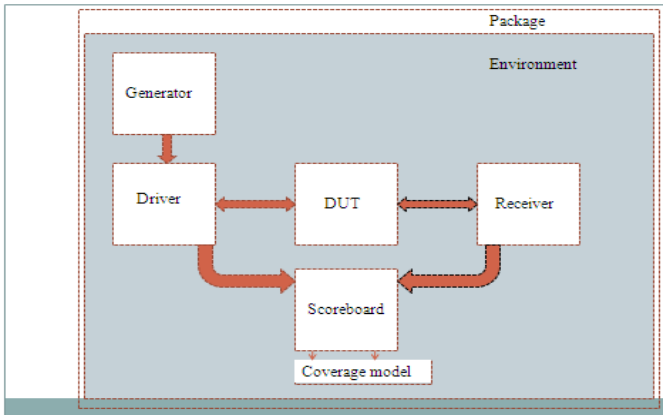

Fig: Test bench ENVIRONMENT

Simulation Results

The below figures shows the simulation results of test cases applied to the DUT . figure 10.4 shows the response of the device for the control test case at the usb interface. Figure below shows the master transmitter sending random data to the external slave device.

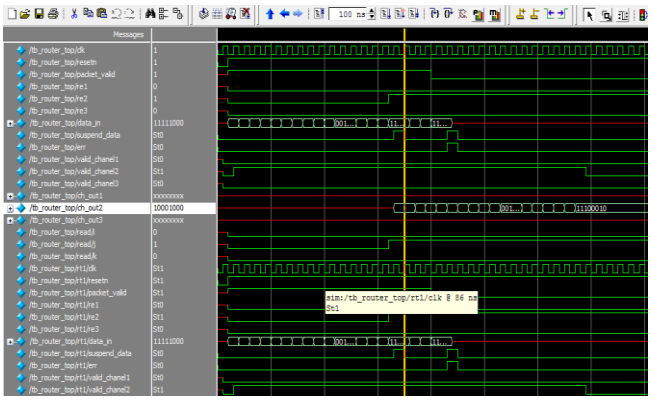

Fig: Simulation results of Four Port Router for Noc.

Data_in[1:7] = input =deferent data packets
Data_in[0] = 11111001

Output : Ch_out1 = 8'bXXXXXXXX
Ch_out2 = data_in,
Ch_out3 = 8'bXXXXXXXX.

After **80ns** again applying inputs immediately output obtained, because of no delay elements.

Data_in[1:7] = input =deferent data packets
Data_in[0] = 11111000

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Output : Ch_out2 = 8'bXXXXXXXX, Ch_out1 = data_in, Ch_out3 = 8'bXXXXXXXX.

RTL Designs:

RTL is generated when code is synthesized that is when gate level net list.

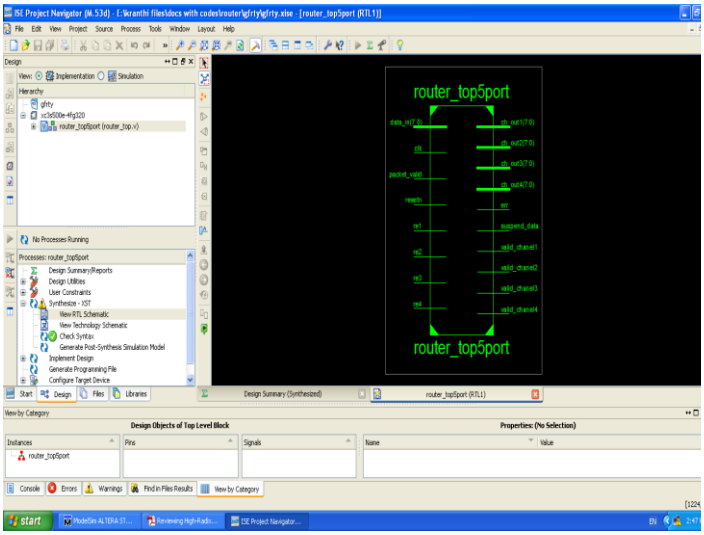

Fig: Schematic of top level RTL

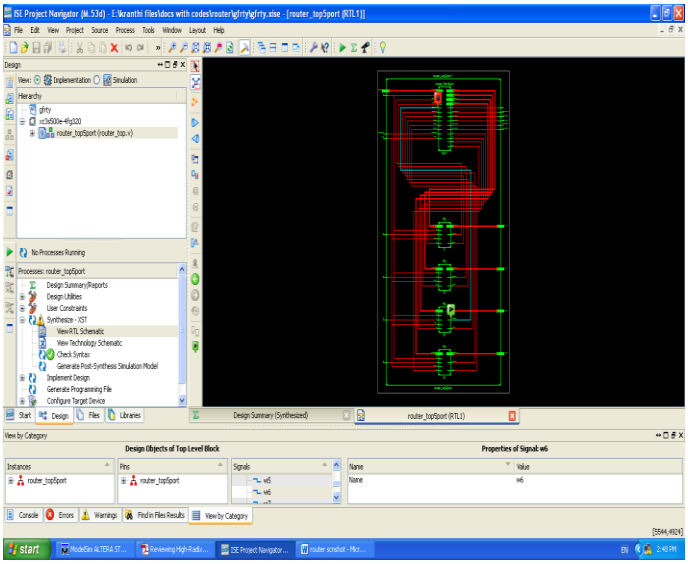

Fig: Internal diagram of RTL diagram.

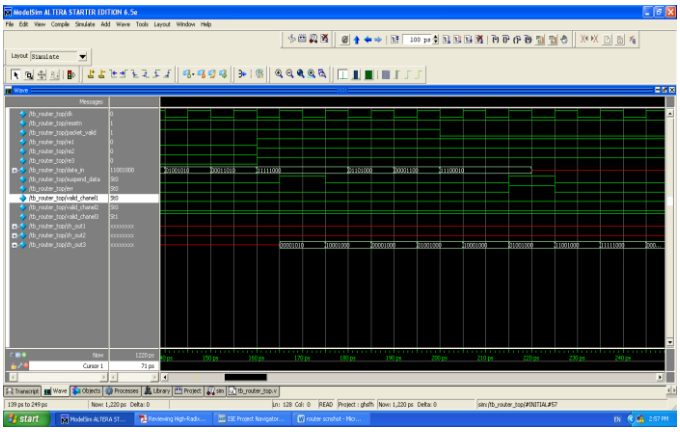

Fig: Simulation Result for top level

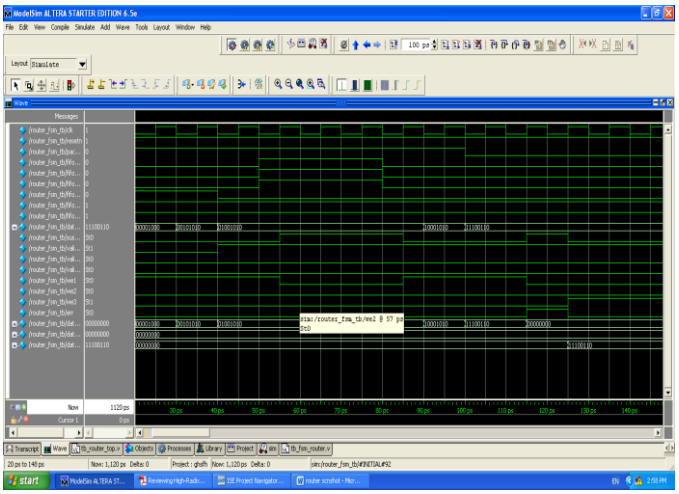

Fig: Simulation Result for FSM

Synthesis Results

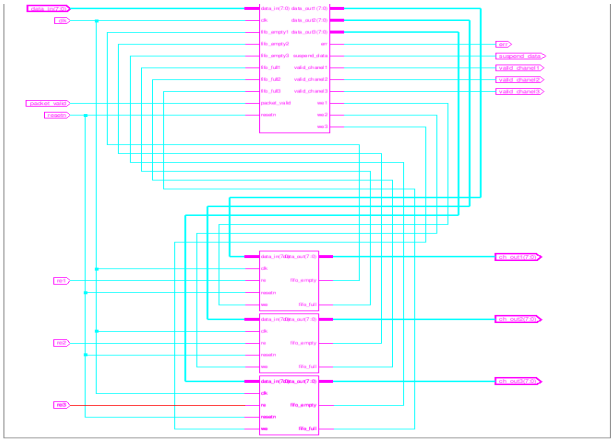

Fig: Synthesis results of Four Port Router for Noc.

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Advantages:

1. Router limits the collision domain.

2. Router can function on LAN & WAN

3. Router can connects different media & architectures.

4. It can determine best path/route for data to reach the destination.

5. Router can filter the broadcasts.

Applicaltions:

1. Router provides connectivity within enterprises, between enterprises and the internet.

2 . Large routers such as Cisco CRS-1 or Juniper T1600 interconnects various ISP's.

Conclusion

As the functional verification decides the quality of the silicon, we spend 60% of the design cycle time only for the verification/simulation. In order to avoid the delay and meet the TTM, we use the latest verification methodologies and technologies and accelerate the verification process. This project helps one to understand the complete functional verification process of complex ASICs an SOC's and it gives opportunity to try the latest verification methodologies, programming concepts like Object Oriented Programming of Hardware Verification Languages and sophisticated EDA tools, for the high quality verification.

In this Four Port Router project I Design and verified the functionality of Router with the latest Verification methodology i.e.,System Verilog and observed the code coverage and functional coverage of Router by using cover points ,cross and different test cases like constrained, weighted and directed testcases.By using these testcases I improved the functional coverage of Router. In this I used one master and eight slaves to monitor the Router.Thus the functional coverage of Router was improved.

The results shows that System Verilog methodology can be used to make reusable test benches successfully. Large part of the test bench is made reusable over multiple projects.even though this reusablity is limited to the interfaces. A large class of devices that are build on these inerfaces can be verified successfully. Once these components are made the amount of time required to build test benches for other projects can be reduced a lot.

Future Scope

This project used System verilog i.e., the technology used is direct testcases, randomized testcases ,OVM for verification even though the coverage is 100% there may be some errors which cannot be shown so inoder to overcome this the new technology of System verilog i.e.,OVM and UVM.In the coming future the Router can be done by using OVM and UVM.

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