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Design and Analysis of Four-Bit Non Interleaved Data Converter Pair for Advanced Serial Links in VDSM Technology

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Abstract:

This paper presents the look and check of a fourteen GSps, four-bit convertor combine in ninety nm CMOS appropriate for implementing advanced serial links. the information convertor combine consists of a non-interleaved flash analog-digital converter (ADC) and a noninterleaved current-steering digital-analog converter (DAC). each the convertor styles adopt the wave pipelining technique to extend the on the market signal subsiding time. Through elaborated analysis, we have a tendency to show that cascading 3 active feedback preamplifiers to implement the cores of the comparators within the ADC balances the facility budget and also the style issue after we push the rate to the method limit. Current mode logic gates square measure accustomed alleviate the facility bouncing issue. to handle the problem and high price of testing the very high-speed converters, {the style|theplanning|the look} embeds the easy design for- checkability circuits cooperating with the on-chip resources to produce 2 cost-efficient test modes. the primary check mode cascades the ADC and DAC so they will be tested at the rated speed while not the requirement of a awfully high speed logic analyzer.

The second check mode permits the attention diagram tests by shuffling the digital outputs of ADC because the inputs of the DAC rather than adopting typical linear feedback register. The experimental results show that the cascaded ADC and DAC combine achieves a thirty one.0dBc spurious-free dynamic vary and a twenty five.9 dB signal-to noise- and-distortion quantitative relation with a one.11 GHz, −1 dBFS input at 14GSps. The ADC and DAC consume 214mW and 85mW from a one.0-V provide and occupy zero.1575 mm2 and zero.0636 mm2, severally.

Index Terms: Analog-to-digital converter (ADC), design-fortestability,digital loopback, digital-to-analog converter (DAC),eye diagram test, high-speed.

I. INTRODUCTION:

Serial links become the most stream of contemporary wired or wireless communication systems as a result of their price effectiveness and power potency [1]. business product like PCI-Express and Serial ATA accommodate information rates over Gb/s. The IEEE normal 802.3ba-2010 any defines forty Gb/s and one hundred Gb/s local area network [2]. no doubt, the endless demands for quicker and quicker communication and therefore the unceasingly advancing technology push the info rates of future serial links on top of ever.Two elementary factors would limit the improvement of the info rate: the intrinsic information measure of the transmission medium and inevitable noise. in line with the Shannon– David Hartley theorem, associate degree error-correction cryptography theme that gives a data rate of C bits per second through a such as channel exits. Mathematically, C may be expressed as

$$C = BW\log2(1 + SNR) \quad (1)$$

where BW is that the information measure of the channel in hertz, and therefore the SNR represents the S/N (SNR) of the communication signal to the mathematician noise interference. Given constant SNR, (1) indicates that the sole thanks to increase the data rate is to extend BW. However, it's sometimes terribly expensive to possess a channel with a wider information measure, regardless of it's wired or wireless. An alternative to extend the data rate is to extend the SNR.

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during a panel of consultants at the International Solid State Circuits Conference (ISSCC) 2009, serializer/de-serializer (SerDes) chip designers argued that analog-to-digital converters (ADCs) combined with construction cryptography techniquesenable lower price styles, following the roaring pattern set by the digital connective and voice-band modems years ago[3].High-speed ADCs and digital-to-analog converters (DACs) with moderate resolution area unit the key enablers of the higher than idea:

Enhancing the SNR term in (1) notwithstanding the channel information measure therefore on increase the general data rate [4], [5].Several progressive styles have incontestable seriallink transceivers that accomplish information rates over five Gb/s [6]–[8]. Most of them use the interleaved ADCs and DACs as their building blocks. Such styles relax the speed demand of individual convertor, however need additional advanced and correct temporal order and additional areas.

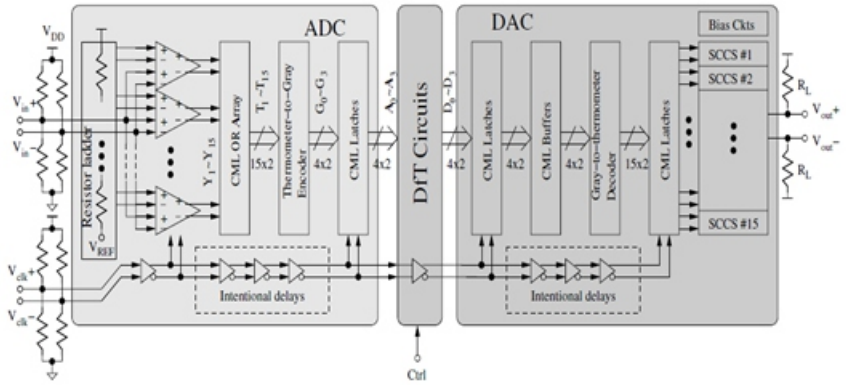

Fig.1: Block diagram of the test chip.

This paper demonstrates the look and check of a fourteen GSps, four-bit ADC and DAC try while not interleaving for the look of advanced serial-link transceivers. to handle the problem and high value of conducting at-speed tests and eye diagram tests of those very quick converters, we tend to conjointly propose a coffee value design-for-test-ability (DfT) theme. The reminder of this paper is organized as follows. Section II describes the elaborate circuit styles of the ADC and DAC. Section III depicts the DfT theme and circuits. measuring results area unit illustrated in Section IV. Finally, Section V attracts our conclusions.

II. CIRCUIT DESIGN:

Fig. one depicts the diagram of our style. It consists of the four-bit flash ADC, the four-bit current-steering DAC, and also the DfT circuits. All circuits as well as the digital circuits square measure realized victimization absolutely differential structures to alleviate the common-mode interference and noise. The differential input vary of the ADC and also the differential output vary of the DAC square measure set to four hundred mV. It corresponds to associate LSB of fifty mV. we tend to use the grey codes to represent the first outputs of the ADC and also the primary inputs of the DAC.

Adopting the grey codes advantages from that a single-bit error induces reduced error to a grey code than to a code. the rationale is 2 consecutive grey codes continually disagree from one another at the most by one bit. Hence, a single-bit error presumably results in associate LSB distinction.

A. Analog-to-Digital Converter:

The ADC may be a noninterleaved flash ADC while not a preceding sampled-and-hold (S/H) stage almost like that in [9]. the first inputs of ADC directly connect with 2 electrical device dividers which offer 50-ohm terminations and bias the inputs of the ADC core at the required voltage. The ADC core consists of fifteen comparators that convert the analog inputs to the corresponding thermometer-coded outputs. the subsequent logic OR array eliminates the single-bubble errors of the thermometer-coded outputs. Finally, the thermometerto- grey encoder encodes the outputs of the OR array and produces the four-bit Gray-code outputs.1) style of the Comparator: every of the comparator compares the differential primary input with the corresponding differential reference voltage and produces a digital little bit of the measuring system code. the most style goal of the comparator is to realize the desired gain ACP and information measure

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BWCP with the smallest amount power. within the worst case, the comparator should resolve a distinction but one LSB at intervals a [*fr1] clock cycle that is <36 annotation. A conservative style constraint of the comparator is that a 1/√2 LSB input is amplified to a complete digital signal. an extra conservative style constraint asks the comparator for a information measure as wide because the Nyquist information measure of the ADC. For this ADC style, the look targets area unit ACP = twenty seven sound unit and BWCP = seven gigacycle. Realizing the comparator by an easy single-stage differential electronic equipment requests the electronic equipment to realize a gain-bandwidth product (GBWP) >158 gigacycle. Such a style isn't sensible as a result of the last word GBWP is already round the intrinsic unit-gain frequency of the MOSFET. though the MOSFET were quick enough, the single-stage style consumes an excessive amount of power. Cascading many identical preamplifiers (Pre Amps) may be a low power different [10], [11].Let the comparator be enforced by cascading N identical PreAmps and each PreAmp incorporates a information measure of BWPA, a dc gain of APA, and a first- or second-order transfer operate. especially, the second-order transfer operate is assumed to own a maximally flat frequency response. Then, the ith-order PreAmp style ought to follow [10]

$$BW_{PA} = \frac{BW_{CP}}{\sqrt[2^i]{\sqrt[N]{2}-1}}$$
$$A_{PA} = \sqrt[N]{A_{CP}} \qquad (2)$$

and its GBWP equals to

$$\frac{BW_{CP}\sqrt[N]{A_{CP}}}{\sqrt[2^i]{\sqrt[N]{2}-1}} \qquad (3)$$

We adopted the differential electronic equipment with active feedback to implement the second-order PreAmp [10]. Fig. two shows the schematic. The active feedback configuration extends the information measure of the PreAmp as our want. The transfer perform of the active feedback PreAmp is shown [10] to be

$$\frac{V_o}{V_{in}} = \frac{A_{PA}\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \qquad (4)$$

where

$$A_{PA} = \frac{g_{m1}g_{m2}R_{L1}R_{L2}}{1 + g_{m2}g_{mf}R_{L1}R_{L2}}$$
$$\zeta = \frac{R_{L1}C_{L1} + R_{L2}C_{L2}}{2\sqrt{R_{L1}C_{L1}R_{L2}C_{L2}(1 + g_{m2}g_{mf}R_{L1}R_{L2})}}$$
$$\omega_n = \sqrt{\frac{1 + g_{m2}g_{mf}R_{L1}R_{L2}}{R_{L1}C_{L1}R_{L2}C_{L2}}}. \qquad (5)$$

By designating $g_{m1} \approx g_{m2} = g_m$, $R_{L1} \approx R_{L2} = R_L$, $C_{L1} \approx C_{L2} = C_L$, and $\zeta = 1/\sqrt{2}$, the active feedback Pre Amphasthe following design parameters:

$$A_{PA} = \left(\frac{g_m R_L}{2}\right) g_m R_L$$
$$BW_{PA} = \left(\sqrt{2}\right) \frac{1}{2\pi R_L C_L} \qquad (6)$$

where g RL and 1/(2π RLCL) are often thought to be the gain and information measure of a first-order PreAmp, severally.Equation (6) explains the most important good thing about adopting the active feedback PreAmp, particularly once we wish to attain the last word sampling rate: the information measure is boosted by an element of √2 comparison that of a first-order PreAmp. it's as a result of the required gain will continually be achieved by cascading a lot of stages whereas the information measure wouldn't. Besides, the desired GBWP of the first-order Preamp is on top of that of the second order PreAmp in step with Fig. 2. It makes the PreAmp style a lot of tough due to the method limitation.

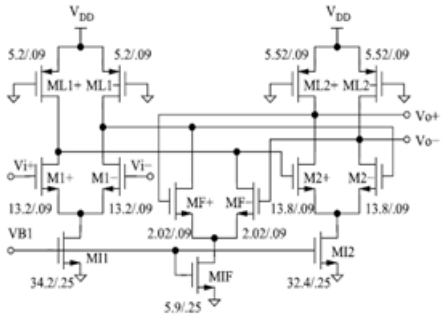

Fig.2: Schematic of the second-order PreAmp with active feedback [10].

To sum up, the active feedback technique is beneficial once attempting to push the comparator's speed to the limit.Another style target folks is to stay an honest energy potency. consistent with Fig. 2, the a lot of the cascaded second order PreAmps, the smaller is that the GBWP that the PreAmp needs. though a PreAmp with a smaller GBWP consumesless power, however, the full power of the cascaded chain is proportional to the stage variety of the PreAmps.

Consequently, there exists Associate in Nursing optimum stage variety. In our style, the active feedback PreAmp entirely consumes concerning double the bias current of the key current supply (MI1) in it. Hence, the full power of the comparator is expressed as

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$$P_{CP}(N) \simeq V_{DD}N(4I_{DS,M1}) = \frac{2V_{DD}}{\beta_n}Ng_m^2 \quad (7)$$

Where $\beta_n = \mu_n C_{ox} W/L$ is the process transconductance Parameter. Given the specified C_L and BW_{CP}, we have

$$P_{CP}(N) = \left(\frac{8\pi^2 V_{DD} C_L^2 BW_{CP}^2}{\beta_n}\right)\frac{N\sqrt[N]{A_{CP}}}{\sqrt{\sqrt[N]{2}-1}} \quad (8)$$

according to (2), (5), and (6).

Fig. three shows the diagram of the ultimate comparator style. The comparator may be a cascade of a differential distinction electronic equipment (DDA), same 3 second-order PreAmp stages, and a current mode logic (CML) latch.

The DDA isn't counted as a PreAmp stage as a result of its selected gain is near unity and its information measure is way on top of the specification of the comparator.Fig. four shows the schematic of DDA. It generates the amplified distinction of the first differential input and also the corresponding differential reference voltage [12]. Note that the DDA style pairs the positive input and also the positive reference rather than the negative input. Such a rendezvous eliminates the planning problem of keeping the differential try functioning with a differential reference input as high as 800 mV.2) Design of the Digital Blocks: Making the logic functions quick and quiet ar another style challenges. Customary CMOS logic gates generate vital switch noise on the facility rails. They conjointly consume goodish power once operative at

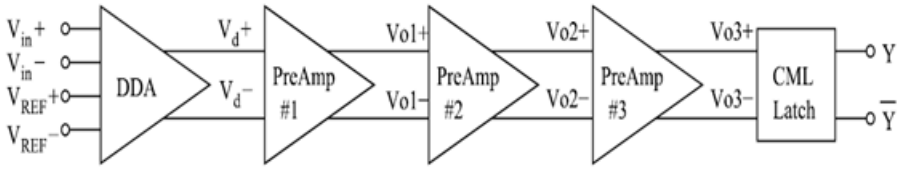

Fig.3: Block diagram of the proposed comparator

14 gigacycle thanks to their rail-to-rail input/output (I/O) swings. to handle these problems, all digital circuits are enforced with the CML family projected in [13].

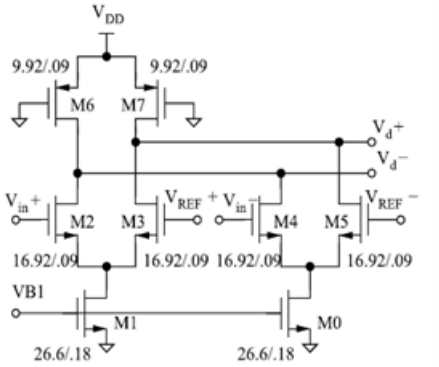

Fig.4: Schematic of DDA.

Fig. five shows some CML gates utilized in our style. The CML gates deliver the goods quicker logic shift as a result of alittle input voltage distinction is adequate to totally switch the currents of the differential try. Besides, the constant tail current sources of the CML gates alleviate severe power bouncing. The CML gates additionally consume less power than their CMOS counterparts once operate at fourteen gigacycle per second as a result of the I/O swings of the CML gates don't seem to be rail-to-rail. The I/O swings of the CML gates area unit designed to be an equivalent because the all-out I/O swings of the ADC and DAC.

Even with the CML circuits, the essential delay of the ADC's logic half remains too long for 14-GHz operation. therefore we have a tendency to apply the wave-pipelining technique [14] to handle this issue.

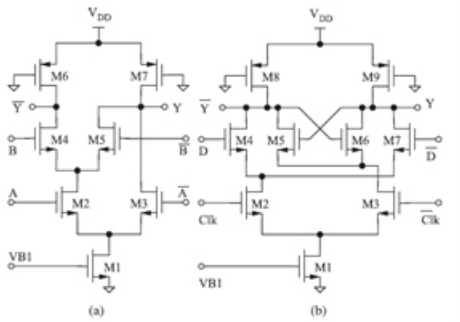

Fig.5: CML gates [13]. (a) AND/NAND/OR/NOR. (b) Latch.

As shown in Fig. 1, intentional clock buffers area unit inserted to the clock methods to make amends for the delay time of the signal methods to achieve some further temporal arrangement margins.

B. Digital-to-Analog Converter:

The DAC includes a Gray-to-thermometer decoder followed by the switched current supply array. every switched current supply is enforced mistreatment the switched

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cascode current supply (SCCS) configuration owing to the next output resistivity and a far better spurious free dynamic vary (SFDR) [15]. CML latches ar inserted between the decoder's outputs and each SCCS cell to confirm that every one SCCS cells ar at the same time switched.Similar to the ADC style, the DAC additionally suffers from a really short amount for its logic components. a similar wave-pipelining technique by adding some intentional delays on the clock methods is additionally wont to atone for the essential delay of the DAC's logic half.

III SIMULATION RESULTS:

The simulation of the projected style is meted out in Hspice tool. The simulated results and performance comparison table square measure shown in below figures:

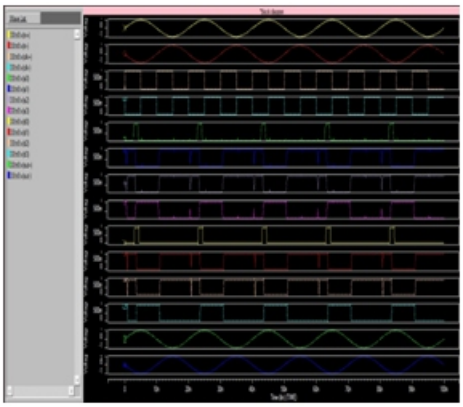

Fig.6: Simulation results of proposed block diagram

Table 1: Performance Comparison table

Circuit	Avg Power (W)	Delay (sec)	FOM (J/bit)
Comparator	0.018	2064p	0.047
Encoder	0.02m	33.9p	0.00067p
ADC	0.333	10.37p	3.453n
DFT	0.0124m	149.8p	0.00185p
Decoder	0.0294m	105.69p	0.0031p
DAC	3.159m	2.16n	6.823p
Final results	0.30	1.94p	0.646p

IV. CONCLUSION:

A fourteen GSps four-bit ADC and DAC combine in 90-nm CMOS for the planning of advanced serial-link transceivers was given. The active feedback amplifiers, CML, and wave pipelining technique were applied to alleviate the severe power bouncing and to realize the last word fourteen GSps rate. The DfT circuits used the digital loop-back theme to alter the at-speed measurements within the cascade mode. we have a tendency to noticed that compensating the measured output spectra for the S/H effects within the cascade mode improved the measure accuracy. By shuffling the association order of the digital loop-back within the different shuffled mode, the attention diagrams were additionally tested. The experimental results showed that the cascaded ADC and DAC combine achieved a twenty five.9 sound unit SNDR and a thirty one.0dBc SFDR with the one.11 Gc stimulation, and consumed 323mW from a one.0 V supply.

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