ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Solar PV and Battery Storage Integration using a New Configuration of a Five-level NPC Inverter

K.Nooka Raju, (M.E)
Assistant Professor,
Department of Electrical & Electronics Engineering,
Lords Institute of Engineering &Technology;
Rangareddy (Dt); Telangana, India.

B.Sridevi
M.Tech Student Scholar,
Department of Electrical & Electronics Engineering,
Lords Institute of Engineering &Technology;
Rangareddy (Dt); Telangana, India.

Abstract:

In this paper, a novel configuration of a five-level neutral-point-clamped (NPC) inverter that can integrate solar photo voltaic (PV) with battery storage in a grid-connected system is proposed. The strength of the proposed topology lies in a novel, extended unbalance five-level vector modulation technique that can generate the correct ac voltage under unbalanced dc voltage conditions. This paper presents the design philosophy of the proposed configuration and the theoretical framework of the proposed modulation technique. A new control algorithm for the proposed system is also presented in order to control the power delivery between the solar PV, battery, and grid, which simultaneously pro-vides maximum power point tracking (MPPT) operation for the solar PV. The effectiveness of the proposed methodology is investigated by the simulation of several scenarios, and THD is calculated for both levels including battery charging and discharging with different levels of solar irradiation.

Index Terms:

Battery storage, solar photovoltaic (PV), space vector modulation (SVM), three-level inverter, and five-level inverter, maximum power point tracking (MPPT).

I. INTRODUCTION:

Due to the world energy crisis and environmental problems caused by conventional power generation, renewable energy sources such as photovoltaic (PV) and wind generation systems are becoming more promising alternatives to replace conventional generation units for electricity generation [1], [2]. Advanced power electronic systems are needed to utilize and develop renewable energy sources. In solar PV or wind energy applications, utilizing maximum power from the source is one of the most important functions of the power electronic systems [3]–[5]. In three-phase applications, two types of power electronic configurations are commonly used to transfer power from the renewable energy resource to the grid: single-stage and double-stage conversion. In the double-stage conversion for a PV system, the first stage is usually a dc/dc converter and the second stage is a dc/ac inverter. The function of the dc/dc converter is to facilitate the maximum power point tracking (MPPT) of the PV array and to produce the appropriate dc voltage for the dc/ac inverter. The function of the inverter is to generate three-phase sinusoidal voltages or currents to transfer the power to the grid in a grid-connected solar PV system or to the load in a stand-alone system [3]–[5].In the single-stage connection, only one converter is needed to fulfill the double-stage functions, and hence the system will have a lower cost and higher efficiency, however, a more complex control method will be required.

The current normal of the industry for high power application is a three-phase, single stage PV energy systems by using a voltage-source converter (VSC) for power conversion [4]. One of the major concerns of solar and wind energy systems is their unpredictable and fluctuating nature. Grid-connected renewable energy systems accompanied by battery energy storage can overcome this concern. This also can increase the flexibility of power system control and raise the overall availability of the system [2]. Usually, a converter is required to control the charging and discharging of the battery storage system and another converter is required for dc/ac power conversion; thus, a three phase PV system connected to battery storage will require two converters. This paper is concerned with the design and study of a grid-connected three-phase solar PV system integrated with battery storage using only one five-level converter having the capability of MPPT and ac-side current control, and also the ability of controlling the battery charging and discharging. This will result in lower cost, better efficiency and increased flexibility of power flow control.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

II.STRUCTURE OF A THREE-LEVEL INVERTER AND ITS CAPACITOR VOLTAGE CONSIDERATIONS

A. Three-level Inverter :

Since the introduction of Three-level inverters in 1981 [6], [7], they have been widely used in several applications, such as: motor drives, STATCOM, HVDC, pulse width modulation (PWM) rectifiers, active power filters (APFs), and renewable energy applications [7], [8]. Fig. 1(a) shows a typical three phase three-level neutral-point clamped (NPC) inverter circuit topology.

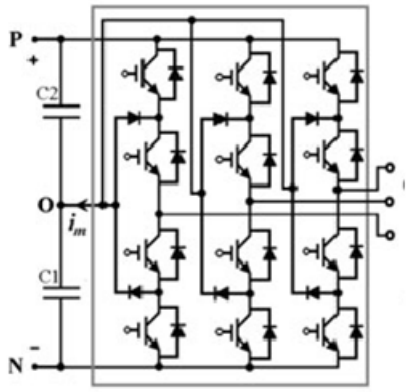

Fig. 1. Typical three-level inverter (a) structure of circuit,

The converter has two capacitors in the dc side to produce the three level ac-side phase voltages. Normally, the capacitor voltages are assumed to be balanced ,sincerity as been reported that unbalance capacitor voltages can affect the ac side voltages and can produce unexpected behavior on system parameters such as even-harmonic injection and power ripple [7], [9]. Several papers have discussed methods of balancing these capacitor voltages in various applications [6],[7],[9]–[16].

B. Balanced Capacitors Voltage :

Various strategies have been proposed to balance the capacitor voltages using modulation algorithms such as sinusoidal carrier based PWM (SPWM) or space vector pulse width modulation (SVPWM) [17]. In SPWM applications, most of the strategies are based on injecting the appropriate zero-sequence signal into the modulation signals to balance the dc-link capacitors [12], [13], [16], [18].

In SVPWM applications, a better understanding of the effects of the switching options on the capacitor voltages in the vector space has resulted in many strategies proposed to balance capacitors voltages in the three-level NPC inverter. These include capacitor balancing using conventional SVPWM, virtual SVPWM (VSVPWM) and their combination [14], [15], [19]. In vector control theory, ideally, the inverter must be able to generate the voltage output instantaneously, following the reference vector (V ref), generated by the control system. However, because of the limitation of the switches in the inverter, it is not possible to guarantee that any requested vector can be generated; as a matter of fact, only a limited number of vectors (27 vectors for five-level inverter) can be generated. To overcome such difficulties, in any space vector modulation (SVM) scheme such as SVPWM and VSVPWM, the reference vector V ref is generated by selecting the appropriate available vectors in each time frame in such a way that the average of the applied vectors must be equal to the reference vector Equation (1) shows the mathematical relation between the timing of the applied vectors and the reference vector.

$$\begin{cases} T_s \vec{V}_{\text{ref}} = \sum_{i=1}^{n} T_i \vec{V}_i \\ T_s = \sum_{i=1}^{n} T_i \end{cases} \quad (1)$$

Where Ts is the time frame and preferred to be as short as possible. It can be considered as a control update period where an average vector will be mathematically generated during this time duration. Ti is the corresponding time segment for selected inverter vector V i and n is the number of applied vectors. Generally, the reference vector is generated by three different vector (n = 3), and (1) can be converted to three different equation with three variables T1,T2, and T3 to be calculated. Several vector PWM techniques presented in [6], [7], [9]–[11], and [13]–[15] apply similar technique of timing calculation. They are six long vectors (200, 220, 020, 022, 002, and 202), three zero vectors (000, 111, and 222), six medium vectors (210, 120, 021, 012, 102, and 201), six upper short vectors (211, 221, 121, 122, 112, and 212), and six lower short vectors (100, 110, 010, 011, 001, and 101). For generating V ref , when one of the selections (V i), is a short vector, then there are two

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

choices that can be made which can produce exactly the same effect on the ac side of the inverter in the three wire connection (if voltages are balanced). For example, the short vector "211" will have the same effect as "100" on the ac side of the inverter. However, this choice will have different effect on the dc side, as it will cause a different dc capacitor to be chosen for the transfer of power from or to the ac side, and a different capacitor will be charged order charged depending on the switching states and the direction of the ac side current. For example, Fig. 2 shows the connection of the capacitors when "100"or "211" is selected, demonstrating how different capacitors are involved in the transfer of power. Capacitor balancing in most reported five-level NPC inverter applications is achieved by the proper selection of the short Vectors.

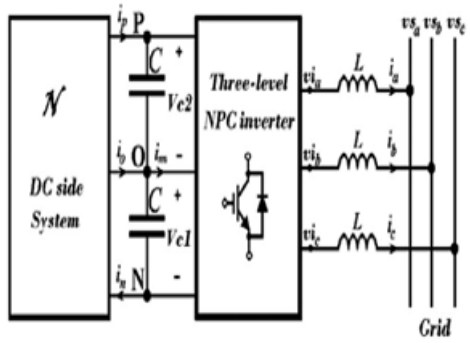

Fig.2 General diagram of a grid connected three-wire three-level inverter.

Although the control system is trying to ensure balanced capacitor voltages, should any unbalance occur during a transient or an unexpected operation, the above method will produce an inaccurate ac-side waveform which can be different from the actual requested vector by the control system. This can result in the production of even-harmonics, unbalanced current and unpredicted dynamic behavior.

However, in some applications, the requirement of having balanced capacitor voltages may be too restrictive. It is possible to work with either balanced or unbalanced capacitor voltages. The method proposed in this paper is based on the freedom of having balance or unbalanced capacitor voltages. In such applications, it is important to be able to generate an accurate reference vector based on (1), irrespective of whether the capacitor voltages are balanced or not, to achieve the desired objectives of the system.

III. Proposed topology to Integrate Solar PV and Battery Storage and Its associated control

A. Proposed Topology to Integrate Solar PV and Battery Storage Using an Improved Unbalanced DC Functionality of a Five-level Inverter The 5 level converters reduce the harmonics, when it was first used in a three-level converter in which the mid-voltage level was defined as the neutral point. The 5 level converters use capacitors in series to divide up the dc bus voltage into a set of voltage levels. To produce m levels of the phase voltage, an m level 5 level converter needs m-1 capacitors on the dc bus. A single-phase five-level converter is shown in Fig. 3. The dc bus consists of four capacitors, i.e., C1, C2, C3, and C4. For a dc bus voltage Vdc, the voltage across each capacitor is Vdc/4, and each device voltage stress will be limited to one capacitor voltage level, Vdc/4, through clamping diodes. DCMI output voltage synthesis is relatively straightforward.

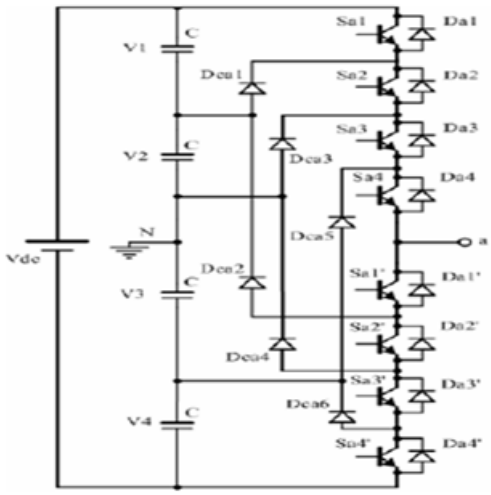

Fig.3 five- level converter

To explain how the staircase voltage is synthesized, point O is considered as the output phase voltage reference point. Using the five-level converter shown in Fig. 1.10, there are five switch combinations to generate five level voltages across A and O. Table 2.2 shows the phase voltage level and their corresponding switch states. From Table 2.2, state 1 represents that the switch is on, and state 0 represents the switch is off. In each phase leg, a set of four adjacent switches is on at any given time. There exist four complimentary switch pairs in each phase, i.e., Sa1-Sa1', Sa2-Sa2', and Sa4-Sa4'. Two new configurations of a five-level inverter to integrate battery storage and solar

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

PV shown in Fig. 3.6 are proposed, where no extra converter is required to connect the battery storage to the grid connected PV system.

Table.1. Five-level converter voltage levels and their switch states

Output V_{AO}	Switch state							
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	$S_{a1'}$	$S_{a2'}$	$S_{a3'}$	$S_{a4'}$
$V_5=V_{dc}$	1	1	1	1	0	0	0	0
$V_4=3V_{dc}/4$	0	1	1	1	1	0	0	0
$V_3=V_{dc}/2$	0	0	1	1	1	1	0	0
$V_2=V_{dc}/4$	0	0	0	1	1	1	1	0
$V_1=0.$	0	0	0	0	1	1	1	1

Features:

High-Voltage Rating Required for Blocking Diodes. Although each active switching device is only required to block a voltage level of Vdc/(m - l), the clamping diodes These can reduce the cost and improve the overall efficiency of the whole system particularly for medium and high power applications. Fig. 3.6(a) shows the diagram of the basic configuration. In the proposed system, power can be transferred to the grid from the renewable energy source while allowing charging and discharging of the battery storage system as requested by the control system. The proposed system will be able to control the sum of the capacitor voltages (VC1 + VC2 = Vdc) to achieve the MPPT condition and at the same time will be able to control independently the lower capacitor voltage (VC1) that can be used to control the charging and discharging of the battery storage system. Further, the output of the inverter can still have the correct voltage waveform with low total harmonic distortion (THD) current in the ac side even under unbalanced capacitor voltages in the dc side of the inverter. Although this configuration can operate under most conditions, however when the solar PV does not produce any power, the system cannot work properly with just one battery.

Fig. 3.6(b) shows the improved configuration where two batteries are now connected across two capacitors through two relays. When one of the relays is closed and the other relay is open, the configuration in which can charge or discharge the battery storage while the renewable energy source can generate power. However, when the renewable energy is unavailable, both relays can be closed allowing the dc bus to transfer or absorb active and reactive power to or from the grid. It should be noted that these relays are selected to be ON or OFF as required; there is no PWM control requirement. This also provides flexibility in managing which of the two batteries is to be charged when power is available from the renewable energy source or from the grid. When one of the batteries is fully charged, the relay connected to this battery can be opened while closing the relay on the other battery to charge. Special consideration needs to be made to ensure that current through the inductor Lb at must be zero prior to opening any of these relays to avoid disrupting the inductor current and also to avoid damaging the relay.

B. Control Topology:

In Fig.3 Three different relay configurations can be obtained: 1) when the top relay is closed; 2) when the bottom relay is closed; and 3) when both relays are closed. Fig. 4 shows the block diagram of the control system for configuration 1).In Fig. 3, the requested active and reactive power generation by the inverter to be transferred to the grid will be determined by the network supervisory block. This will be achieved based on the available PV generation, the grid data, and the current battery variables. The MPPT block determines the requested dc voltage across the PV to achieve the MPPT condition. This voltage can be determined by using another control loop, with slower dynamics, using the measurement of the available PV power. The details of the MPPT algorithm to determine the desired voltage (V*dc) can be found in [3] and [4]. Based on the requested active (p) and reactive power (q), and the grid voltage in the dq-axis, vsd and vsq , the requested inverter current in the dq-axis, id and iq can be obtained using (17):

$$\begin{cases} p = v_{sd} i_d + v_{sq} i_q \\ q = v_{sq} i_d + v_{sd} i_q \end{cases} \Rightarrow \qquad (2)$$

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

$$i_d^* = \frac{p^* v_{sd} - q^* v_{sq}}{v_{sd}^2 + v_{sq}^2}; \qquad i_q^* = \frac{q^* v_{sd} - p^* v_{sq}}{v_{sd}^2 + v_{sq}^2} \tag{3}$$

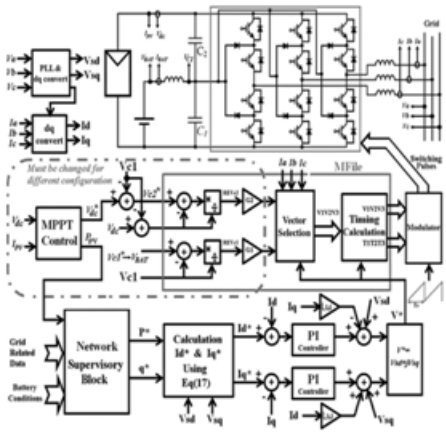

Fig.4 Control system diagram to integrate PV and battery storage.

By using a proportional and integral (PI) controller and decoupling control structure, the inverter requested voltage vector can be calculated. The proposed control system is shown in Fig. 4. In the proposed system, to transfer a specified amount of power to the grid, the battery will be charged using surplus energy from the PV or will be discharged to support the PV when the available energy cannot support the requested power.After evaluating the requested reference voltage vector, the appropriate sector in the vector diagram can be determined.

$$e_{V\,c1} = \frac{V_{C1}^* - V_{C1}}{V_{C1}}$$

$$e_{V\,c2} = \frac{V_{C2}^* - V_{C2}}{V_{C2}}$$

Where VC1 and V*C2 are the desired capacitor voltages, and VC1and VC2 are the actual capacitor voltages for capacitor C1 and C2 , respectively

IV. SIMULATION RESULTS

Mode: 1:

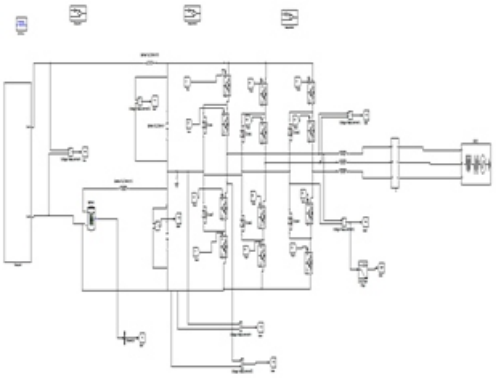

Fig :5. Circuit diagram of the proposed network during mode1

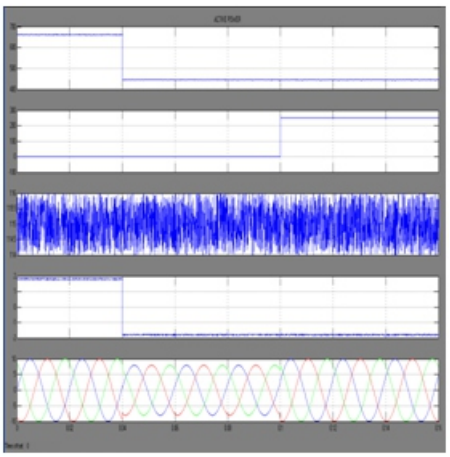

Fig: 6. simulated results for the first scenario. (a) Active power injected to the grid. (b) reactive power injected to the grid. (c) PV module DC voltage.(d) Battery current. (e) Inverter AC current. (f) Grid current.

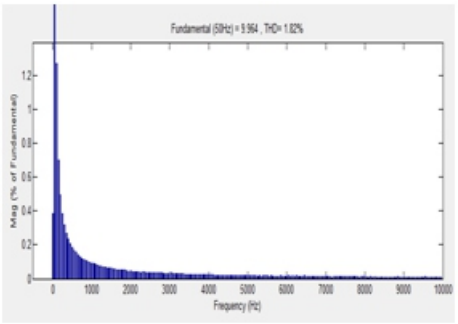

Fig.7. Total Harmonic Distortion of source current with 3 level Inverter shows 1.82%.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

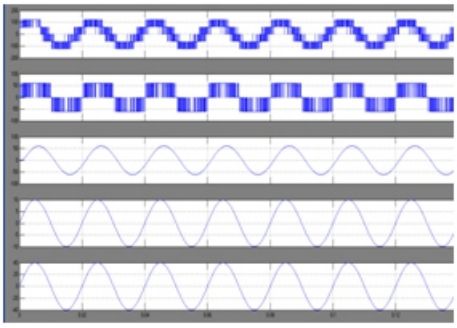

Fig.8 Simulated inverter waveforms. (a) Vab-Phase to phase inverter voltage. (b) V ao Inverter phase voltage reference to midpoint. (c) Filtered Von-Filtered inverter phase voltage reference to midpoint. (d) Filtered Von-Filtered midpoint voltage reference to neutral. (e) Filtered Van-Filtered phase voltage reference to neutral.

Mode 2:

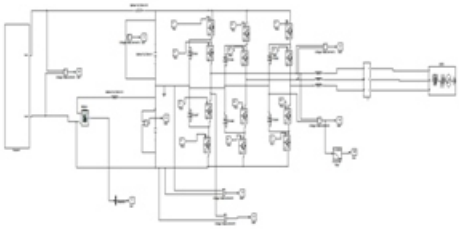

Fig.9 Circuit diagram of the proposed network during mode2.

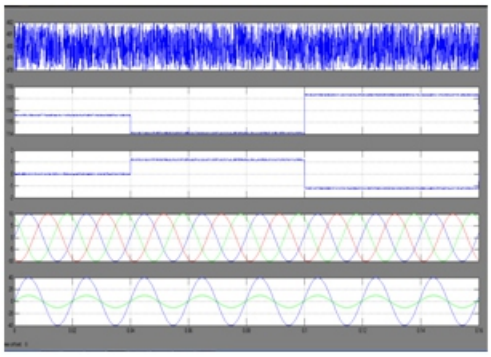

Fig.10 Simulated results for the second scenario. (a) Active power injected to the grid. (b) PV module DC voltage. (c) Battery currents. (d) Grid side currents.(e) Grid side Phase (a) voltage and its current.

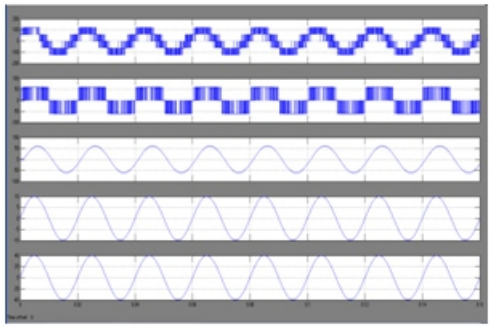

Fig.11 Simulated inverter waveforms. (a) Vab-Phase to phase inverter voltage. (b) Vao-Inverter phase voltage reference to midpoint. (c) Filtered Von-Filtered inverter phase voltage reference to midpoint. (d) Filtered Von-Filtered midpoint voltage reference to neutral. (e) Filtered Van-Filtered phase voltage reference to neutral.

Mode 3:

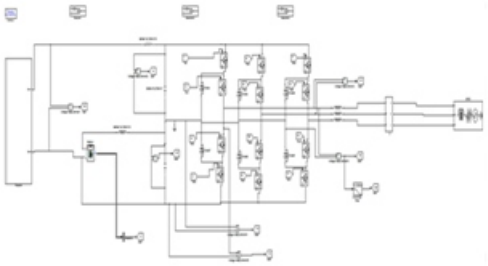

Fig.12 Circuit diagram of the proposed network during mode1.

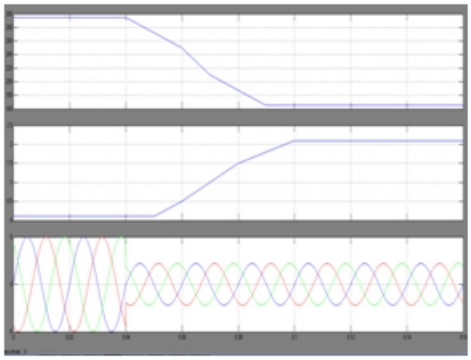

Fig.13 Simulated result for third scenario. (a) Active power injected to the grid. (b) Battery current. (c) Grid side currents.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

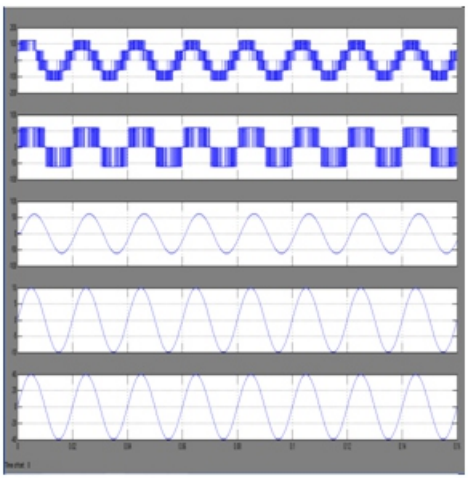

Fig.14 Simulated inverter waveforms. (a) Vab-Phase to phase inverter voltage. (b) Vao-Inverter phase voltage reference to midpoint. (c) Filtered Von-Filtered inverter phase voltage reference to midpoint. (d) Filtered Von-Filtered midpoint voltage reference to neutral. (e) Filtered Van-Filtered phase voltage reference to neutral.

Proposed Concept with 5 levels Inverter:

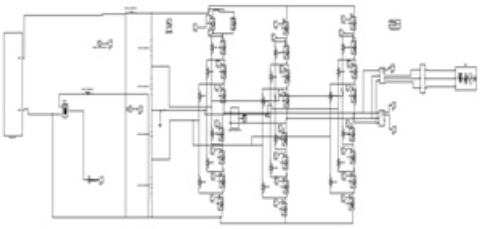

Fig.15 Circuit diagram of the proposed network extension with five level inverter.

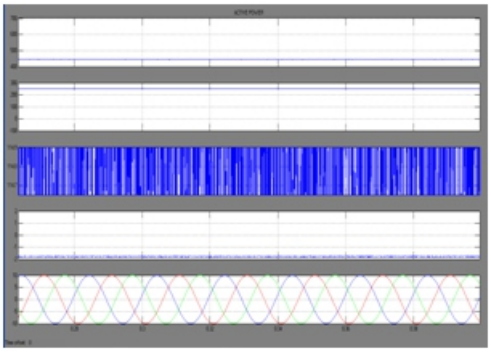

Fig.16: simulated results for the first scenario. (a) Active power injected to the grid. (b) Reactive power injected to the grid. (c)PV module DC voltage.(d) Battery current. (e) Inverter AC current.

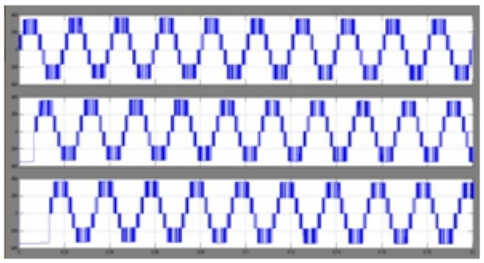

Fig:17 :Output waveforms of the 5level inverter

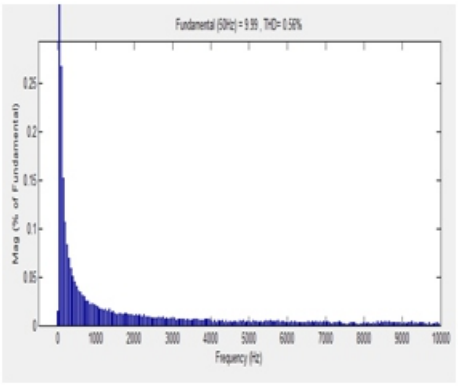

Fig.18.Total Harmonic Distortion of source current with 5 level Inverter shows 0.56%.

V.CONCLUSION:

A novel topology for a analysis of the five level and three-level NPC voltage source inverter that can integrate both renewable energy and battery storage on the dc side of the inverter has been presented. A theoretical framework of a novel extended unbalance three-level vector modulation technique that can generate the correct ac voltage under unbalanced dc voltage conditions has been proposed. Anew control algorithm for the proposed system has also been presented in order to control power flow between solar PV, battery, and grid system, while MPPT operation for the solar PV is achieved simultaneously. The results demonstrate that the proposed system is able to control ac-side current, and battery charging and discharging currents at different levels of solar irradiation. From the simulation results it has been analyzed that the three level NPC converters reduces the source current harmonic to 1.82% even it less than the IEEE STD 519, still the current suffers from harmonics. Hence a five level converter has been implemented and finally five level NPC converters reduce the source current harmonics to 0.56%. The effectiveness of the proposed 5 level NPC topology over the 5 level NPC and control algorithm was tested using simulations and results are presented.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

REFERENCES:

[1] O. M. Toledo, D. O. Filho, and A. S. A. C. Diniz, "Distributed photo voltaic generation and energy storage systems: A review," Renewable Sustainable Energy Rev., vol. 14, no. 1, pp. 506–511, 2010.

[2] M. Bragard, N. Soltau, S. Thomas, and R. W. De Doncker, "The balance of renewable sources and user demands in grids: Power electronics for modular battery energy storage systems," IEEE Trans. Power Electron., vol.25,no.12,pp.3049–3056,Dec.2010.

[3] A. Yazdani and P. P. Dash, "A control methodology and characterization of dynamics for a photovoltaic (PV) system interfaced with a distribution network," IEEE Trans. Power Del., vol. 24, no. 3, pp. 1538–1551, Jul. 2009.

[4] A. Yazdani, A. R. Di Fazio, H. Ghoddami, M. Russo, M. Kazerani, J. Jatskevich, K. Strunz, S. Leva, and J. A. Martinez, "Modeling guidelines and a benchmark for power system simulation studies of three-phase single-stage photovoltaic systems," IEEE Trans. Power Del., vol. 26, no. 2, pp. 1247–1264, Apr. 2011.

[5] M. A. Abdullah, A. H. M. Yatim, C. W. Tan, and R. Saidur, "A review of maximum power point tracking algorithms for wind energy systems," Renewable Sustainable Energy Rev., vol. 16, no. 5, pp. 3220–3227, Jun. 2012.

[6] S. Burusteta, J. Pou, S. Ceballos, I. Marino, and J. A. Alzola, "Capacitor voltage balance limits in a multilevel-converter-based energy storage system," in Proc. 14th Eur. Conf. Power Electron. Appl., Aug./Sep. 2011, pp. 1–9.

[7] L. Xinchun, Shan Gao, J. Li, H. Lei, and Y. Kang, "A new control strategy to balance neutral-point voltage in three-level NPC inverter," in Proc. IEEE 8th Int. Conf. Power Electron. ECCE Asia, May/Jun. 2011, pp. 2593–2597.

[8] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "A survey on neutral-point-clamped inverters," IEEE Trans. Ind.Electron.,vol.57,no.7,pp.2219–2230,Jul.2010.

[9] A. Lewicki, Z. Krzeminski, and H. Abu-Rub, "Space-vector pulsewidth modulation for three-level npc converter with the neutral point voltage control," IEEE Trans. Ind. Electron., vol. 58, no. 11, pp. 5076–5086, Nov.2011.

[10] J. Pou, D. Boroyevich, and R. Pindado, "Effects of imbalances and nonlinear loads on the voltage balance of a neutral-point-clamped inverter," IEEE Trans. Power Electron., vol. 20, no. 1, pp. 123–131, Jan. 2005.

[11] Z. Huibin, S. Jon Finney, A. Massoud, and B. W. Williams, "An SVM algorithm to balance the capacitor voltages of the three-level npc active power filter," IEEE Trans. Power Electron., vol. 23, no. 6, pp. 2694–2702, Nov. 2008.

[12] J. Zaragoza, J. Pou, S. Ceballos, E. Robles, C. Jaen, and M. Corbalan, "Voltage-balance compensator for a carrier-based modulation in the neutral-point-clamped converter," IEEE Trans. Ind. Electron., vol. 56, no. 2, pp. 305–314,Feb.2009.

[13] W. Chenchen and L. Yongdong, "Analysis and calculation of zerosequence voltage considering neutral-point potential balancing in threelevel npc converters," IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2262–2271,Jul.2010.

[14] S. Busquets-Monge, S. Somavilla, J. Bordonau, and D. Boroyevich, "Capacitor voltage balance for the neutral-point-clamped converter using the virtual space vector concept with optimized spectral performance," IEEETrans.PowerElectron.,vol.22,no.4,pp.1128–1135-,Jul.2007.

[15] S. Busquets-Monge, J. Bordonau, D. Boroyevich, and S. Somavilla, "The nearest three virtual space vector PWM—A modulation for the comprehensive neutral-point balancing in the three-level NPC inverter," IEEE PowerElectron.Lett.,vol.2,no.1,pp.11–15,Mar.2004.

[16] J. Pou, J. Zaragoza, S. Ceballos, M. Saeedifard, and D. Boroyevich, "A carrier-based PWM strategy with zero-sequence voltage injection for a three-level neutral-point-clamped converter," IEEE Trans. Power Electron.,vol.27,no.2,pp.642–651,Feb.2012.

[17] J. Wei-dong, D. Shao-wu, C. Liu-chen, Y. Zhang, and Q. Zhao, "Hybrid PWM strategy of SVPWM and VSVPWM for NPC three-level voltagesource inverter," IEEE Trans. Power Electron., vol. 25, no. 10, pp. 2607–2619,Oct.2010.

[18] J. Zaragoza, J. Pou, S. Ceballos, E. Robles, P. Ibaez, and J. L. Villate, "A comprehensive study of a hybrid modulation technique for the neutralpoint-clamped converter," IEEE Trans. Ind. Electron., vol. 56, no 2, pp. 294–304,Feb.2009.

[19] Z. Jian-Yong, S. Zhang-Liang, M. Jun, and L.-f. Wang, "An improved neutral-point voltage balancing algorithm for the npc three-level inverter based on virtual space vector PWM," in Proc. Int. Conf. Elect. Control Eng.,Jun.2010,pp.3283–3287.

[20] J. Pou, D. Boroyevich, and R. Pindado, "New feed forward space-vector PWM method to obtain balanced AC output voltages in a three-level neutral-point-clamped converter," IEEE Trans. Ind. Electron., vol. 49, no. 5, pp. 1026–1034, Oct. 2002