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# Designing of Synchronous Clock Distribution Using VLSI Technology for Energy Consumption

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## ABSTRACT:

In this paper, a wideband 2/3 prescaler is verified in the design of wide band multi-modulus 32/33/47/48 prescaler. Since the multimodal's 32/33/47/48 prescaler has maximum operating frequency of 6.2 GHz, the values of P and S counters can actually be programmed to divide over the whole range of frequencies.

However, the P and S zounters are programmed accordingly. The proposed Frequencies and modified bit lengths also uses an proved loadable bit-cell for Swallow - counter and consumes a low power respectively. This Project was done in XILINX 14.2 using Verilog Language.

**Keywords:** prescaler, nor gates, multiplexers, Shallow counter,Programmable Counter.

## I.INTRODUCTION:

WIRELESS LAN (WLAN) in the multigigahertz bands, such as Hiper LAN II and IEEE 802.11a/b/g, are recognized as leading standards for high-rate data transmissions, and standards like IEEE 802.15.4 are recognized for low-rate data transmissions. The demand for lower cost, lower power, and multiband circuits increased in conjunction with need of higher level of integration.

The frequency synthesizer, usually implemented by a phase-locked loop (PLL), is one of the power-hungry blocks in the RF front-end and the first-stage frequency divider consumes a large portion of power in a frequency synthesizer.

The integrated synthesizers for WLAN applications at 5 GHz reported in and consume up to 25 mW in CMOS realizations, where the first-stage divider is implemented using an injection-locked divider which consumes large chip area and has a narrow locking range.

The best published frequency synthesizer at 5 GHz consumes 9.7 mWat 1-V supply, where its complete divider consumes power around 6 mW where the first-stage divider is implemented using the source-coupled logic (SCL) circuit, which allows higher operating frequencies but uses more power. Dynamic latches are faster and consume less power compared to static dividers. The frequency synthesizer reported in uses a prescaler as the first-stage divider, but the divider consumes Power.

Most IEEE 802.11a/b/g frequency synthesizers employ SCL dividers as their first stage , while dynamic latches are not yet adopted for multiband synthesizers. In this paper, a dynamic logic multiband flexible integer-N divider based on pulse-swallow topology is proposed which uses a low-power wideband 2/3 prescaler and a wideband multimodulus 32/33/47/48 prescaler.

The divider also uses an improved low-power loadable bit-cell for the Swallow S counter. The frequency synthesizer is one of the basic building blocks in modern communication systems. The operating frequency of the frequency synthesizer is limited by the frequency divider and the voltage-controlled oscillator.

The function of channel selection in the frequency synthesizer demands programmable division ratios for the frequency divider. The integer-N frequency synthesizer is more practical, less costly and of low spurious sideband performance as compared with the fractional-N frequency synthesizer.

It is usually formed by a prescaler, a program counter (P counter) and a swallow counter( S counter). Such a topology can provide a programmable division ratio of N X P + S, where N, P and S are the division ratios of three blocks respectively. The prescaler provides a dual-modulus of N=N +1. The P counter provides a fixed division ratio according to the requirement of the overall division ratio,

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while the continuous division ratios from 3 to 2n is achieved through the S counter by periodically reloading the divideby-2 stages, where n is the number of stages of the S counter. The continuous division ratio is used to select the desired channels. Much research has been focused on the prescaler design for its highest operating frequency . However, in the modern communication system, there is an increasing demand for multi-standards applications. The requirement for wide band and high resolution operations continue to be the problems. To satisfy these requirements, different reference frequencies, and different arrangement for N, P and S counters are selected for different applications. For example, only the UNII bands are covered. In this paper, a new wideband high resolution programmable frequency divider is proposed. The wide band and high resolution are obtained by using the all-stage programmable topology in both counters, The high-speed frequency divider is a key block in frequency synthesis.

The prescaler is the most challenging part in the high-speed frequency-divider design because it operates at the highest input frequency. A dual-modulus prescaler usually consists of a divideby-2/3 (or 4/5) unit followed by several asynchronous divide-by-2 units. The operation of the divide-by-2/3 unit at the highest input frequency makes it the bottleneck of the prescaler design. To achieve the two different division ratios, D flip-flops (DFFs) and additional logic gates, which reduce the operating frequency by introducing an additional propagation delay, are used in the unit. The power consumption of this divide-by-2/3 unit, which is the greatest portion of the total power consumption in the prescaler, significantly increases due to the power consumption of the additional components.

## II. LITERATURE SURVEY:

A 13.5-mW 5-GHz frequency synthesizer with dynamiclogic frequency divider- S.; Levantino, S.; Samori, C.; Lacaita, A.L.-Feb. 2004. DESCRIPTION: The adoption of dynamic dividers in CMOS phaselocked loops for multigigahertz applications allows to reduce the power consumption substantially without impairing the phase noise and the power supply sensitivity of the phase-locked loop (PLL). A 5-GHz frequency synthesizer integrated in a 0.25-µm CMOS technology demonstrates a total power consumption of 13.5 mW. The frequency divider combines the conventional and the extended true-single-phase-clock logics. The oscillator employs a rail-to-rail topology in order to ensure a proper divider function.

This PLL intended for wireless LAN applications can synthesize frequencies between 5.14 and 5.70 GHz in steps of 20 MHz. A lowpower 5-GHz CMOS frequency synthesizer for wireless LAN transceivers has been presented. The PLL integrated in a 0.25- m CMOS technology consumes only 13.5 mW, thanks to a dynamic TSPC divider. This class of dividers is demonstrated to be suitable for multigigahertz synthesizers, since it does not impair the power supply rejection or the phase noise performance. WIRELESS LAN systems in the 5–6-GHz band, such as HiperLAN II and IEEE 802.11a, are recognized as the leading standards for high-rate data transmissions. Being intended for mobile operations, the radio transceiver has a limited power budget. The frequency synthesizer, usually implemented by a phase-locked loop (PLL), is one of the most critical blocks in terms of average current dissipation since it operates extensively for both receiving and transmitting.

The best published integrated synthesizers around 5 GHz suitable for wireless LAN receivers consume up to 25mWin both CMOS and bipolar realizations. Other synthesizers embedded in 802.11a-compliant transceivers can consume up to 200 mW.The demand for lower cost, lower power, and multiband RF circuits increased in conjunction with need of higher level of integration. The frequency synthesizer, usually implemented by a phase-locked loop (PLL), is one of the power-hungry blocks in the RF front-end and the firststage frequency divider consumes a large portion of power in a frequency synthesizer. The integrated synthesizers for WLAN applications at 5 GHz reported in and consume up to 25 mW in CMOS realizations, where the first-stage divider is implemented using an injection-locked divider which consumes large chip area and has a narrow locking range. Frequency synthesizer at 5 GHz consumes 9.7 mW 1-V supply, where its complete divider consumes power around 6 mW where the first-stage divider is implemented using the source-coupled logic (SCL) circuit, which allows higher operating frequencies but uses more power.

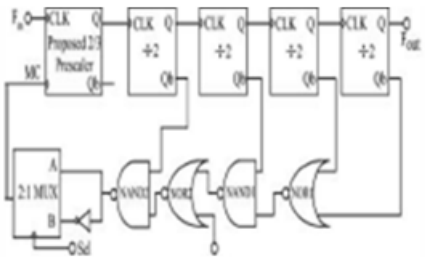

Figure.1. Multimodulus 32/33/47/48 Prescaler.

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The multi-modulus prescaler consists of the wideband 2/3 (N/(N]+I)) prescaler, four asynchronous TSPC divide-by-2 circuits ((AD)=16) and combinational logic circuits to achieve multiple division ratios. Beside the usual MOD signal for controlling N/(N+l) divisions,the additional control signal sel is used to switch the prescaler between 32/33and 47/48 modes.

1) Case 1: sel='O'

When sel='O', the output from the NAND2 gate is directly transferred to the input of 2/3 prescaler and the multi-modulus prescaler operates as the normal 32/33 prescaler, where the division ratio is controlled by the logic signal MOD. If MC=I, the 2/3 prescaler operates in the divide-by-2 mode and when MC=O, the 2/3 prescaler operates in the divide-by-3 mode. If MOD=I, the NAND2 gate output switches to logic "I" (MC=I) and the wideband pres caler operates in the divide-by-2 mode for entire operation Case 2:sel =' l' When sel=' 1', the inverted output of the NAND2 gate is directly transferred to the input of 2/3 prescaler and the multimodulus prescalar operate as a 47/48 prescaler, where the division ratio is controlled by the logic signal MOD. If MC= 1, the 2/3 prescaler operates individe-by-3 mode and when MC=O, the 2/3 prescaler operates individe-by-2 mode which is quite opposite to the operation performed when sel='O' If MOD=I, the division ratio N+ 1 performed by the multi-modulus prescaler is same except that the wideband prescale operates in the divide by-3 mode for the entire operation.

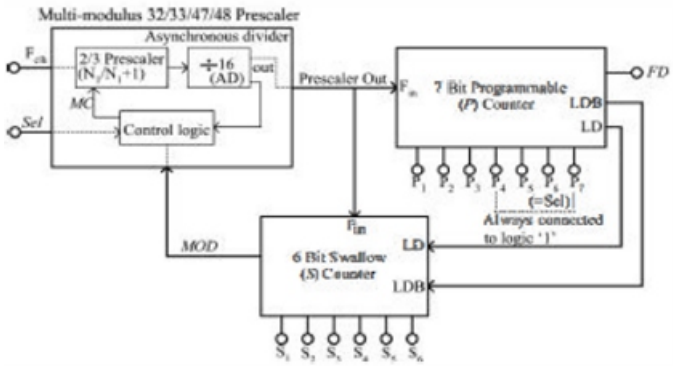


Figure.2.Dynamic logic multiband flexibleDivider.

## MULTTBAND FLEXIBLE DIVIDER:

The single-phase clock multiband flexible divider which is shown in Figl.l consists of the multi modulus 32/33/47/48 prescaler, a 7-bit programmable P-counter and a 6 bit swallow S-counter. The control signal Sel decides whether the divider is operating in lower frequency band (2.4 GHz) or higher band (5-5.825 GHz).

## A.Swallow (S) Counter:

The 6-bit s-counter shown in Fig.4. consists of six asynchronous loadable bit-cells, a NOR-embedded DFF and additional logic gates to allow it to be programmable from 0 to 31 for low-frequency band and from 0 to 47 for the high-frequency band. The asynchronous bit cell used in this design shown in Fig.4. is similar to the bit-cell except it uses two additional transistors M6 and M7whose inputs are controlled by the logic signal MOD. If MOD is logically high, nodes S 1 divide-by-48) and P, S counters start down counting the input clock cycles. When the S-counter finishes counting, MOD switches to logic "1" and the prescaler changes to the divide-by-n mode (divide-by-32 or divide-47) for the remaining P-S clock cycles. During this mode, since S-counter is idle, transistors M6 and M7 which are controlled by MOD, keep the nodes S 1 and S2 at logic "0," thus saving the switching power in S-counter for a period of (N*(P-S)) clock cycles. Here, the programmable input (PI) is used to load the counter to a specified value.

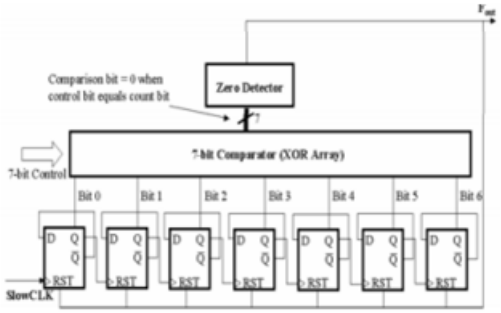


Figure.3. Block Diagram Of a 6-Bit Swallow Counter

The 6-bit ripple counter implemented as an array of flip-flops, and clocked with the gated clock provided by the AND of SlowCLKand modulus control. In addition, the comparator is implemented as an array.

## B. Programmable (P) Counter:

The programmable P-counter is a 7-bit asynchronous down counter which consists of 7 loadable bit-cells and additional logic gates. Here, bit P7 is tied to the Sel signal of the multi modulus prescaler and bits P 4 and P7 are always at logic "1." The remaining bits can be externally programmed from 75 to 78 for the lower frequency band and from 105 to 122 for the upper frequency band. When the P-counter finishes counting down to zero, LD switches to logic "1" during which the output of all the bit-cells

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in S-counter switches to logic "1" and output of the NOR embedded DFF switches to logic "0" (MOD=O) where the programmable divider get reset to its initial state and thus a fixed division ratio is achieved. If a fixed 32/33 (N/(N+ 1)) dual-modulus prescaler is used, a 7bit P-counter is needed for the low-frequency band (2.4 GHz)while an 8-bit S-counter would be needed for the high frequency band(5-5.825 GHz) with a fixed 5-bit Scounter. Thus, the multimodulus32/33/47/48 prescaler eases the design complexity of the P-counter.

## OVERVIEW:

### Existing Method:

In existing we are implementing the architecture by using 16_Divider Frequency and 6-Bit Shallow Counter and we are interlinking this to pre-scalar and 7-Bit Programmable Counter. So, in order to vary the output nature and to verify whether there is increment of complexity, delay,power variations.

### Proposed Method:

In proposed Method w implemented this structure by considering 32-Divider Frequency and 8-bit Shallow Counter and we interlinked this with same prescalar and 7-Bit programmable counter in order to check whether ant variations occur in output or to any constraints like Area, Delay, Power.

## III. SIMULATION IMPLEMENTATION:

This method helps a designer to design a circuit in a shorter timeframe. The savings in design time is achieved because the designer need not be concerned with the intricate complexities that exist in a particular circuit, but instead is focused on the functionality that is required. This new method of design has been widely adopted today in the field of ASIC design. It allows designers to design large numbers of logic gates to implement logic features and functionality that are required on an ASIC chipAs the size and complexity of digital systems increase, more computer aided design (CAD) tools are introduced into the hardware design process. Early simulation and primitive hardware generation tools have given way to sophisticated design entry, verification, high-level synthesis, formal verification, and automatic hardware generation and device programming tools.

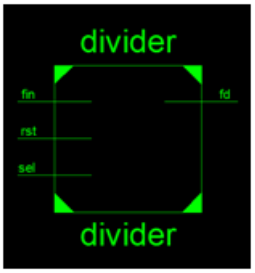


Figure.4. proposed block diagram

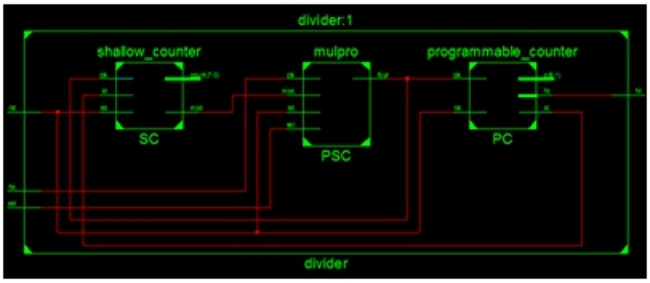


Figure.5. proposed RTL Schematic

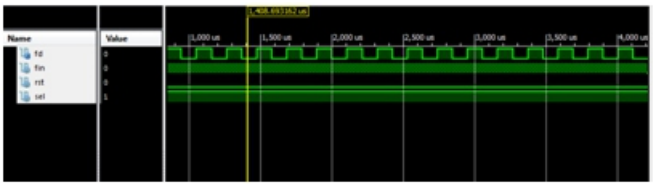

Figure.6. proposed Waveform

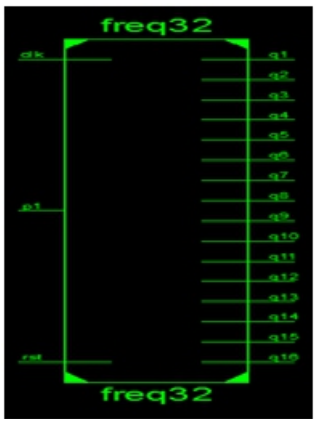


Figure.7. Frequency Divider_32

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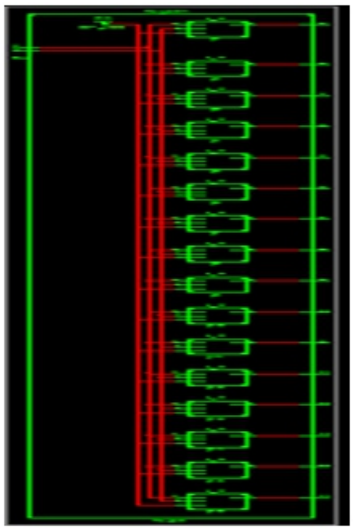


Figure.8. RTL Schematic

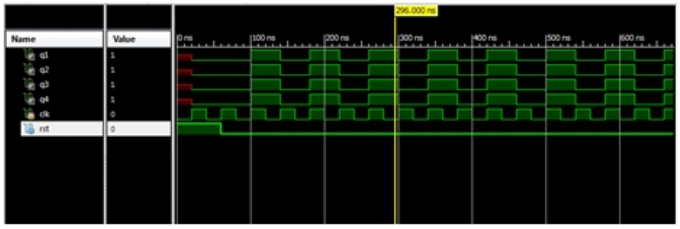


Figure.9. Waveform for FD

## AREA & DELAY & POWER REPORTS

### EXISTING:

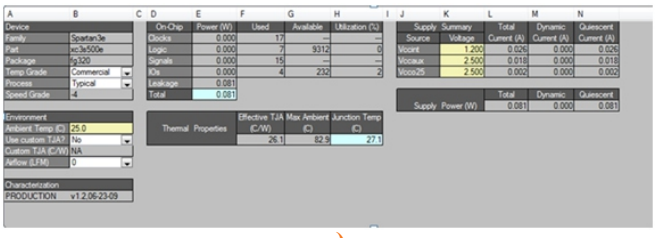
| Device Utilization Summary (estimated values) | | | |
|---|---|---|---|
| Logic Utilization | Used | Available | Utilization |
| Number of Slices | 17 | 4656 | 0% |
| Number of Slice Flip Flops | 25 | 9312 | 0% |
| Number of 4 input LUTs | 28 | 9312 | 0% |
| Number of bonded IOBs | 4 | 232 | 1% |
| Number of GCLKs | 1 | 24 | 4% |

a)

```
Timing Summary:
---------------
Speed Grade: -4

   Minimum period: 5.023ns (Maximum Frequency: 199.084MHz)
   Minimum input arrival time before clock: 4.624ns
   Maximum output required time after clock: 4.450ns
   Maximum combinational path delay: No path found
```

b)



c)

Figure.10. a)Area, b)Delay, c)Power for Existing System

## PROPOSED:

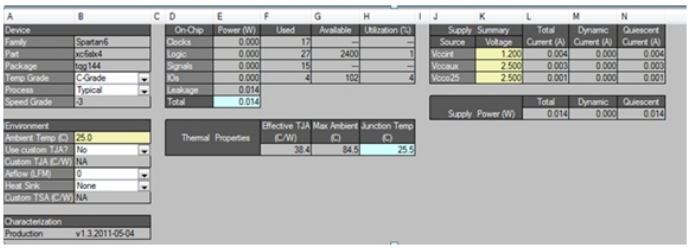
| Device Utilization Summary (estimated values) | | | |
|---|---|---|---|
| Logic Utilization | Used | Available | Utilization |
| Number of Slices | 1 | 4656 | 0% |
| Number of Slice Flip Flops | 1 | 9312 | 0% |
| Number of 4 input LUTs | 1 | 9312 | 0% |
| Number of bonded IOBs | 6 | 232 | 2% |
| Number of GCLKs | 1 | 24 | 4% |

a)

```
Timing Summary:
---------------
Speed Grade: -4

   Minimum period: 2.656ns (Maximum Frequency: 376.506MHz)
   Minimum input arrival time before clock: 2.549ns
   Maximum output required time after clock: 4.496ns
   Maximum combinational path delay: No path found
```

b)



c)

Figure.11. a)Area, b)Delay,c)Power for Proposed System

## VII. CONCLUSION:

In this paper, a wideband 2/3 prescaler is verified in the design of proposed wide band multimodulus 32/33/47/48 prescaler. A dynamic logic multiband flexible integer N divider is designed which uses the wideband 2/3 prescaler, multimodulus 32/33/47/48 prescaler. Since the multimodulus 32/33/47/48 prescaler has maximum operating frequency the values of P- and S-counters can actually be programmed to divide over the whole range of freqencies with finest resolution of 1 MHz and variable channel spacing. However,, the P- and S-counters are programmed accordingly. The proposed multiband flexible divider also uses an improved loadable bit-cell for Swallow S-counter and consumes a power of 0.081 and 0.014 mW respectively.

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