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Design of Single Phase Cascaded Multilevel Inverter Using Developed H-Bridges

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ABSTRACT:

A new general cascaded multilevel inverter is developed by using H-bridges in this paper. This topology consists of lower blocking voltage on switches and requires less number of dc voltage sources, power switches which results in decreasing the complexity and total cost of the inverter. These abilities obtained within comparing the topology with the conventional topologies from above-mentioned point of view. Moreover, a new algorithm is used to determine the magnitude of dc voltage sources for generation all voltage levels. The performance has been analyzed by functionality accuracy of the topology by using its new algorithm in generating all voltage levels for a 7-level and 31- level inverters are simulated using MATLAB/SIMULINK.The output shows the better performance results.

Key words: ***Cascaded multilevel inverter, developed H-bridge, voltage source inerter, multilevel inverter***

INTRODUCTION:

Multilevel inverters include an array of power semi-conductors and dc voltage sources, the output of which generate voltages with stepped waveforms. In comparison with a two-level voltage-source inverter (VSI), the multilevel VSI enables to synthesize output voltages with reduced harmonic distortion and lower electromagnetic interference. By increasing the number of levels in the multilevel inverters, the output voltages have more steps in generating a staircase waveform, which has a reduced harmonic distortion[1]. However, a larger number of levels increase the number of devices that must be controlled and the control complexity.

Mainly there are three types of conventional Multilevel inverter topologies. They are Diode clamped inverters, flying capacitor inverters and cascaded H – Bridge inverters[2].

In the Diode clamped inverters switches, diodes and capacitors are used. Diodes are the clamping elements. The switch pair works in complimentary mode and diodes used to provide access to mid – point voltage with the help of capacitors, the DC bus voltage can be divided into different voltage levels. The disadvantage of this type of topology is more complex to control. The failure any clamping diode will cause to shutdown of the system.

This disadvantage of Diode clamped Inverters are rectified in Flying Capacitor Inverters. This topology uses same number of switches and capacitors for generating same number of output voltage levels when compared to Diode Clamped Inverter. But the basic difference is, here the clamping elements are capacitors. The main disadvantage of Flying Capacitor Inverter is, the use of more number of capacitors will affect the voltage unbalance across capacitors. To eliminate all disadvantages like, voltage unbalancing, system shutdown when any element gets failure in circuit, a topology is developed. That is Cascaded H – Bridge Inverter. In this Cascaded H – Bridge inverters, a series connection of H - Bridge inverters are used. By using control techniques, the levels in the output will be obtained. The Cascaded H – Bridge topology are more advantageous compared to above two topologies, because it consists fewer number of components, it is very simple to control.

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To reduce the number of power supplies and power electronic components, a new topology is proposed in this paper. When compared to conventional inverters, large reduction of power electronic switches can be obtained in this topology.

In this paper, in order to increase the number of output voltage levels and reduce the number of switches, driver circuits, and the total cost of the inverter, a new topology of cascaded H – Bridge multilevel inverters is proposed. It is important to note that in the proposed topology, the unidirectional power switches are used.

Then, to determine the magnitude of the dc voltage sources, a new algorithm is proposed. Moreover, the proposed topology is compared with other topologies [3],[4]&[5], from different points of view such as the number of IGBTs, number of dc voltage sources, the variety of the values of the dc voltage sources, and the value of the blocking voltages per switch. Finally, the performance of the proposed topology in generating all voltage levels through a 7-level and 31-level inverter is confirmed by simulation using MATLAB/SIMULINK.

PROPOSED TOPOLOGY:

The multilevel inverters have received high power and medium voltage operation. The main advantages are high power quality, lower harmonics interference. The multilevel inverters have mainly three structures, they are Diode clamped inverters, flying capacitor inverters and cascaded H – Bridge inverters.

The cascaded multilevel inverter is comprised to H – Bridge inverters are classified into two groups symmetrical and asymmetrical based on the magnitude of DC voltage sources. In symmetrical type, the magnitudes of DC voltage sources are equal and in asymmetrical type the magnitude of DC voltage sources are unequal.

In proposed topology asymmetric type of configuration is used for generating more number of output voltage levels without increasing the number of switches and DC voltage sources.

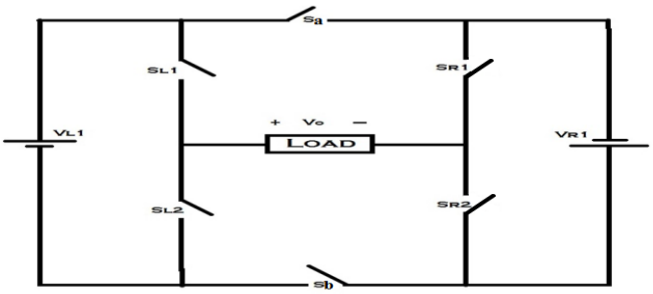

Fig.1 Multilevel inverter of 7 – level proposed Topology

The proposed topology for 7 – level inverter is as shown in Fig. (1). A H – Bridge inverter circuit with combination of two unidirectional switches and one DC voltage source is used as proposed topology for developing the proposed H – Bridge.

In proposed circuit, a IGBT with anti parallel diode is used as switch, which is capable of blocking voltage in reverse direction and allows current flow in both directions. In proposed inverter we have six unidirectional power switches (Sa, Sb, SL1, SL2, SR1 and SR2) and two DC voltage sources (VL1 and VR1). The values of DC voltage sources are different. The magnitude of VL1 and VR1 considered 1 P.U. and 2 P.U. respectively to generate more output voltage levels without increasing the number of switches and DC voltage sources.

In this topology, SL1 and SL2 or SR1 and SR2 should not turn on simultaneously to avoid the short circuits in circuit. Similar to that, Sa and Sb also should not turn on simultaneously.

NO	SL1	SL2	SR1	SR2	Sa	Sb	Vo
1	1	0	1	0	0	1	VL1+VR1
2	0	1	1	0	0	1	VR1
3	1	0	0	1	0	1	VL1
4	1	0	1	0	1	0	0
5	0	1	1	0	1	0	-VL1
6	1	0	0	1	1	0	-VR1
7	0	1	0	1	1	0	-(VL1+VR1)

Table(1) output voltage for the 7 – level inverter

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Table(1) represent the output voltages of proposed inverter at different states of switches 1 and 0, which indicating on and off states of switches respectively. Proposed seven level inverter has seven modes of operation to generate seven voltage levels.

Mode(1): In this mode, the output voltage is VL1+VR1, to generate this output voltage level, switches SL1, SR1 and Sb are turned on. SL2, SR2 and Sa are turned off.

Mode(2): In this mode, the output voltage is VR1, to generate this output voltage level, switches SL2, SR1 and Sb are turned on. SL1, SR2 and Sa are turned off.

Mode(3): In this mode, the output voltage is VL1, to generate this output voltage level, switches SL1, SR2 and Sb are turned on. SL2, SR1 and Sa are turned off.

Mode (4): In this mode, the output voltage is '0', to generate this output voltage level, switches SL1, SR1 and Sa are turned on. SL2, SR2 and Sb are turned off or vice versa.

Mode(5): In this mode, the output voltage is -VL1, to generate this output voltage level, switches SL2, SR1 and Sa are turned on. SL1, SR2 and Sb are turned off.

Mode(6): In this mode, the output voltage is -VR1, to generate this output voltage level, switches SL1, SR2 and Sa are turned on. SL2, SR1 and Sb are turned off.

Mode (7): In this mode, the output voltage is –(VL1+VR1), to generate this output voltage level, switches SL2, SR2 and Sa are turned on. SL1, SR1 and Sb are turned off.

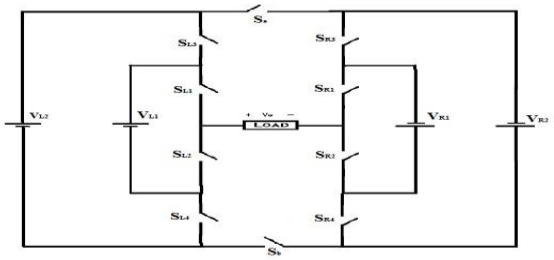

Fig.2 Multilevel inverter of 31 – level proposed Topology

The operation of 31 – level inverter is similar as 7 – level inverter. All switching states and output voltages are shown in Table (2). The proposed 31 – level inverter circuit is comprised of ten unidirectional switches (Sa, Sb, SL1, SL2, SL3, SL4, SR1, SR2, SR3, SR4) and four DC voltage sources (VL1, VL2, VR1, VR2). The magnitudes of DC voltage sources are must be considered as 1P.U, 5P.U, 2P.U and 10P.U respectively. The values of DC voltage sources are different to generate more output voltage levels without increasing the power switches and DC voltage sources.

No	SL1	SL2	SL3	SL4	SR1	SR2	SR3	SR4	Sa	Sb	Vo
1	1	0	1	0	1	0	1	0	0	1	VL2+VR2
2	0	1	1	0	1	0	1	0	0	1	VL2+VF2-VL1
3	1	0	1	0	0	1	1	0	0	1	VR2+VL2-VR1
4	0	1	1	0	0	1	1	0	0	1	VL2+VR2-VL1-VR1
5	1	0	0	1	1	0	1	0	0	1	VL1+VR2
6	0	1	0	1	1	0	1	0	0	1	VR2
7	1	0	0	1	0	1	1	0	0	1	VL1-VR1+VR2
8	0	1	0	1	0	1	1	0	0	1	VR2-VR1
9	1	0	1	0	1	0	0	1	0	1	VL2+VR1
10	0	1	1	0	1	0	0	1	0	1	VL2+VR1-VL1
11	1	0	1	0	0	1	0	1	0	1	VL2
12	0	1	1	0	0	1	0	1	0	1	VL2-VL1
13	1	0	0	1	1	0	0	1	0	1	VL1+VR1
14	0	1	0	1	1	0	0	1	0	1	VR1
15	1	0	0	1	0	1	0	1	0	1	VL1
16	1	0	1	0	1	0	1	0	1	0	0
17	0	1	1	0	1	0	1	0	1	0	-VL1
18	1	0	1	0	0	1	1	0	1	0	-VR1
19	0	1	1	0	0	1	1	0	1	0	-(VL1+VR1)
20	1	0	0	1	1	0	1	0	1	0	-(VL2-VL1)
21	0	1	0	1	1	0	1	0	1	0	-VL2
22	1	0	0	1	0	1	1	0	1	0	-(VL2+VR1-VL1)
23	0	1	0	1	0	1	1	0	1	0	-(VL2+VR1)
24	1	0	1	0	1	0	0	1	1	0	-(VR2-VR1)
25	0	1	1	0	1	0	0	1	1	0	-(VL1-VR1+VR2)
26	1	0	1	0	0	1	0	1	1	0	-VR2
27	0	1	1	0	0	1	0	1	1	0	-(VL1+VR2)
28	1	0	0	1	1	0	0	1	1	0	-(VL2+VR2-VL1-VR1)
29	0	1	0	1	1	0	0	1	1	0	-(VR2+VL2-VR1)
30	1	0	0	1	0	1	0	1	1	0	-(VL2+VR2-VL1)
31	0	1	0	1	0	1	0	1	1	0	-(VL2+VR2)

Table (2) output voltage for the 31 – level inverter

PROPOSED ALGORITHM TO SOLVE THE MAGNATUDE OF DC VOLTAG SOURCES

The magnitudes of voltage sources are unequal to generate more output voltage levels. In this paper

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following algorithm is applied generating the all voltage levels.

The 7-level proposed inverter

The magnitudes of dc voltage sources are determined as follows:

VL1=Vdc

VR1=2Vdc

Considering Table (1),the proposed 7-level inverter can be generated as 0, ±1Vdc, ±2*Vdc*, and ±3Vdc at output.

The 31-level proposed inverter

The magnitudes of dc voltage sources are determined as follows:

VL1=Vdc

VR1=2Vdc

VL2=5Vdc

VR2=10Vdc

Considering Table (2), the proposed 31-level inverter can be generated all even and odd voltage levels from 0 to 15Vdc at output with step of Vdc.

SIMULATION RESULT

The proposed multilevel inverter generating all voltage levels (even and odd), the 7-level and 31-level based on the topology show in fig(1) and fig(2) has been used for simulation. Table (1) and table(2) show switching states for 7-level and 31-level inverter. The simulation of proposed topology has done by MATLAB software. All simulation performance connected to R-load with R=100 Ω.

The simulation output wave forms of 7 – level and 31 – level are shown. Fig(3) shows the output voltage of 7 – level inverter and Fig(4) shows the current waveform of 7 – level inverter. For the 31 – level inverter, Fig (5) shows the voltage waveform and Fig (6) shows the current waveform.

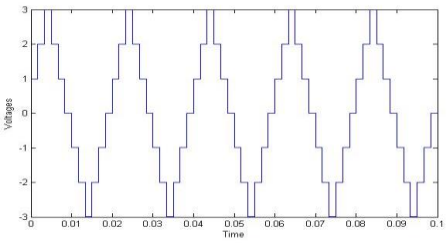

Fig.3 7 – level output voltage

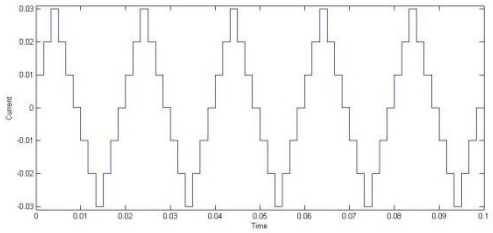

Fig.4 7 – level output current

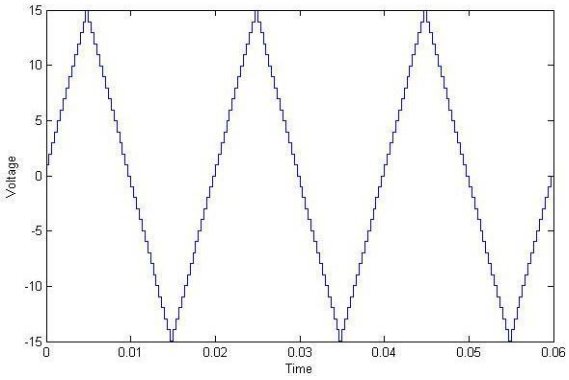

Fig.5 31 – level output voltage

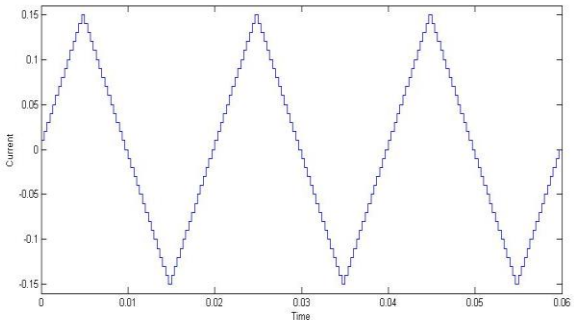

Fig.6 31 – level output current

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CONCLUSION

In this paper, a new topology is proposed for multilevel inverter to generate 7 - levels and 31 – levels at the output. In addition, a new algorithm to determine the magnitude of the dc voltage sources has been proposed. Through the proposed algorithm, the proposed inverter can generate all voltage levels (Even and Odd). The proposed topology requires less number of IGBTs, power diodes, drive circuits and DC voltage sources. Moreover, the magnitude of the blocking voltage of the switches is lower than that of conventional topologies. The advantage of this topology, that cause to reduction of installation space and cost of inverter. The performance accuracy of the proposed topology is verified through the MATLAB simulation.

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