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# Design of Low Power Fault Coverage Circuit Using LT-LFSR

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*Abstact*

***A new design approach is proposed for a fault coverage circuit. In this design a linear feedback shift register which is called as LT_LFSR (Low Transition Linear Feedback Shift Register) is used. Using LT_LFSR reduces the power consumption by reducing the number of transitions during test mode. Power reduction is done by implementing two new test pattern generation methods in LFSR. In between two consecutive test patterns generated by conventional LFSR, three intermediate random test patterns are injected. These test patterns reduce the power consumption by reducing the switching activity at the primary inputs of Circuit under Test (CUT) without the need of any additional logic. Power consumption results for c17 benchmark circuit with conventional LFSR and with LT-LFSR confirm the reduction in power using LT_LFSR.***

*Keywords—* ***LFSR, Low Power, Low Transition, Test pattern generation***

## INTRODUCTION

In VLSI design the main challenging areas are performance, cost, and power dissipation. As the consumer electronic industry is growing, demand for battery operated portable devices are increasing. These devices have to be designed such that they dissipate very less power. Power dissipation is more during test mode than normal mode of operation. So it becomes very important to reduce the power dissipation during testing.

Power dissipation is one of the important design issues in System-on-Chips (SoCs) for both normal and test mode. Power dissipation in CMOS technology is of two types static and dynamic. Static power dissipation is negligible in CMOS. It is mainly due to leakage currents. The power dissipation in CMOS circuits is mainly due to dynamic power dissipation. Dynamic power is the power that consumed when there is a transition at the node form 1 to 0 or 0 to 1. Power in CMOS circuits is given by

$$P = 0.5VDD^2E(sw)C_LF_{CLK} \quad -(1)$$

Where VDD is the power supply voltage. E(sw) is the number of transitions at the node. Fclk is the clock frequency and Cl is the capacitance of the load at the output of the gate. Power dissipation depends on the power supply voltage, number of transitions at the node and clock frequency. To reduce power dissipation power supply voltage or number of transitions or clock frequency has to be reduced. Power supply voltage cannot be reduced with degrading performance. If clock frequency is reduced circuit performance will be degraded. Power dissipation can be reduced by reducing the number of transitions at the node without affecting the circuit performance. Power dissipation in testing mode is an important issue.

With advances in VLSI technology transistors are being scaled down. As the size is getting reduced many devices can be fabricated in a single chip. As the demand for low power portable devices is increasing power dissipation has to be reduced.

Power dissipation in test mode is more than normal mode of operation. During testing more large number of test vectors has to be applied at the primary inputs of the circuit. Correlation between two consecutive test vectors is low. Because of this low correlation switching activity increases. Increase in switching

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activity increases the total power dissipation of the circuit. This increase in power dissipation can damage the device.

As the integration of chip increases, the design complexity increases. Complex designs require more test vectors during test mode. This increased switching activity increases the power dissipation which intern increases the cost of the testing.

Automatic test equipment (ATE) is the method used in external testing to apply test vectors to the circuit under test (CUT), and to analyze the responses from CUT. External testing has some disadvantages. ATE is very expensive and the cost increases as the complexity increases. Internal testing method like Built-in Self Test (BIST) method is used more commonly. BIST method generates test vectors internally. Only drawback with this method is increase in area but cost is reduced drastically. To generate test vectors in BIST, linear feedback shift register (LFSR) is used. To reduce power dissipation, LFSR has to be designed carefully.

## LOW POWER TESTING METHODS

Low power testing methods are divided into two categories

A) Low-Power Testing Methods for External Testing

B) Low-Power Testing Methods for Internal Testing

Low-Power Testing Methods for External Testing

External testing methods contain various methods used to reduce the power dissipation during external testing by ATE. Reference [3] proposed a method to generate test vectors which reduces the power by using dynamically constrained version of D-algorithm. A novel scan chain division algorithm [4] reduces the power by analyzing the signal dependencies and by creating the circuit partitions. Reference [5] proposes a low power ATPG. This ATPG reduces the growth of test vectors.

Reference [6] proposed a method which reduces the power dissipation by eliminating the switching activity in the combinational part.

Low-Power Testing Methods for Internal Testing

Various methods have been proposed to reduce the power dissipation during internal testing by using BIST. Reference [8] proposed a method to reduce power dissipation by controlling the BIST architecture for complex IC’s. This method reduces the power by scheduling the execution of each BIST element. Dual-speed LFSR [9] is an another method proposed to reduce the power dissipation by reducing the overall switching activity.

Many low power methods have been proposed for BIST architecture.

## PATTERN GENERATOR

There are two major components in BIST test pattern generator and response checker. Linear feedback shift register (LFSR) is used in both these components.

### Generating Test Vectors by using LT-LFSR

A Low transition LFSR (LT-LFSR) is proposed by combing the techniques of random pattern injection called R-Injection (RI) and Bipartite LFSR. This new LFSR will have reduced number of transitions which in turn reduces the power dissipation. By combining these two methods, in between two consecutive test vectors three intermediate patterns are generated. RI method injects a random pattern when the corresponding bits in the consecutive test vectors are not same. Bipartite LFSR generates two intermediate test vectors. First test vector uses first half and second test vector uses second half of consecutive test vectors. This new design reduces the total number of transitions and increases the correlation between two consecutive test vectors.

This design has one advantage. The same design is used for both sequential and combinational logic. This method does not reduce randomness of test vectors.

### BIST Architecture

BIST is technique which is used in self testing. To

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enable self testing BIST uses additional logic, this is integrated into the circuit under test (CUT). BIST reduces the dependency on external ATE and thereby reducing the cost of testing.

### Implementation of BIST

BIST Logic consists of Test vector generator (TPG), Test response analyzer, Multiple Input Signature Register (MISR), CUT and BIST control unit.

**CUT:** In the design which is being tested using BIST method. CUT can be sequential, combinational or memory. Test vectors are applied at the primary inputs of CUT and response is analyzed at the primary outputs of CUT.

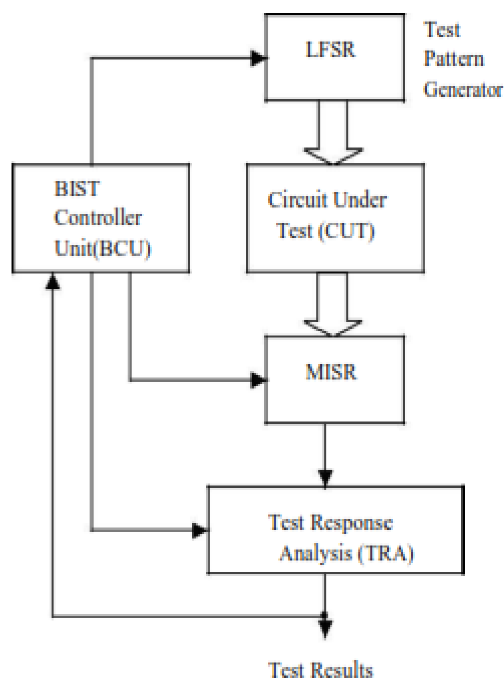


Fig1. BIST architecture

**TPG:** It generates test vectors for CUT. LFSR is used to implement Test vector generator. Test vectors can be generated in pseudo randomly of deterministically.

**MISR:** It is used for signature analysis. Signature is created by using data compression technique. MISR maps a signature for every test vector generated.

**TRA:** This is designed to check output response. It compares the output from MISR and verifies the result.

**BIST Control Unit:** It controls the test pattern generation, configures the CUT in test mode and normal mode, feeds the input value to test pattern generator.

LFSR generates test vectors, these test vectors are applied at the primary inputs of CUT. Test response is captured at the primary output of the CUT and verified by using TRA.

Implementation of Low-Transition test vector generation

This paper proposes a new test vector generation which will have low transition between two consecutive test vectors. By using this method random nature of the test vectors does not decrease. This method combines both RI method and Bipartite LFSR. By combining these two methods three intermediate patterns are generated in between two consecutive test vectors of conventional LFSR.

Let assume two test vectors generated by conventional LFSR are $T^i$ and $T^{i+1}$. Proposed method generates three intermediate test vectors $T^{k1}$, $T^{k2}$ and $T^{k3}$ in between $T^i$ and $T^{i+1}$. These test vectors are generated such that total number of transitions between these five test vectors are equal to the number of transitions between $T^i$ and $T^{i+1}$. By reducing the number of transitions power dissipation of the circuit during test mode can be reduced. To implement these intermediate test vectors area over head increases. But the area overhead is very less. These intermediate patterns are generated by the adding additional logic to the conventional LFSR.

### Design of LT-LFSR

LT-LFSR reduces the power dissipation by reducing the switching activity at the primary inputs.

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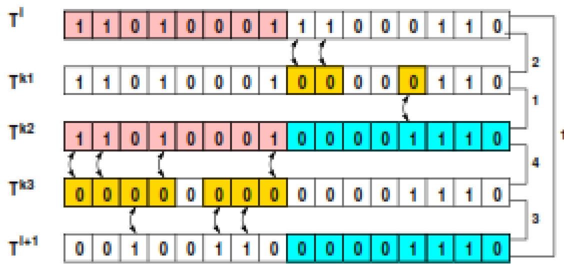

Fig 2: Low Power Pattern generation technique

This design is divided into two halves. Test vector $T^{i}$ is generated when first half is active and second half if idle. When both halves are idle new random pattern $T^{k1}$ is injected. Second random pattern $T^{k2}$ is generated when first half is idle and second half is active. Third random pattern $T^{k3}$ is generated when both halves are idle. Next pattern $T^{i+1}$ is generated again when first half is active and second half is idle.

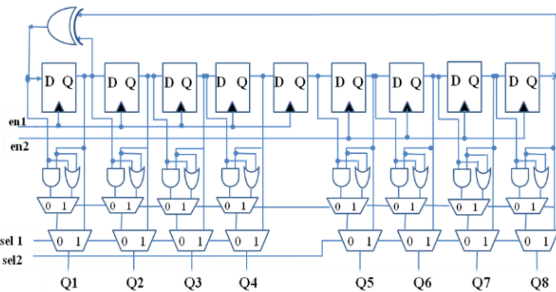


Fig 3: Low-Transition Test pattern generator

This LT-LFSR is designed in verilog hardware description language. Initial seed vector is loaded at the initial stage. In this design of LT-LFSR Q1,Q2,Q3,Q4 acts as first half and D5,Q6,Q7,Q8 acts as second half.

## Result and discussion

## Power analysis and simulation

This section presents the experimental results of LT-LFSR on ISCAS C432 bench mark circuits. 32-bit conventional LFSR and LT-LFSR is tested on C432 benchmark circuit. Simulation results verify the functionality of 32-bit LT-LFSR. 32-bit test vectors are applied at the primary inputs of the circuit under test.

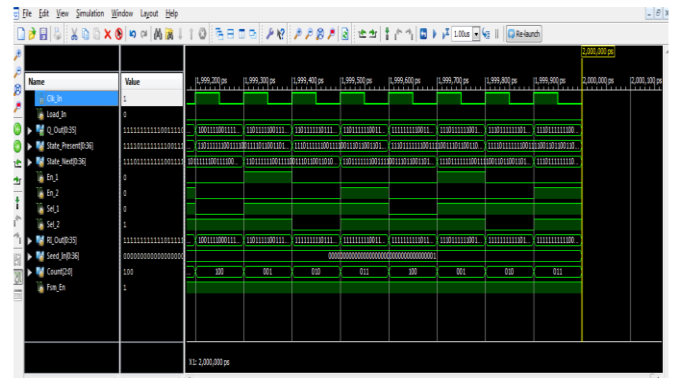

Fig 4: Simulation results of LT-LFSR

Power consumption during testing is measured using Xilinx Power Analyzer tool. Power analysis results generated from conventional LFSR and LT-LFSR are analyzed. Power reduction in LT-LFSR is 70% more when compared to conventional LFSR.

| Name | Power (W)* | Logic Power (W) | Signal Power (W) | #FFs | #LUTs |
|---|---|---|---|---|---|
| Hierarchy total | 0.00170 | 0.00064 | 0.00106 | 38 | 98 |
| test | 0.00022 / 0.00170 | 0.00000 / 0.00064 | 0.00022 / 0.00106 | 0 / 38 | 0 / 98 |

Fig 5: Power Report for conventional LFSR

| Name | Power (W)* | Logic Power (W) | Signal Power (W) | #FFs | #LUTs |
|---|---|---|---|---|---|
| Hierarchy total | 0.00109 | 0.00047 | 0.00062 | 153 | 178 |
| test | 0.00013 / 0.00109 | 0.00000 / 0.00047 | 0.00013 / 0.00062 | 0 / 153 | 0 / 178 |

Fig 6: Power Report for LT-LFSR

By comparing power consumption for LFSR and LT-LFSR it is observed that conventional LFSR uses less number LUTs in the design but power consumption is more for conventional LFSR. Because of the additional logic implemented in LT-LFSR it takes more number of LUTS but the total power consumption is less than conventional LFSR. This result proves that by reducing the number of transitions at the nodes which are internal and as well as external to the circuit under test power consumption can be reduced.

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## Conclusion

The proposed LT-LFSR has been design using verilog hardware description language and implemented using EDA tools. This method is optimized technique which reduces the power dissipation and also increases the fault coverage of the circuit under test. This method reduces the power dissipation by increasing correlation and by reducing the number of transitions at the nodes. This design is tested for fault coverage and power consumption during testing is 10.9 mW.

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