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Active DC Volatge Balancing PWM Technique for Cascaded Multilevel Converters and Dc Motors

Marla Navya
M.Tech Student,
Sridevi Women's Engineering College.

J.K.Soni, ME(EE-IDC)
Assistant Professor,
Sridevi Women's Engineering College.

Abstract:

A Multilevel converter (which can be operated both as rectifier/inverter—bi-directional) is used. This is operated in rectifier mode with three separate PMDC motor loads running at equal constant speeds. This paper a dedicated PWM technique specifically designed for single-phase (or four wire three-phase) multilevel Cascaded H-Bridge Converters is presented. The aim of the proposed technique is to minimize the DC-Link voltage unbalance, independently from the amplitude of the DC-Link voltage reference, and compensate the switching device voltage drops and on-state resistances. Such compensation can be used to achieve an increase in the waveform quality of the converter. This is particularly useful in high-power, low supply voltage applications where a low switching frequency is used. The DC-Link voltage balancing capability of the method removes the requirement for additional control loops to actively balance the DC-Link voltage on each H-Bridge, simplifying the control structure. The proposed modulation technique has been validated through the use of simulation and extensive experimental testing to confirm its effectiveness.

Index Terms:
Multilevel Converters; Predictive Control; Smart Grid.

I.Introduction:

Multilevel converters have been identified as a favored topology for high power applications as a result of advantages such as high levels of modularity, availability, overall efficiency, and high output waveform quality. This is achieved at the expense of increased numbers of components and control complexity [1]–[3]. In electrical traction drives multilevel inverters have been successfully applied in order to improve system reliability and reduce failures on motor windings as a result of the lower common mode voltages that they produce [4], [5]. The same advantages can be achieved when applied to Hybrid Electric Vehicles.

In addition to this functionality, when the DC side is connected to a set of batteries or other energy storage devices the multilevel converter can be used to maintain the charge balance of the energy storage system [6], [7]. Multilevel converters have also been applied for power quality improvement and FACTS where, especially in aerospace applications, the reduced filtering requirement needed for multilevel converter represents an advantage in terms of total converter weight and cost [8]–[11]. In the coming years, multilevel converters are likely to be used increasingly in electrical power grids in order to achieve a higher flexibility and reliability and allow smart power management in the presence of different energy sources and utilities connected to the grid.

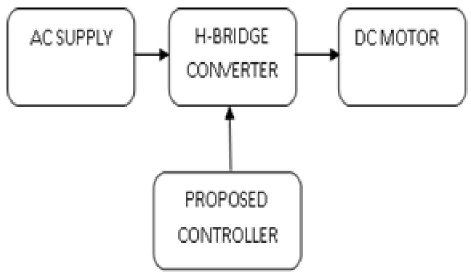
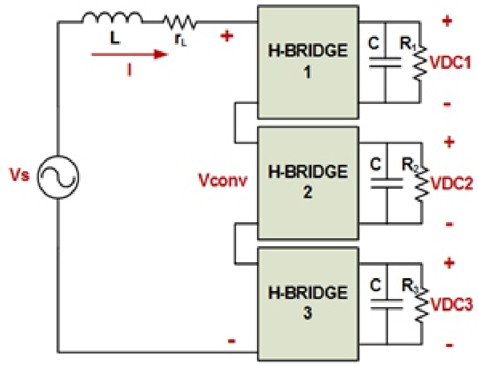


Fig.1.Proposed system block diagram

II.Cascaded H-Bridge Converters:

In Fig.1 the schematic diagram of a single-phase 7-level CHB converter, connected as an active rectifier, is shown.



(a)

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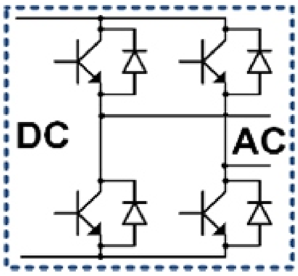

(b)

Fig. 1. Schematic diagram of a 7-level CHB in active rectifier configuration, (a) and a single HB circuit (b).

Although the proposed method is equally as effective in the inverter mode configuration, in order to test the capability of a DC-Link voltage balancing algorithm and avoid the necessity of isolated high voltage sources, the rectifier configuration is preferred. Referring to figure 1, the HBs are series-connected on the grid side and an inductive filter L, with a parasitic resistance rL, is used to facilitate the required connection between the converter and the grid. Each HB cell is connected to a capacitor, C, and a resistor, R, used to represent the loading of the converter, which in reality could potentially be another converter, providing back-to-back operation, or a real load. For a symmetrical converter, the generic i-th cell is connected to a voltage source and can produce three voltage levels, indicated as -VDCi, 0 and + VDCi. These voltage levels are associated, respectively, to states -1, 0 and 1. As a consequence, an n-cell cascaded converter can produce 2n+1 voltage levels on the AC side. The output voltage VCONV is composed of seven different voltage levels which can be produced by one or more combinations of H-Bridge states, as indicated in Table I.

V_{CONV}	*H-Bridges States*
$+3V_{DC}$	(111)
$+2V_{DC}$	(110) (101) (011)
$+V_{DC}$	(100) (010) (001) (11-1) (1-11) (-111)
0	(000) (10-1) (-101) (1-10) (-110) (01-1) (0-11)
$-V_{DC}$	(-100) (0-10) (00-1) (-1-11) (-11-1) (1-1-1)
$-2V_{DC}$	(-1-10) (-10-1) (0-1-1)
$-3V_{DC}$	(-1-1-1)

Table I. Possible voltage levels of a 3-cell converter.

III.Proposed Modulation Technique:

As stated in the introduction, the main goal of the proposed modulation method is to minimize DC-Link voltage imbalances and compensate the device voltage drops and on-state resistances. To achieve such a result, a fast response to any unbalance on the DC loads is required.

For this reason the balancing algorithm is fully integrated into the modulation scheme, without using any additional controllers. It is important to note that since one of the targets of the proposed algorithm is to equalize the voltages on the capacitors, their average value is considered as the reference voltage for each DC-link capacitor in the algorithm, while the total DC-Link voltage is set to the reference value using a Proportional-Integral action external to the modulator. In order to reduce stress on the power switches and improve their reliability, the commutations are permitted only between adjacent voltage levels i.e. it is possible to switch only one leg of one H-Bridge cell during every sampling interval. The algorithm is modular and applicable to a generic n-level CHB converter; however increasing the number of voltage levels requires an obvious increase in computational effort.

3.1 Control Scheme:

Fig. 2, shows the control block diagram implemented for the converter of Fig.1, where VDC denotes the total DC-Link voltage and VDC* is the desired DC-Link voltage. A single-phase Phase-Locked-Loop (PLL) is used in the control scheme to obtain the supply phase angle, θ, and RMS value, Vs,RMS. The PLL scheme is obtained by cascading the orthogonal system generator proposed in [37], based on the Second Order Generalized Integrator, with the three-phase PLL presented, based on a steady-state linear Kalman filter.

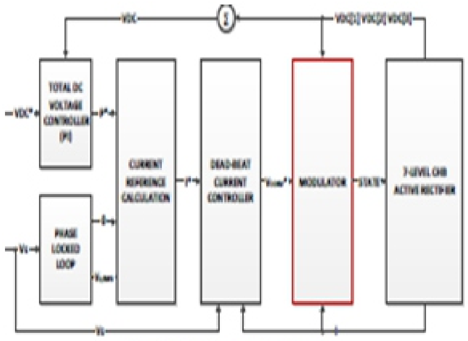

Fig 2. Overall control scheme.

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The line current is controlled in order to obtain the required DC-Link voltage; to achieve this goal, the current reference I* is calculated, at every sampling period Ts of the controller, as follows [39]:

$$I^*(t_k + iT_s) = \frac{P^*}{V_{s,RMS}\sqrt{2}} \sin(\theta + iT_s) \ , \ i = 1,2 \qquad (1)$$

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where P* is the required power, imposed by the voltage PI controller and tk is the current time instant. The current reference I* is predicted at two sampling instants, Ts and 2Ts, in order to obtain a Dead-Beat current control law, described for various converter configurations, specifically for the proposed 7-Level CHB. The obtained control law is used to derive the desired voltage reference V*CONV according to the following expression.

$$V_{CONV}^*(t_k+T_s) = V_S(t_k+T_s) - \frac{L}{2T_s}[I^*(t_k+2T_s) - I(t_k)] + r_L I^*(t_k+T_s) \quad (2)$$

The control output represents the desired converter voltage average value during the next sampling interval, applied using the proposed modulation scheme.

IV.Pi Based PMDC Motor Control:

DC motors have been around for quite a long time, converting electrical energy into mechanical energy for many, many types of applications. Additionally, mechanical energy can be converted into electrical energy for use, and in this case we refer to it as a generator. DC motors are typically constructed with a field circuit in order to produce magnetic flux in a magnetic material such as ferrite. However, one variation of a DC motor is the permanent magnet DC motor, which has no brushes and has permanent magnets on the stator or rotor. This fact allows the motors to be constructed without brushes or a field circuit – this aspect reduces the power used by the motor and allows for smaller design. Typical applications for DC motors are motors that run CD drives because they require little input power and are highly efficient. Figure 1 below shows two examples of permanent magnet DC motors, with two poles and four poles.

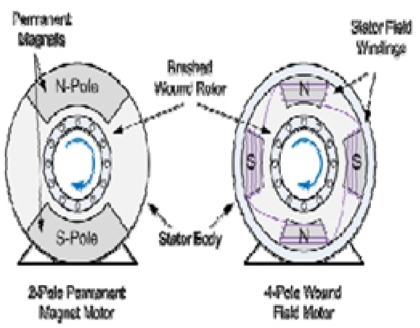


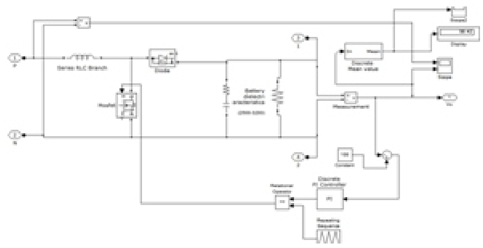
Figure 1: A typical permanent magnet DC motor – left side shows a 2-pole motor and the right is a 4-pole

The drive takes the speed reference that is specified by the Speed Reference Selection Block and compares it to the speed feedback. The speed regulator uses proportional and integral gains to adjust the torque reference that is sent to the motor. This torque reference attempts to operate the motor at the specified torque necessary to maintain speed. This regulator also produces a high bandwidth response to speed command and load changes. The important part is the Speed PI Regulator output is used to produce a torque reference for the current regulator block.

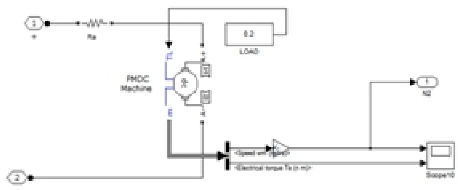
V.Simulation Results:

Simulation is performed using MATLAB/SIMULINK software. Simulink liabrary files include inbuilt models of many electrical and electronics components and devices such as diodes, MOSFETS, capacitors, inductors, motors, power supplies and so on. The circuit components are connected as per design without error, parameters of all components are configured as per requirement and simulation is performed.

Simulation Circuit Diagram:
a)PI based voltage regulator:



b)PMDC motor drive:



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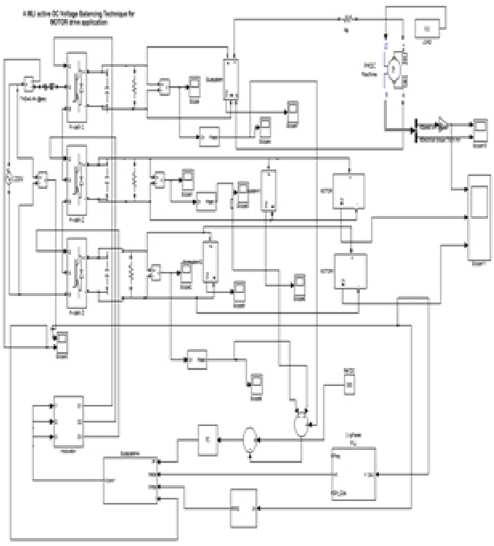
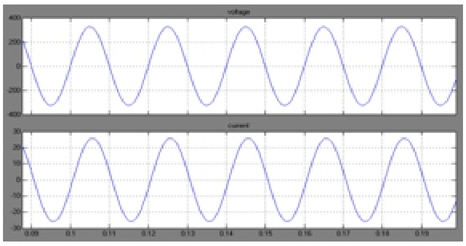
c)Converter circuit :

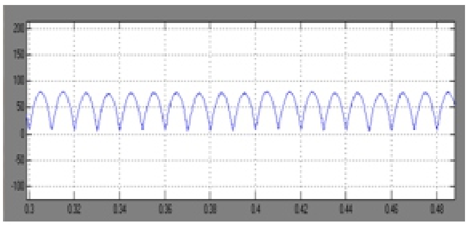


Waveforms:

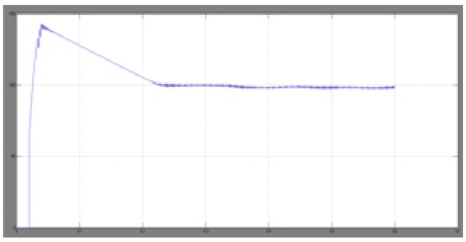
a)AC side voltage & current:



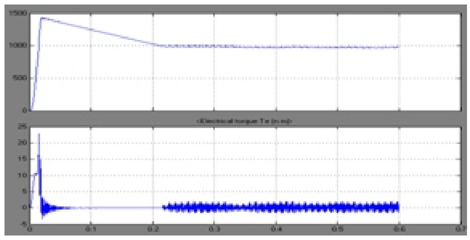
b)Unregulated DC voltage before filtering



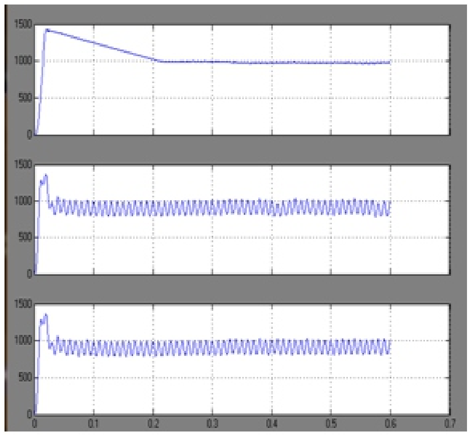
c)Regulated DC side voltage



d)Motor Speed & Torque:



e)Three Motors Speeds individually



VI.Conclusion:

In this paper a new modulation technique based PWM for low switching frequency based multilevel converters is proposed. The regulated DC voltages from three different sections of converter is fed to PMDC motors for constant and equal speed regulation. Model is validated through simulation study using MATLAB.

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