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Reduced Architecture Based Fixed Width Multiplier with Radix-8 Booth Recording

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ABSTRACT-

In DSP systems entire precision of internal values are not essential because sometimes they need approximate values. Even though we are not using the full precision why we need to design the elements that are present in architecture as sub modules their by increasing the unwanted power and area in order to eliminate the unwanted power we proposes the new concept called fixed width calculations. For DSP applications multiplication is the major considerable and important element. So we concentrated on the novel multiplication mechanism by using the fixed width and less power strategies like, for partial product reduction radix-8 modified booth algorithm and multi-operand tree for partial product addition. The proposed architecture coding written in Verilog, simulated using model-sim and synthesized using the Xilinx.

Keywords: ***DSP System, multiplication mechanism, Radix-8, Xilinx and fixed width multiplication.***

I. INTRODUCTION

In order to achieve the better performance in terms of speed and accuracy many systems like digital signal processing and communication etc relay on the efficient multiplier. Different methods, implementations and researches are increased for to find the appropriate high performance multiplier in different applications. Majorly multiplication involves the major steps like partial product generation and partial product addition lot of researches are going on these two steps. But these have the major problem of precision consideration. In general multiplication takes two n- bit input numbers and produces the 2n (n + n) bit result. In all application the total precision in not required for such application like digital signal processing turns towards the fixed width multiplication.

In fixed width multiplication process it takes the two n-bit number inputs and produces the upper MSP (most significant part) product result. With which the hardware complexity reduces along with reduced power and increased throughput. And moreover the least significant partial product addition circuitry are reduced hence the area can be reduced. But the major problems with these mechanisms are the truncation error that cannot be tolerated in present advanced systems and applications.

To overcome the problem that associated with the fixed with multiplication proper compensation bias circuit can be used. This compensation circuit carries the equivalent truncated resultant that should add to the original addition calculation circuit. While an effortful attempt to attain compensation equivalent the adder cells are used. That may be efficiently evaluates the problems that associates with the fixed width multiplication.

Different methods are proposed of the design of fixed width multiplication for to reduction of the hardware cost and increase of accuracy. In some methods different compensation circuitry designing and method are proposed. In [1], In order to neutralize the truncated error effect the constant can be to the partial product addition; this method has the feature of easy generation of compensation constant. But the pull back of this method is the truncation error cannot be eliminated that much efficiently. Whenever the increased researches on adaptive systems with the change of inputs this may expeditiously produces the proper compensation values to the resultant sum based on the input. For the increase of different multiplication researches the all these are can be adopted for the fixed width multiplication also like advanced partial product generation and partial product addition methods like modified booth

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algorithm and CSA and different addition strategies like CSA ,Walles tree and Dada tree etc.

Further organization of this paper is as follows .In Section I deals with the introduction, followed by the session II that deals with modified booths algorithm. Session III covers the proposed technique and design of fixed width multiplier. Results and analysis of our architecture with the proposed techniques is covered in Section IV. And Section V concludes the paper.

II. BOOTH ALGORITHM

Modified booth algorithm is one of the promising algorithms for the design of advanced multipliers which can reduce the partial product count. There by not only the reduce of area, power of partial product generator and also the increases the addition features There are different modified booth algorithms which selected based on the requirement and also concern with the bit length for multiplication. In general smaller bit lengths we use the radix-4 booth algorithms. In radix -4 booth algorithm it reduces the partial products by two i.e. N/2.

Whenever the bit length is increasing and also we requires the faster computations then upgraded to next radix algorithm like radix-8, radix-16 etc
In our proposal radix-8 booth algorithm can be used. It reduces the partial products N/3. Whenever the partial products reduces the area and power also reduces, especially for the fixed width multiplication it reduces the truncation error effect and hence the compensation circuit complexity also reduces.

III. RADIX-8 BOOTH ALGORITHM

Let us consider $X = \sum_{i=0}^{n-1} x_i . 2_i$

$Y = \sum_{i=0}^{n-1} y_i . 2_i$

X, Y is the two inputs of multiplier. A digit set conversion of four consecutive over lapping multiplier bits will be introduces in Radix-8 booth encoding.

$$y_{3i} + 2y_{3i} + 1y_{3i}(y_{3i-1})$$

The redundant values can be [-4 to 4].this redundant bit can be calculated by the individual group value that can be shown in below figure.
The digit set finally formed as

$$d_i = y_{3i-1} + y_{3i} + 2y_{3i+1} - 4y_{3i+2}$$

For generation of partial products from the redundant bits there are two multiples namely hard multiple and soft multiple.

Soft multiple is nothing but it can be generated from general shift operations but whereas for hard multiple cannot be generated using by the general shift operation. In our proposed Radix-8 booth encoding we do have the hard multiple. For determination of partial product of hard multiple can be done in two ways that is by adding or by subtracting i.e. the generation of 3X can be done in two ways by addition 2X+X or subtractions 4X+X .in general addition can be preferred rather than subtraction.

For generation of partial products from the overlapped we use the two basic elements called booth encoder and booth selector. The booth encoder is used to determine the redundant value of the group along with the sign based on the redundant value generated at the booth encoder the booth selector will select the particular value, below figure shows the architecture of booth encoder and selector.

Partial product PP0, PP1 and PP2are generated using the Booth Encoder (BE) and Booth Selector (BS) are show in fig1&2

TABLE I
RADIX-8 BOOTH ENCODING

Group value	*Redundant value*
0000	0
0001	+1
0010	+1
0011	+2
0100	+2
0101	+3
0110	+3
0111	+4
1000	-4
1001	-3
1010	-3
1011	-2
1100	-2
1101	-1
1110	-1
1111	0

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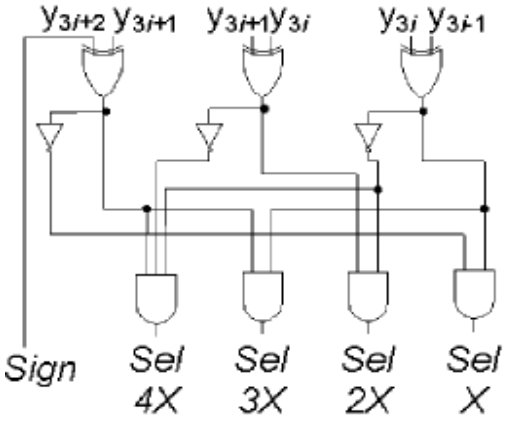

Fig1. booth encoder

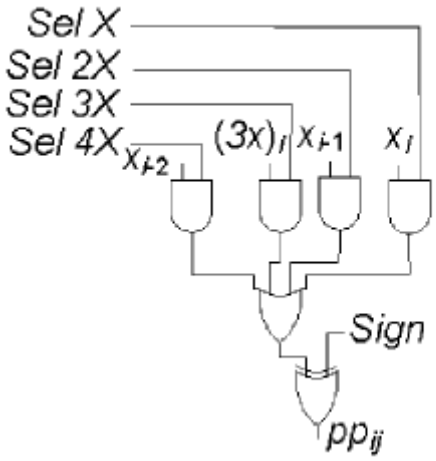

Fig2. booth selector

Partial product PP0, PP1 and PP2are generated using the Booth Encoder (BE) and Booth Selector (BS) are show in fig1&2.The Booth Encoder takes the overlapped multiplier bits and produces the one hot coded digit along with the sign digit. The result of Booth Encoder outputs fed to the Booth selector which produces the proper multiple outputs to chive the PP_i.bit generation of Radix-8 booth encoded partial product of bit PP_{ij} .

Partial product addition can be carried out by the CSA tree which can reduces the addition time by limiting the addition stages. And addition time also reduces by avoiding the carry propagations at each stage

IV. RESULTS AND DISCUSSION

The above fig shows the radix-8 fixed with multiplier with truncation error compensation circuit result. By this the partial products can be reduced and as well as the operation time also will be reduced.

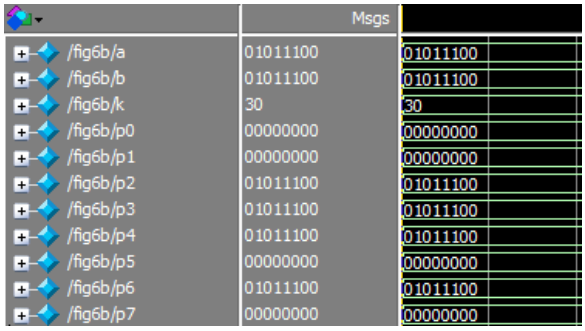

Fig 3 simulation results of proposed method

V. CONCLUSION

Proposed method is design with the fixed width multiplier with the Radix-8 booth recording multiplier with the CSA tree addition and easy truncated error compensation circuit can be designed. This gives the efficient method for the designing the fixed width multiplier gives the less area utilization and less power.

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