

Design of Class -AB Op-Amps with High and Symmetrical Slew -Rate with Low Power Consumption



P.Swathi

**Assistant Professor,
Department of ECE,**

**Mallareddy Engineering College for women, R.R Dist,
AP, India.**



K.Raju

**Assistant Professor,
Department of ECE,**

**Mallareddy Engineering College for women, R.R Dist,
AP, India.**

ABSTRACT:

We introduced various class AB two stage op-amps with high and approximately symmetrical slew rate and very simple architecture are introduced. A combination of adoptive loads and current replicating branch with scaled-down transistors is used to implement a push-pull output stage with maximum output current several times higher than the bias current. post layout simulation and measurement results are presented and verify a 400%-500% slew rate and 80%-100%GB.

Keywords:

Symmetrical slew rate, operational amplifiers, class AB operation, gain, CMOS analog integrated circuits.

I.INTRODUCTION:

In single-stage op-amps achieves highly symmetrical slew rate by using different efficient schemes. A drawback of a single stage op-amp is that relatively low open-loop gain(AOL). since the output cascading transistors is to increase the output resistances(R_{out}) would seriously limit the maximum output current and the slew rate enhancement factor. In the conventional class-A two-stage Miller-compensated op-amp is characterized by a highly asymmetrical slew rate with large positive slew rate and much lower negative slew rate. This lower negative-slew rate is due to the output transistor (MoN) acts as a dc current source with value $2I_B$ and increase the static power dissipation. To avoid this limitation many class AB two-stage op-amps have been reported. Most of them feature is relatively modest effective slew rate improvement and require additional complex circuitry, and non negligible additional static power dissipation or increased supply requirements. This decreases their current efficiency.

In fig (b) achieves class AB operation with additional small hardware. It consists of a large resistive R_{large} and small capacitor C_{bat} . This combination operates as a open battery that transfers ac variations taking place at the gate of Mop to the gate of Mon transistors. The output stage operates as a push-pull amplifier and provides dynamic class-AB operation with large positive and negative output currents. This does not increase power dissipation or supply requirements but operates only for dynamic changes with frequencies.

II.CLASSAB TWO-STAGE OP-AMPS PROPOSED

A.Op-Amp with Current Replication Branch:

To achieve class AB operation, the output transistor MoN can be transformed into an active amplifying device by simply adding a current replicating branch formed by M2R and MoNR as shown in fig1(c). This transfers current variations I_a in M1-M2 to the output transistor MoN and increases and increases the maximum positive output current by $2I_B$. The maximum negative current is still limited to a value of $2I_B$. The current replicating branch does not require additional compensation circuit. Since the node V_x with gain in the current replicating branch is gate to the drain of MoN, and at the higher frequencies miller compensation causes MoP to behave as low impedance load.

This reduces the gain between the gate of MoN and the op-amps output terminal to closely a unity value. The current replicating branch has small dimensions reducing area and static power dissipation. In order to achieve large negative output currents, a non-linear adoptive load can be used. This modification is seen in another circuit.

B. Class AB Two-Stage Op-Amp Using Adaptive Loads:

By using an adaptive load at the input side in the circuit we can achieve class AB operation efficiently. Two different alternatives are shown in fig (d) and fig (e). In both cases, the adoptive loads manoeuvre the large variation of output resistance of transistors between triode and saturation regions in quiescent conditions. In both schemes a current increase in I_a causes transistors to go in triode region and to develop large drain-source voltages. These changes cause large currents flow in the output transistors Mop and thanks to the current replicating branch, MoN. A bias voltage with value $V_{btriode} = V_{ss} + V_{gs} + V_{DSSat} = V_{TH} + 2V_{DSSat}$ is required at the gate of MoNR. Where $V_{DSSat} = V_{gs} - V_{th}$ is the minimum V_{ds} voltage to operate in saturation region. This $V_{btriode}$ leaves a quiescent drain-source voltage for MoNtriode with value V_{DSSat} , which causes MoNtriode to operate at the boundary between the triode and saturation regions. The circuit of fig (2) is denoted as operational amplifier with current replicating branch and adaptive loads. These topologies are not harmful in terms of stability of the ac responses. The current replicating branch helps compensating the current through the miller capacitor just as in other multipath miller zero-cancellation scheme.

III. SIMULATION RESULTS:

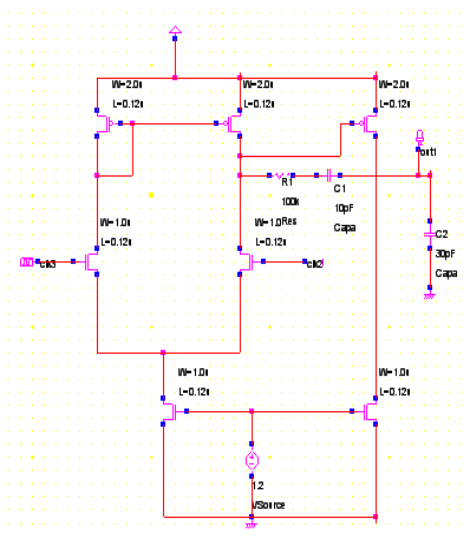


Fig 1(a) .Schematic of Conventional class A two-stage miller op-amp

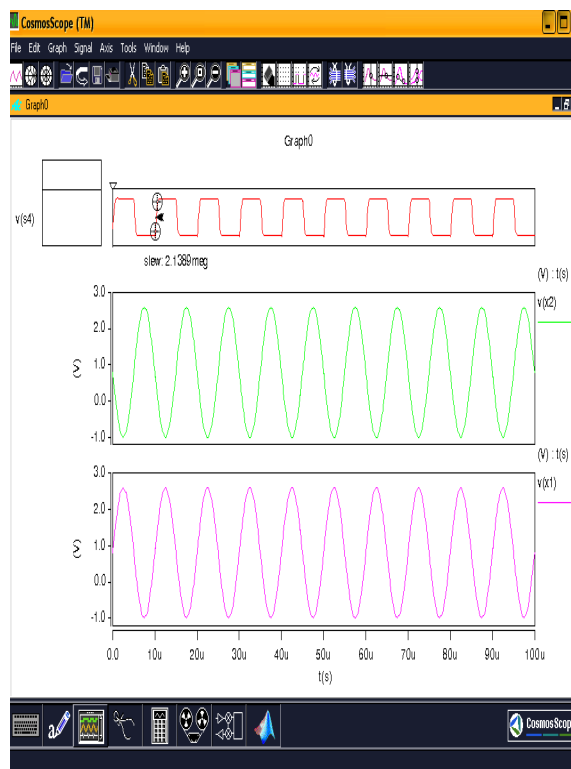


Fig1(b). Output result Conventional class A two-stage miller op-amp

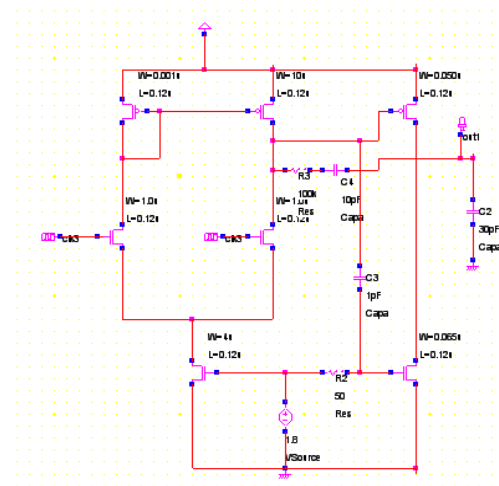


Fig 2(a). Schematic of Free class AB op-amp

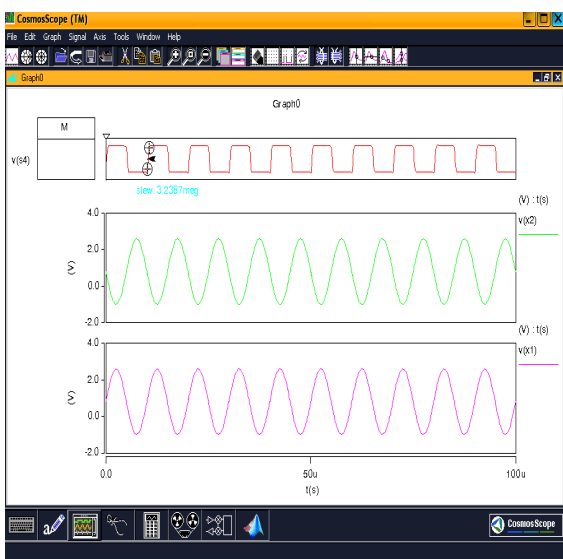


Fig 2(b).Output waveform Free class AB op-amp.

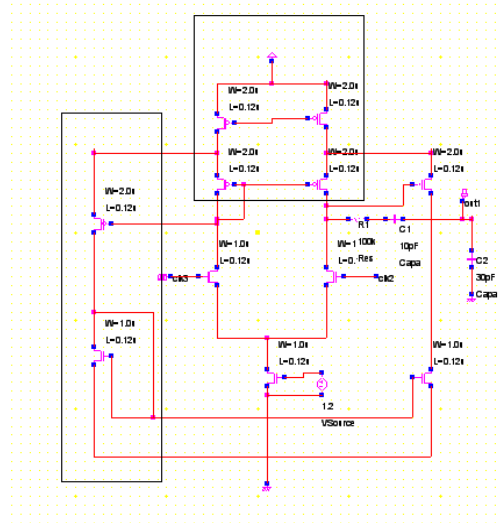


Fig 4(a).Schematic of class AB two stage op-amps with current replicating branch using adoptive loadIII.

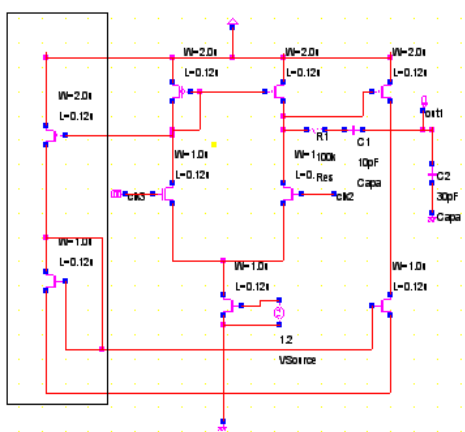


Fig 3(a) Schematic of push pulls op-amp with current replication branch.

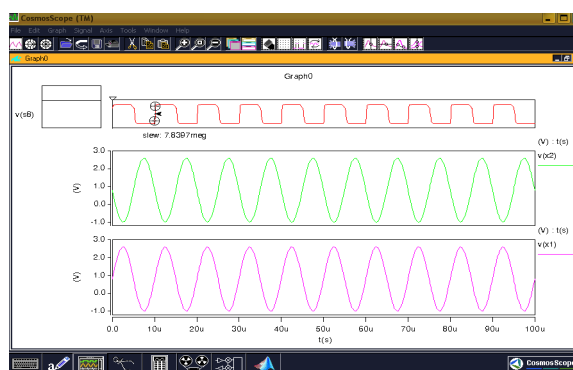


Fig 4(b).Output waveform of class AB two stage p-amps with current replicating branch using adoptive loadII.

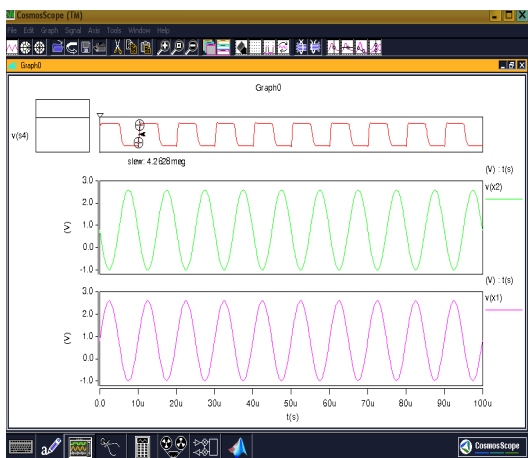


Fig 3(b).Output waveform of push pulls op-amp with current replication branch

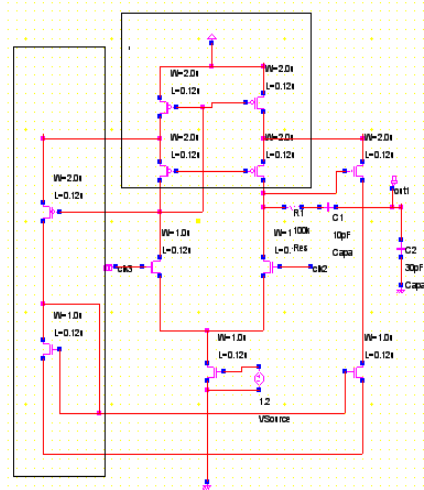


Fig 5(a).Schematic of Class AB two stage op-amp with current replicating branch using adaptive load I at the input stage.

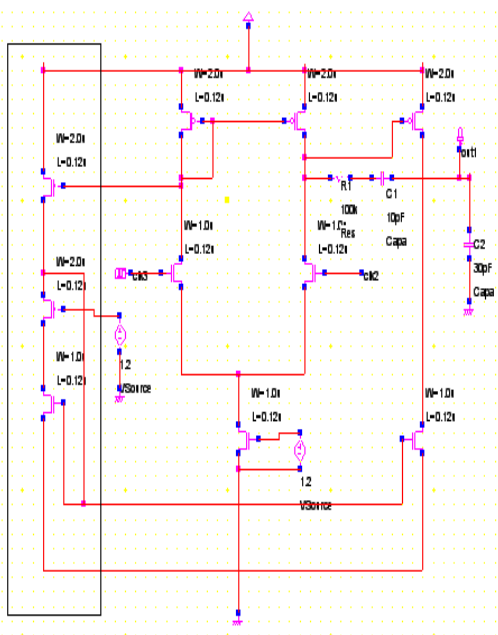


Fig 5(b).Schematic of class AB two-stage op-amp with current replicating branch using an adaptive load.

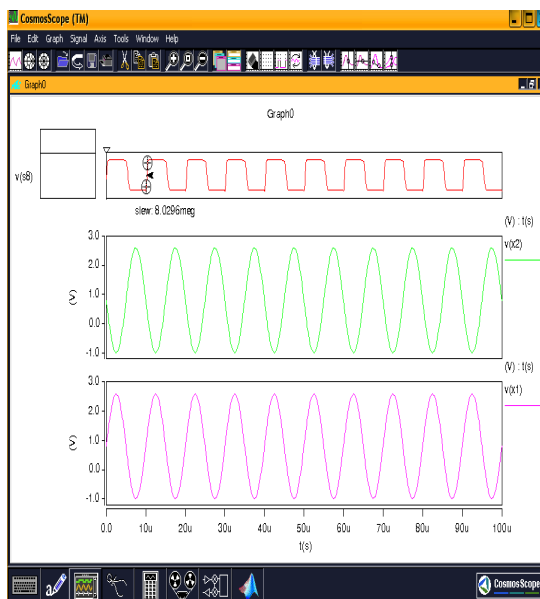


Fig 6(b).Output waveform of class AB two-stage op-amp with current replicating branch using an adaptive load

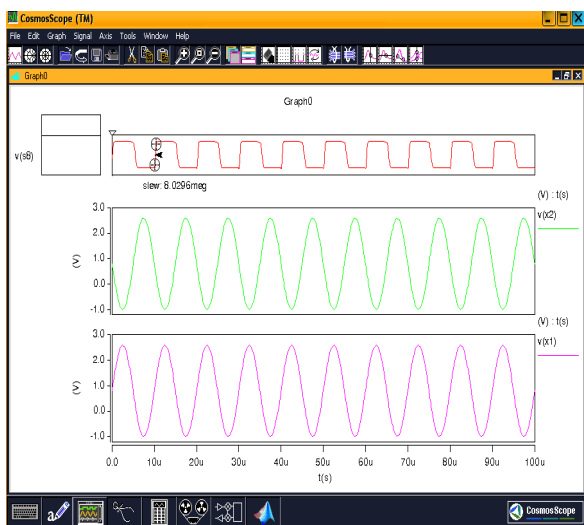
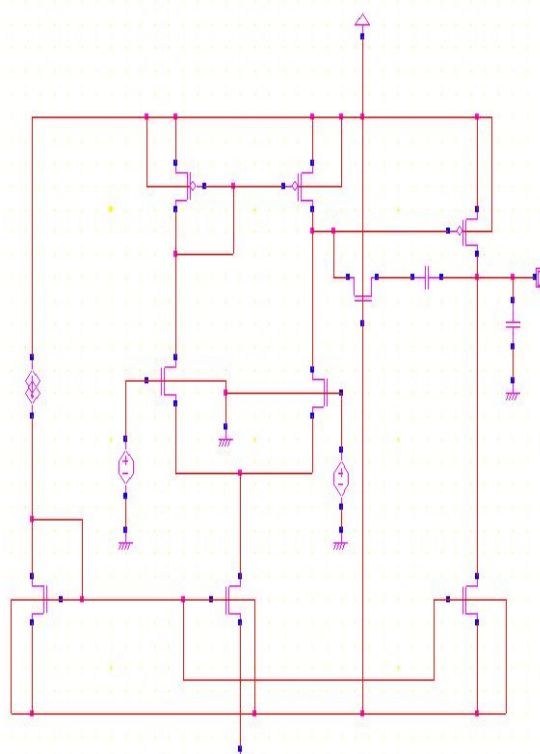
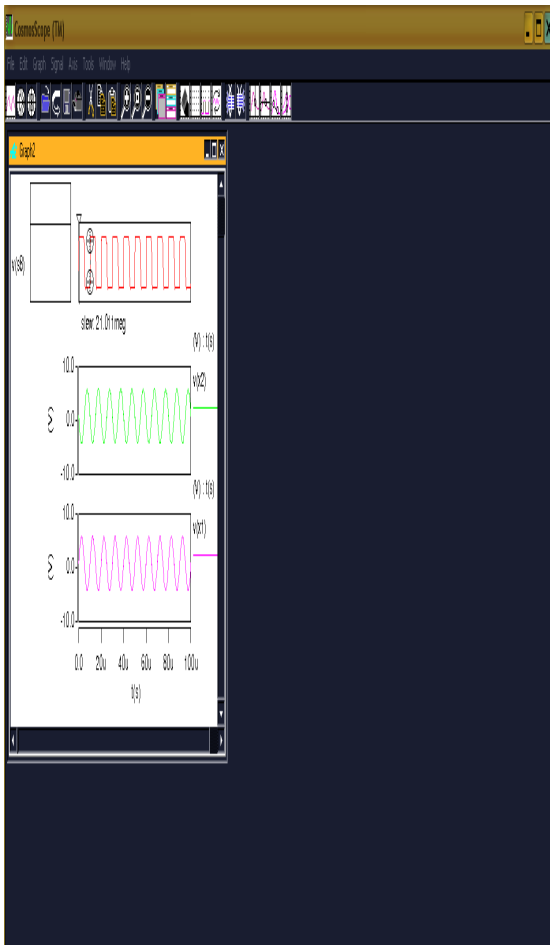


Fig 6(a).Output waveform of Class AB two stage op-amp with current replicating branch using adaptive load I at the input stage.



FIG(7) Common gate class-ab op-amp



IV.COMPARISION TABLE

CIRCUIT NAME	SLEW RATE (V/ μ S)	POWER (MW)
(a) Conventional two stage op-amp	2.1389Meg	2.761
(b)Freeclassab op amp	3.2387 Meg	1.8597
(c) Push pull op-amp with current replication branch	4.2628 Meg	2.2329
(d) Class ab two stage opamp with current replication branch and adoptive loads	7.8397 Meg	2.2818
(e) Class AB two stage op-amp with current replication branch using adoptive load I at the input stage	8.0296 Meg	6.3124
(f) Proposed	8.0296 Meg	1.1636
(g) common gate class ab-op-amp	21.011Mega	1.0612

V.ACKNOWLEDGMENT:

The authors gratefully acknowledge the constructive comments by the reviewers.

VI. CONCLUSION:

The different schemes of power-efficient class AB two-stage op-amps are introduced by using a current replication branch and adoptive loads have been experimentally tested. They achieve approximately symmetrical and high slew rate with very small additional static power dissipation and small additional circuitry.

REFERENCES:

[1] A.J. López-Martín, A. J., Baswa, S., Ramirez-Angulo, J., & Carvajal, R. G. (2005). Low-voltage super class AB CMOS OTA cells with very high slew rate and power efficiency. Solid-State Circuits, IEEE Journal of, 40(5), 1068-1077. May 2005.

[2] Galan, J. A., Lopez-Martin, A. J., Carvajal, R. G., Ramirez-Angulo, J., & Rubia-Marcos, C. (2007). Super class-AB OTAs with adaptive biasing and dynamic output current scaling. Circuits and Systems I: Regular Papers, IEEE Transactions on, 54(3), 449-457. Mar. 2007

[3] Ramirez-Angulo, J., & Holmes, M. (2002). Simple technique using local CMFB to enhance slew rate and bandwidth of one-stage CMOS op-amps. Electronics Letters, 38(23), 1409-1411. Nov. 2002.

Author's Details:

P.Swathi, Received the Master's degree from JNTU, Kakinada, in 2010. During her Master's thesis research, she was involved in the area of neural network design and implementation, and analog and mixed-signal chip design.. She is working as Assistant Professor in Department of Electronics and Communications Engineering in Mallareddy Engineering College for women, R.R Dist, AP, India. She has 6 years of Teaching Experience. Her Research Interests in Signal Processing and VLSI.

K.Raju, Received the Master's degree from JNTU, Hyderabad, in 2009. During her Master's thesis research, he was involved in the area of neural network design and implementation, and analog and mixed-signal chip design.. He is working as Assistant Professor in Department of Electronics and Communications Engineering in Mallareddy Engineering College for women, R.R Dist, AP, India. He has 6 years of Teaching Experience. His Research Interests in Signal Processing and VLSI.