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A Single Phase Multilevel Inverter Based Seven-Level Switched-Capacitor Fed Induction Motor Drive

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Abstract

The main objective here is to analyze the seven level and nine level diode clamped multilevel inverter for control the speed of an induction motor with respect to their variable loads. To give high quality sinusoidal input voltage with reduced harmonics to IMD (Induction motor Drive) the proposed Scheme for diode clamped multilevel inverter is multicarrier SPWM (sinusoidal pulse width modulation) control. The V/f technique is used to obtain an open loop speed control. This method can be implemented by changing the supply voltage and frequency applied to the three phase induction motor at constant ratio. The proposed method (7-Level MI) is an effective replacement for the conventional method which has high switching losses, as a result a poor drive performance. The voltage ripple of the capacitors is also reduced, which leads to higher power conversion efficiency. This feature improves the reliability of the circuit. A induction motor is run with the proposed topology for the full modulation range. The effectiveness of the capacitor balancing algorithm is tested for the full range of speed and during the sudden acceleration of the motor. The improved seven level PWM converter versions is also considered to suppress the circulating current due to phase shift pulse modulation principle by using MAT Lab/Simulink.

Index Terms — ***a boost converter, H-bridge, Switched capacitor converters, charge pump, switched-capacitor, Induction Machine Drive.***

I.INTRODUCTION

Multilevel inverters have changed the face of medium- and high-voltage drives. The most popular topologies of multilevel converters are the neutral point-clamped inverter (NPC), the flying capacitor inverter (FC) , and the cascaded H-bridge (CHB) inverter[1]. Each one of these inverters has its own merits and demerits. In the NPC inverter, multiple dc sources are generated by splitting a single-dc bus voltage using capacitor banks. This configuration has large number of clamping diodes and presents the problem of dc bus capacitor unbalance especially with high number of voltage levels. An interesting work for balancing capacitor in NPC inverter that can be operated in limited modulation range has been presented in . A pulse-width modulation (PWM) control scheme to balance the dc link capacitor voltages of the NPC inverter, connected in cascade with a two level inverter to realize a five level inverter structure for an open end winding induction motor, is proposed. The concept of FC inverter was introduced first in 1992[1].

In this configuration, multiple capacitors of different voltage magnitudes are used to generate multiple voltage levels. The advantages include modularity, lack of clamping diodes, lack of problems like unbalance in the split dc –link capacitors, etc. Also, as in the NPC case, single supply can be used to generate multiple pole voltage levels.

There are many modulation methods to drive a multilevel inverter: the multicarrier PWM, the space vector modulation, the hybrid modulation [12] the selective harmonic elimination and the alternatively in

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opposition (APO) disposition PWM. In the preliminary version of this paper, one of the APO PWMs is applied, which is the combination of the level-shifted PWM (LS-PWM) and the phase-shifted PWM (PS-PWM). That is called "level- and phase-shifted PWM (LPS-PWM)." The LPS-PWM realizes low voltage ripple on the capacitors in the SCISPC, which also leads to high-efficiency power conversion. In addition, the carrier frequency of LPS-PWM is reduced to half that of the conventional LS-PWM in SCISPC.

The modulation method, the determination method [11] of the capacitance, and the loss calculation of the inverter proposed. A charge pump outputs a larger voltage than the input voltage with switched capacitors [7], [8]. When the several capacitors and the input voltage sources are connected in parallel, the capacitors are charged. SC inverter is consists of a Marx inverter structure and an H-bridge [10]. The proposed inverter can output larger voltage than the input voltage by switching the capacitors in series and in parallel. The maximum output voltage is determined by the number of the capacitors.

The voltage magnitude of the gate pulses generated by the microcontroller is normally 5V. To drive the power switches satisfactorily the up to coupler and driver circuit are necessary in between the controller and multilevel inverter. The output ac voltage is obtained from the multilevel inverter can be controlled in both magnitude and frequency (V/f open loop control). The controlled ac output voltage is fed to the induction motor drive. When the power switches are ON current flows from the dc bus to the motor winding. The motor windings are highly inductive in nature; they hold electric energy in the form of current. This current needs to be dissipated while switches are off. Diodes are connected across the switches give a path for the current to dissipate when the switches are off. These diodes are also called freewheeling diodes.

The V/f control method permits the user to control the speed of an induction motor at different rates. For continuously variable speed operation, the output frequency of multilevel inverter must be varied. The applied voltage to the motor must also be varied in linear proportion to the supply frequency to maintain constant motor flux.

II.CIRCUIT DESCRIPTION

Fig. 1 shows a circuit topology of the proposed inverter, where *Sak*, *Sbk*, *Sck*(k = 1, 2, . . . , $2n$ − 2) are the switching devices which switch the capacitors *Ck*(k = 1, 2, . . . , $2n$ − 1) in series and in parallel. Switches $S1$ − $S4$ are in the inverter bridge.

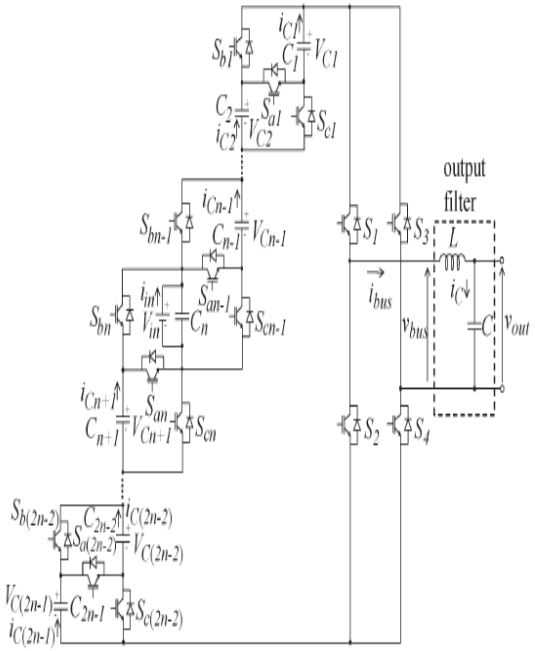

Fig.1. Circuit topology of the switched-capacitor inverter using series/parallel conversion.

A voltage source *Vin* is the input voltage source. A low pass filter is composed of an inductor L and a capacitor

C. There are many modulation methods to drive a multilevel inverter: the space vector modulation the multicarrier pulse width modulation (PWM) the hybrid modulation the selective harmonic elimination and the nearest level control In this paper, the multicarrier PWM method is applied to the proposed inverter.

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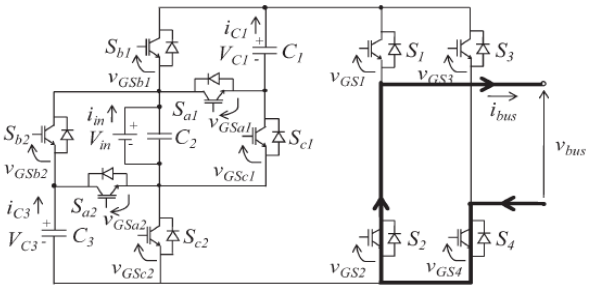
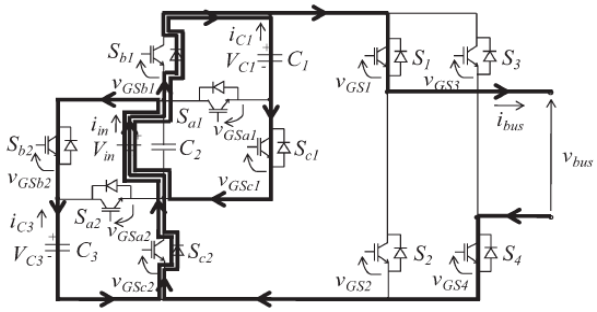
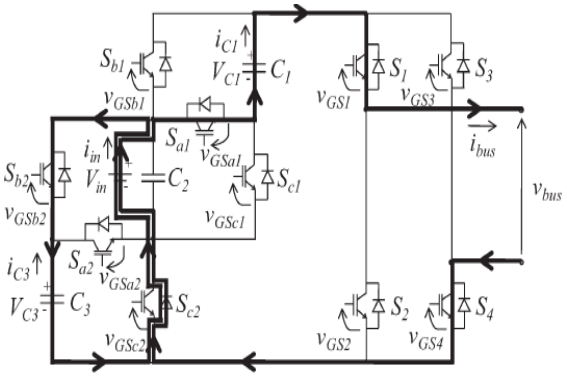


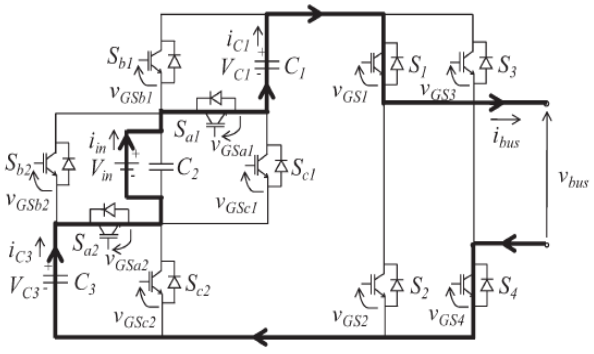
(a) The current *ibus* does not flow in the capacitors *Ck*,



(b) All capacitors are connected in Parallel.



(c) The capacitor *C*1 is connected in series and the capacitor *C*3 is connected in parallel.



(d) All capacitors are connected in series.

Fig.2. Current flow of the proposed inverter (*n* = 2) on each state of (a),(b),(c)and(d)

There are many modulation methods to drive a multilevel inverter: the space vector modulation the multicarrier pulse width modulation (PWM) the hybrid modulation the selective harmonic elimination and the nearest level control. In this paper, the multicarrier PWM method is applied to the proposed inverter. Fig. 2 shows the current flow in the proposed inverter (*n* = 2) and Fig. 3 shows the modulation method of the proposed inverter (*n* = 2).When the time *t* satisfies $0 \leq t < t1$ in Fig. 3, the switches *S*1 and *S*2 are driven by the gate-source voltage *vGS*1 and *vGS*2, respectively. While the switches *S*1 and *S*2 are switched alternately, the other switches are maintained ON or OFF state as shown in Fig. 3.

Therefore, the states shown in Fig. 2(a) and (b) are switched alternately and the bus voltage V*bus* takes 0 or *Vin*. When the time *t* satisfies $t1 \leq t < t2$ in Fig. 3, the switches *Sa*1, *Sb*1, and *Sc*1 are driven by the gate-source voltage *vGSa*1, *vGSb*1, and *vGSc*1, respectively. While the switches *Sa*1, *Sb*1, and *Sc*1 are switched alternately, the other switches are maintained ON or OFF state as shown in Fig.3.Therefore, the states shown in Fig. 2(b) and (c) are switched alternately. The capacitor *C*1 is charged by the current $-iC1$ as shown in
Fig. 2(b) during the state shown in Fig.2(b). Therefore, the proposed inverter can output the bus voltage *vbus* while the capacitor *C*1 is charged. The bus voltage *vbus* in the state of Fig. 2(c) is

$$v_{bus} = V_{in} + V_{C1} \quad (1)$$

III.MODULATION METHOD OF THE PROPOSED INVERTER

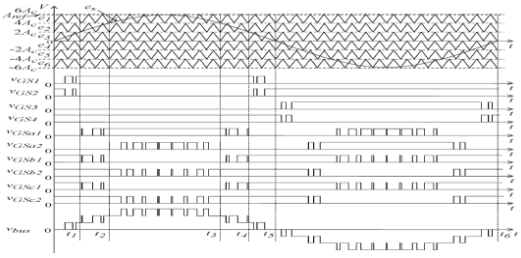


Fig.3. Modulation method of the proposed inverter (*n* = 2).

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Where *VC*1 is the voltage of the capacitor *C*1. Therefore, the proposed inverter outputs *Vin* or *Vin* + *VC*1 alternately in this term. When the time *t* satisfies $t2 \leq t < t3$ in Fig. 3, the switch *Sa*2, *Sb*2 and *Sc*2 are driven by the gate-source voltage *vGSa*2, *vGSb*2 and *vGSc*2, respectively. While the switches *Sa*2, *Sb*2, and *Sc*2 are switched alternately, the other switches are maintained ON or OFF state as shown in Fig. 3. Therefore, the states shown in Fig. 2(c) and (d) are switched alternately. The capacitor *C*3 is charged by the current $-iC3$ as shown in Fig. 2(c) during the state shown in Fig. 2(c). The bus voltage *vbus* in the state of Fig. 2(d) is

$$v_{bus} = V_{in} + V_{C1} + V_{C3} \tag{2}$$

Where *VC*3 is the voltage of the capacitor *C*3. Therefore, the proposed inverter outputs *Vin* + *VC*1 or *Vin* + *VC*1 + *VC*3 alternately in this term. After *t* = *t*3, the four states shown in Fig. 2 are repeated by turns. Table I shows the list of the on-state switches when the proposed inverter (*n* = 2) is driven by the modulation method shown in Fig. 3. The ideal bus voltage *vbus* in Table I means the bus voltage on each state when *VC*1 = *VC*3 = *Vin* is assumed.

As the conventional SC inverter, the proposed inverter has a full bridge which is connected to the high voltage.

TABLE I
LIST OF THE ON –STATE SWITCHES ON EACH STATE

Relationship between e_s and e_k	On-state switches	Ideal bus voltage v_{bus}
$e_s > e_1$	S_1, S_4, S_{a1}, S_{a2}	$3V_{in}$
$e_1 \geq e_s > e_2$	$S_1, S_4, S_{a1}, S_{b2}, S_{c2}$	$2V_{in}$
$e_2 \geq e_s > e_3$	$S_1, S_4, S_{b1}, S_{c1}, S_{b2}, S_{c2}$	V_{in}
$e_3 \geq e_s > e_4$	$S_2, S_4, S_{b1}, S_{c1}, S_{b2}, S_{c2}$	0
$e_4 \geq e_s > e_5$	$S_2, S_3, S_{b1}, S_{c1}, S_{b2}, S_{c2}$	$-V_{in}$
$e_5 \geq e_s > e_6$	$S_2, S_3, S_{b1}, S_{c1}, S_{a2}$	$-2V_{in}$
$e_6 \geq e_s$	S_2, S_3, S_{a1}, S_{a2}	$-3V_{in}$

Therefore, the device stress of the switches $S1 - S4$ in the full bridge is higher than the other switches as the conventional SC inverter. The proposed inverter (*n* = 2) outputs a 7-level voltage by repeating the four states as shown in Fig. 2. Because the driving waveform *vGSa*1 and *vGSa*2 change alternately as shown in Fig. 3, the capacitors *C*1 and *C*3 are equally discharged. Assuming that the number of the capacitors is $2n - 1$, the proposed inverter can outputs $4n - 1$ levels voltage waveform. The modulation index *M* is defined as the following equation because the amplitude of the output voltage waveform is inversely proportional to the double amplitude of the carrier waveform.

$$M = A_{ref}/2A_c. \tag{3}$$

In (3), *Aref* is the amplitude of the reference waveform and *Ac* is the amplitude of the carrier waveform. The proposed inverter requires 10 switching devices for the 7-level, and 16 switching devices for the 11-level. On the other hand, the conventional SC inverter requires 20 switching devices for the 7-level, and 28 switching devices for the 11-level [9]. The conventional cascaded H-bridge (CHB) inverter requires 12 switching devices for the 7-level, and 20 switching devices for the 11-level, when all the dc voltage sources take the same voltage. Therefore, the proposed inverter has less number of switching devices than the conventional multilevel inverters.

IV.DYNAMIC MODELLING OF INDUCTION MOTOR

In a conventional four pole induction motor, there are two sets of identical voltage profile windings will be present in the total phase winding. These two windings are connected in series as shown in fig. 4(a). For the proposed inverter these two identical voltage profile winding coils are disconnected, and the available four terminals are taken out, like shown in the fig.4 (b). Since these two windings are separated equally, stator resistance, Stator leakage inductance and the magnetizing inductance of each identical voltage profile windings are equal to the half of the normal induction motor shown in fig.4 (a). The voltage equitation for the stator winding is given by common dc link.

$$V_{a1} - V_{a2} = \left(\frac{r_s}{2}\right) * i_{as} + \left(\frac{L_{ss}}{2}\right) * i_{as} - \left(\frac{1}{2}\right) * \left(\frac{L_m}{2}\right) * i_{bs} - \left(\frac{1}{2}\right) * \left(\frac{L_m}{2}\right) * i_{cs} \tag{4}$$

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$$V_{a3} - V_{a4} = \left(\frac{r_s}{2}\right) * i_{as} + \left(\frac{L_{ss}}{2}\right) * i_{as} - \left(\frac{1}{2}\right) * \left(\frac{L_m}{2}\right) * i_{bs} - \left(\frac{1}{2}\right) * \left(\frac{L_m}{2}\right) * i_{cs} \quad (5)$$

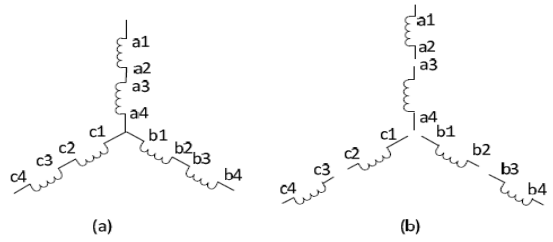

Fig. 4 Induction Motor stator winding: (a) General arrangement (b) Arrangement for the proposed inverter

The effective voltage across the stator winding is the sum of the voltages across the two individual windings.

$$V_{as} = (V_{a1} - V_{a2}) + (V_{a3} - V_{a4}) \quad (6)$$

The motor phase voltage can be achieved by substituting
equations (4) and (5) in (6)

$$V_{as} = r_s * i_{as} + L_{ss} * i_{as} - \left(\frac{1}{2}\right) * L_m * i_{bs} - \left(\frac{1}{2}\right) * L_m * i_{cs} \quad (7)$$

Similarly voltage equitation for the remaining phases are

$$V_{bs} = r_s * i_{bs} + L_{ss} * i_{bs} - \left(\frac{1}{2}\right) * L_m * i_{as} - \left(\frac{1}{2}\right) * L_m * i_{cs} \quad (8)$$

$$V_{cs} = r_s * i_{cs} + L_{ss} * i_{cs} - \left(\frac{1}{2}\right) * L_m * i_{as} - \left(\frac{1}{2}\right) * L_m * i_{bs} \quad (9)$$

Voltage equations in dq0 frame can be solved from the basic equations of induction motor

$$V_{qs} = r_s * i_{qs} + \omega * \lambda_{ds} + \rho * \lambda_{qs}$$

$$V_{ds} = r_s * i_{ds} - \omega * \lambda_{qs} + \rho * \lambda_{ds}$$

$$V_{0s} = r_s * i_{0s} + \rho * \lambda_{0s}$$

$$V_{qr} = r_r * i_{qr} + (\omega - \omega_r) * \lambda_{dr} + \rho * \lambda_{qr}$$

$$V_{dr} = r_r * i_{dr} - (\omega - \omega_r) * \lambda_{qr} + \rho * \lambda_{dr}$$

$$V_{0r} = r_r * i_{0r} + \rho * \lambda_{0r}$$

Flux linkages are as follows

$$\lambda_{qs} = L_{ss} * i_{qs} + L_M * i_{qr}$$

$$\lambda_{ds} = L_{ss} * i_{ds} + L_M * i_{dr}$$

$$\lambda_{0s} = L_{1s} * i_{0s}$$

$$\lambda_{qr} = L_{rr} * i_{qr} + L_M * i_{qs}$$

$$\lambda_{dr} = L_{rr} * i_{dr} + L_M * i_{ds}$$

$$\lambda_{0r} = L_{1r} * i_{0r}$$

The expression for the electromagnetic torque in terms of dq0 axis currents is

$$T_e = \left(\frac{3}{2}\right) * \left(\frac{P}{2}\right) * L_M * (i_{qs} * i_{dr} + i_{ds} * i_{qr}) \quad (10)$$

Rotor speed in terms of Torque is

$$\frac{d}{dt}\omega_e = \left(\frac{P}{2 * J}\right) * (T_e - T_L) \quad (11)$$

Where
d: direct axis,
q: quadrature axis,
s: stator variable,
r: rotor variable,
V_{ds}, V_{qs},: q and d–axis stator voltages,
V_{dr}, V_{qr},: q and d–axis rotor voltages,
r_r : Rotor resistance,
Vr_s : Stator resistance,
L1s: stator leakage inductance,
L1r : rotor leakage inductance,
iqs ,ids: q and d–axis stator currents,
iqr, idr: q and d–axis rotor currents,
p: number of poles,
J: moment of inertia,
Te: electrical output torque,
TL: load torque.
From the equations (4), (5),(6) it can be observed that there is no difference between the normal induction motor.

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V.SIMULATION RESULTS

Here simulation is carried out in different cases 1). Proposed Single Phase Series/Parallel Topology 2). Proposed single Phase Series/Parallel Topology Applied to Induction machine Drive.

Case 1: Proposed Single Phase Series/Parallel Topology

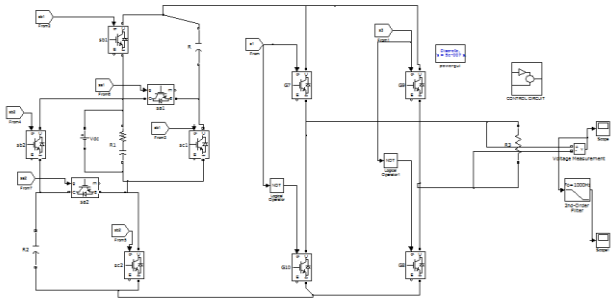

Fig. 5 Matlab/Simulink Model of Proposed Single Phase Series/Parallel Converter.

Fig.5 shows the Matlab/Simulink Model of Proposed Single Phase Series/Parallel Converter.

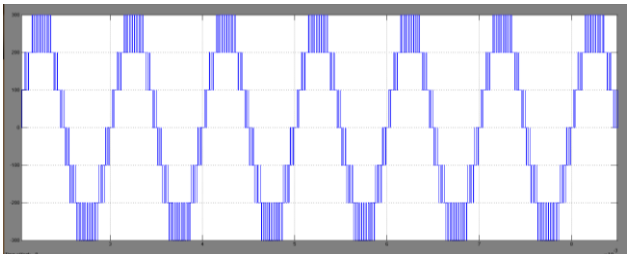

Fig. 6 Seven Level Output Voltage.

As Fig.6 shows the single phase seven level output voltage without filter of proposed series/parallel converter.

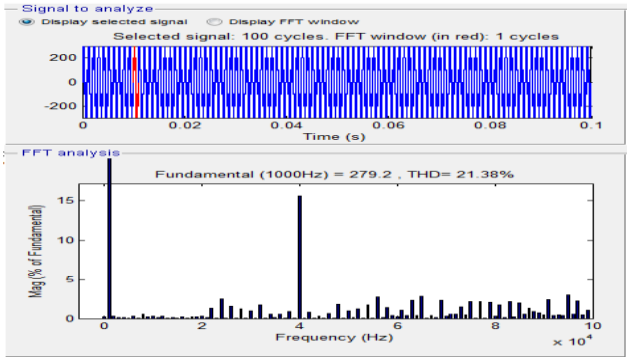

Fig. 7 FFT Analysis of Output Voltage without Filter of Proposed Series/Parallel Converter.

As above Fig. 7 shows the FFT Analysis of Output Voltage without Filter of Proposed Series/Parallel Converter, we get 21.38%.

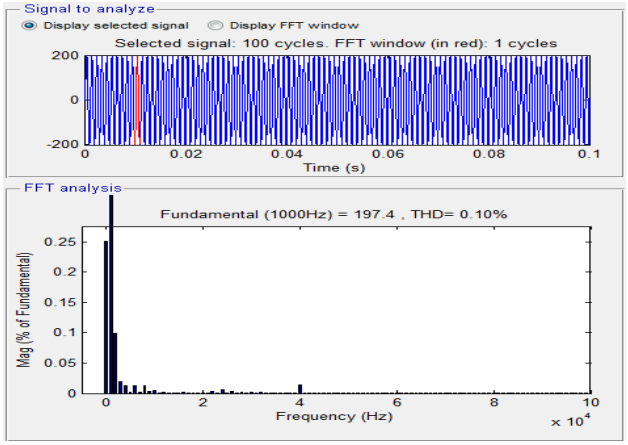

Fig. 8 FFT Analysis of Output Voltage with Filter of Proposed Series/Parallel Converter.

As above Fig. 8 shows the FFT Analysis of Output Voltage with Filter of Proposed Series/Parallel Converter, we get 0.10%.

Case 2: Proposed Series/Parallel Topology Applied to single phase Induction machine Drive.

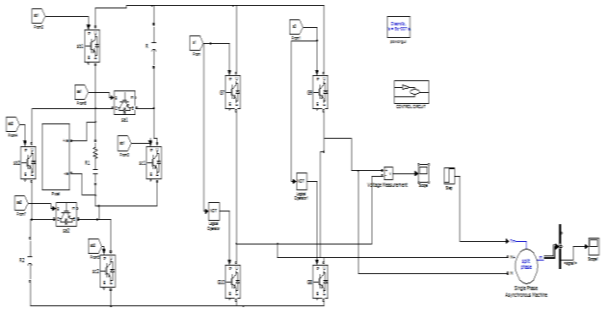

Fig. 9. Matlab/Simulink Model of Proposed Series/Parallel Converter Applied to Single phase IM Drive.

Fig.9. shows the Matlab/Simulink Model of Proposed Single Phase Series/Parallel Topology Applied to Induction machine Drive.

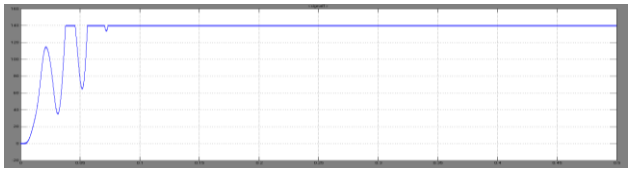

Fig.10. Speed.

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Fig.10.Speed of Proposed Single Phase Series/Parallel Topology Applied to Induction machine Drive.

VI.CONCLUSION

With the advancement of power electronics and emergence of new multilevel converter topologies, it is possible to work at voltage levels beyond the classic semiconductor limits. The multilevel converters achieve high-voltage switching by means of a series of voltage steps, each of which lies within the ratings of the individual power devices. In this paper, a novel boost switched-capacitor inverter was proposed & proposed three phase series/parallel topology applied to induction machine drive to check the performance of drive characteristics, the circuit topology was introduced. The open loop speed control was achieved by maintaining V/*f* ratio at constant value. The simulation results show that the proposed system effectively controls the motor speed and enhances the drive performance through reduction in total harmonic distortion (THD).

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