ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Data Conversion Techniques for Reducing Power Consumption in SOC/Network-on-Chip

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Abstract:

Power is one of the most important criterions in designing any modern system. As technology shrinks, the power dissipated by the links of a network-on-chip (NoC) starts to compete with the power dissipated by the other elements of the communication subsystem, namely, the routers and the network interfaces (NIs). A set of data encoding decoding schemes aimed at reducing the power dissipated by the links of an NoC is presented here. The proposed schemes are general and transparent with respect to the underlying NoC fabric (i.e., their application does not require any modification of the routers and link architecture). The idea presented, is based on encoding the packets before they are injected into the network in such a way as to minimize both the switching activity and the coupling switching activity in the NoC's links which represent the main factors of power dissipation. It is also possible to decode the data back at the receiver by using decoding schemes. Decoding schemes helps to recover the original data back at the receiver. These encoding and decoding schemes assures the secure transmission of data with less power consumption.

Key Words:
Network-on-Chip (NoC), data encoding, low power, coupling switching activity.

1. INTRODUCTION:

Networks-on-Chip (NoCs) are infrastructures essentially composed of routers interconnected by communication channels. Highly scalable modular structure of Network-on-Chips (NoCs) makes a fitting replacement for system-on-chip (SoCs) in designs incorporating large number of processing cores. Amongst the communication resources, as technology shrinks, the power ratio between NoC links and routers increases making the links becoming more power hungry than routers. Several encoding schemes have been proposed to reduce power in context of bus based architectures. Bus-invert method can be applied to encode randomly distributed data patterns. A few encoding techniques have been defined to take into consideration the contribution of cross coupled capacitance, the use of partial bus invert coding as link level low power encoding technique with the conclusion that it spends several times more power than no encoding at all, an end to end encoding technique has been suggested for reducing power dissipation. Here, a two stage coding scheme (TSC) for power reduction has been devised, considering both self switching activity and cross coupling effect.

The encoder and decoder structures are placed at the network interface level. The data packet passes through two stages of encoding before ensuring reduction in switching activity and crosstalk. First stage reorders and rearranges data in such a way that transition in each link is reduced. The second stage sends data as is or inverts the data entering each link, where the decision to invert the data is dependent on contribution of cross-coupled activity in the power dissipation of particular link. Shifting from a silicon technology node to the next one results in faster and more power efficient gates but slower and more power hungry wires. In fact, more than 50% of the total dynamic power is dissipated in interconnects in current processors, and this is expected to rise to 65%–80% over the next several years. Global interconnect length does not scale with smaller transistors and local wires.

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Chip size remains relatively constant because the chip function continues to increase and RC delay increases exponentially. At 32/28 nm, for instance, the RC delay in a 1-mm global wire at the minimum pitch is 25× higher than the intrinsic delay of a two-inputNAND fan-out of 5. If the raw computation horsepower seems to be unlimited, thanks to the ability of instancing more and more cores in a single silicon die, scalability issues, due to the need of making efficient and reliable communication between the increasing number of cores, become the real problem .

The network-on-chip (NoC) design paradigm is recognized as the most viable way to tackle with scalability and variability issues that characterize the ultra-deep sub micrometer era. Nowadays, the on-chip communication issues are as relevant as, and in some cases more relevant than, the computation related issues. In fact, the communication subsystem increasingly impacts the traditional design objectives, including cost (i.e., silicon area), performance, power dissipation, energy consumption, reliability, etc.

As technology shrinks, an ever more significant fraction of the total power budget of a complex many-core system-on-chip (SoC) is due to the communication subsystem. In this project, techniques aimed at reducing the power dissipated by the network links are focused. In fact, the power dissipated by the network links is as relevant as that dissipated by routers and network interfaces (NIs) and their contribution is expected to increase as technology scales. In particular, a set of data encoding schemes operating at flit level and on an end-to-end basis is presented, which allows us to minimize both the switching activity and the coupling switching activity on links of the routing paths traversed by the packets.

The encoding schemes, which are transparent with respect to the router implementation, are presented and discussed at both the algorithmic level and the architectural level, and assessed by means of simulation on synthetic and real traffic scenarios. The analysis takes into account several aspects and metrics of the design, including silicon area, power dissipation, and energy consumption. The results show that by using the proposed encoding schemes up to 51% of power and up to 14% of energy can be saved without any significant degradation in performance and with 15% area overhead in the NI.

2. OVERVIEW OF THE PROPOSAL:

The basic idea of the proposed approach is encoding the flits before they are injected into the network with the goal of minimizing the self-switching activity and the coupling switching activity in the links traversed by the flits. In fact, self-switching activity and coupling switching activity are responsible for link power dissipation. In this paper, we refer to the end-to-end scheme. This end-to-end encoding technique takes advantage of the pipeline nature of the wormhole switching technique [4]. Note that since the same sequence of flits passes through all the links of the routing path, the encoding decision taken at the NI may provide the same power saving for all the links. For the proposed scheme, an encoder and a decoder block are added to the NI. Except for the header flit, the encoder encodes the outgoing flits of the packet such that the power dissipated by the inter-router point-to-point link is minimized.

3. RELATED WORK:

The goal of encoding schemes is to reduce the power dissipation by minimizing the coupling transition activities on the links of the interconnection network. The power model that contains different components of power dissipation of a link is described here. The dynamic power dissipated by the interconnects and drivers is

$$P = [T0\rightarrow1\ (Cs + Cl\ ) + TcCc]\ V2ddFck \quad (1)$$

Where $T0\rightarrow1$ is the number of $0 \rightarrow 1$ transitions in the bus in two consecutive transmissions, Tc is the number of correlated switching between physically adjacent lines, Cs is the line to substrate capacitance, Cl is the load capacitance, Cc is the coupling capacitance, Vdd is the supply voltage, and Fck is the clock frequency.

One can classify four types of coupling transitions as described in . A Type I transition occurs when one of the lines switches when the other remains unchanged. In a Type II transition, one line switches from low to high while the other makes transition from high to low. A Type III transition corresponds to the case where both lines switch simultaneously. Finally, in a Type IV transition both lines do not change. The effective switched capacitance varies from type to type, and hence, the coupling transition activity, Tc, is a weighted sum of different types of coupling transition contributions.

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Here, the occurrence probability for different types of transitions is calculated. Consider that flit (t − 1) and flit (t) refer to the previous flit which was transferred via the link and the flit which is about to pass through the link, respectively. Now consider only two adjacent bits of the physical channel. Sixteen different combinations of these four bits could occur (Table I). Note that the first bit is the value of the generic ith line of the link, whereas the second bit represents the value of its (i +1)th line. The number of transitions for Types I, II, III, and IV are 8, 2, 2, and 4, respectively. For a random set of data, each of these sixteen transitions has the same probability. Therefore, the occurrence probability for Types I, II, III, and IV are 1/2, 1/8, 1/8, and 1/4, respectively. In the rest of this section, three data encoding schemes designed for reducing the dynamic power dissipation of the network links along with a possible hardware implementation of the decoder is presented.

TABLE I
EFFECT OF ODD INVERSION ON CHANGE OF TRANSITION TYPES

Time	Normal			Odd Inverted		
	Type I			Types II, III, and IV		
$t-1$	00, 11	00, 11, 01, 10	01, 10	00, 11	00, 11, 01, 10	01, 10
t	10, 01	01, 10, 00, 11	11, 00	11, 00	00, 11, 01, 10	10, 01
	T1*	T1**	T1***	Type III	Type IV	Type II
$t-1$	Type II			Type I		
t	01, 10			01, 10		
	10, 01			11, 00		
$t-1$	Type III			Type I		
t	00, 11			00, 11		
	11, 00			10, 01		
$t-1$	Type IV			Type I		
t	00, 11, 01, 10			00, 11, 01, 10		
	00, 11, 01, 10			01, 10, 00, 11		

TABLE II
EFFECT OF EVEN INVERSION ON CHANGE OF TRANSITION TYPES

Time	Normal			Even Inverted		
	Type I			Types II, III, and IV		
$t-1$	01, 10	00, 11, 01, 10	00, 11	01, 10	00, 11, 01, 10	00, 11
t	00, 11	10, 01, 11, 00	01, 10	10, 01	00, 11, 01, 10	11, 00
	T1*	T1**	T1***	Type II	Type IV	Type III
$t-1$	Type II			Type I		
t	01, 10			01, 10		
	10, 01			00, 11		
$t-1$	Type III			Type I		
t	00, 11			00, 11		
	11, 00			01, 10		
$t-1$	Type IV			Type I		
t	00, 11, 01, 10			00, 11, 01, 10		
	00, 11, 01, 10			10, 01, 11, 00		

4. ENCODING SCHEMES:

4.1. SCHEME 1:

In scheme I, we focus on reducing the numbers of Type I transitions (by converting them to Types III and IV transitions) and Type II transitions (by converting them to Type I transition). The scheme compares the current data with the previous one to decide whether odd inversion or no inversion of the current data can lead to the link power reduction.

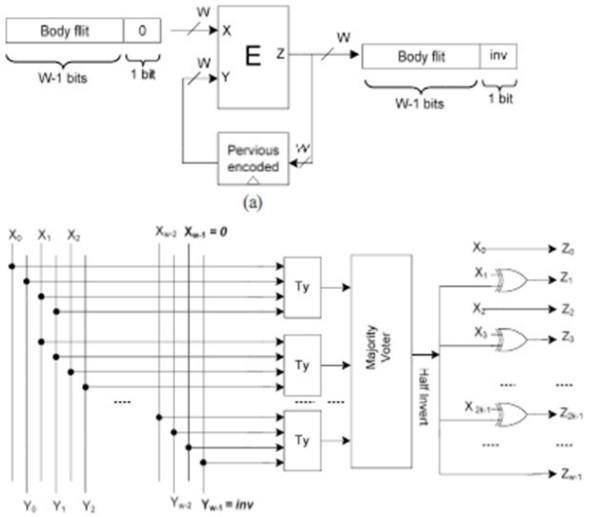

Fig. 1. Encoder architecture scheme 1. (a) Circuit diagram. (b) Internal view of the encoder block.

Scheme 1 Encoding Architecture:

The scheme I encoding architecture, which is based on the odd invert condition, is shown in Fig. 1. A link width of w bits is considered. If no encoding is used, the body flits are grouped in w bits by the NI and are transmitted via the link. In scheme I, one bit of the link is used for the inversion bit, which indicates if the flit traversing the link has been inverted or not. More specifically, the NI packs the body flits in w − 1 bits [Fig. 1(a)]. The encoding logic E, which is integrated into the NI, is responsible for deciding if the inversion should take place and performing the inversion if needed. The generic block diagram shown in Fig. 1(a) is the same for all three encoding schemes proposed in the project and only the block E is different for the schemes. To make the decision, the previously encoded flit is compared with the current flit being transmitted. This latter, whose w bits are the concatenation of w − 1 payload bits and a "0" bit, represents

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International Journal & Magazine of Engineering, Technology, Management and Research
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the first input of the encoder, while the previous encoded flit represents the second input of the encoder [Fig. 1(b)]. The w − 1 bits of the incoming (previous encoded) body flit are indicated by Xi (Yi), i = 0, 1, . . . ,w − 2. The wth bit of the previously encoded body flit is indicated by inv which shows if it was inverted (inv = 1) or left as it was (inv = 0). In the encoding logic, each Ty block takes the two adjacent bits of the input flits (e.g., X1X2Y1Y2, X2X3Y2Y3, X3X4Y3Y4, etc.) and sets its output to "1" if any of the transition types of Ty is detected. This means that the odd inverting for this pair of bits leads to the reduction of the link power dissipation (Table I). The Ty block may be implemented using a simple circuit. The second stage of the encoder, which is a majority voter block, determines if the condition given is satisfied (a higher number of 1s in the input of the block compared to 0s). If this condition is satisfied, in the last stage, the inversion is performed on odd bits. The decoder circuit simply inverts the received flit when the inversion bit is high.

4.2. SCHEME 2:

In the proposed encoding scheme II, we make use of both odd (as discussed previously) and full inversion. The full inversion operation converts Type II transitions to Type IV transitions. The scheme compares the current data with the previous one to decide whether the odd, full, or no inversion of the current data can give rise to the link power reduction.

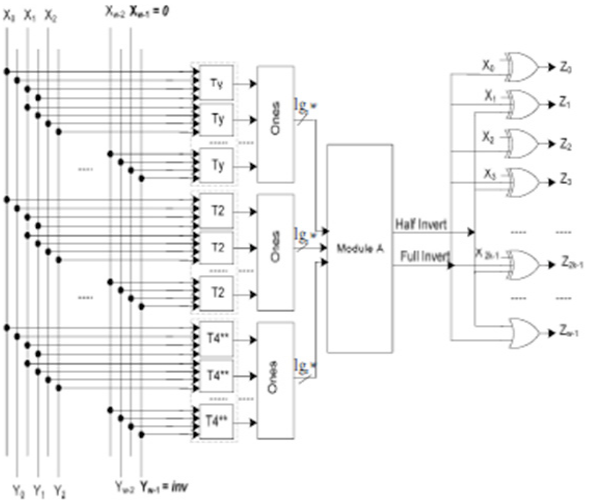

Fig.2. Encoder Architecture Scheme 2.

Scheme 2 Encoding Architecture:

The operating principles of this encoder are similar to those of the encoder implementing Scheme I. The scheme II encoding architecture, which is based on the odd invert condition and the full invert condition, is shown in Fig. 2. Here again, the wth bit of the previously encoded body flit is indicated with inv which defines if it was odd or full inverted (inv = 1) or left as it was (inv = 0). In this encoder, in addition to the Ty block in the Scheme I encoder, we have the T2 and blocks which determine if the inversion based on the transition types T2 and should be taken place for the link power reduction. The second stage is formed by a set of 1s blocks which count the number of 1s in their inputs.

The output of these blocks has the width of log2 w. The output of the top 1s block determines the number of transitions that odd inverting of pair bits leads to the link power reduction. The middle 1s block identifies the number of transitions whose full inverting of pair bits leads to the link power reduction. Finally, the bottom 1s block specifies the number of transitions whose full inverting of pair bits leads to the increased link power. Based on the number of 1s for each transition type, Module A decides if an odd invert or full invert action should be performed for the power reduction. In case no invert action should be taken place, none of the output is set to "1." Module A can be implemented using full-adder and comparator blocks.

4.3. SCHEME 3:

In the encoding Scheme III, even inversion to Scheme II is added. The reason is that odd inversion converts some of Type I transitions to Type II transitions. As can be observed from Table II, if the flit is even inverted, the transitions indicated as in the table are converted to Type IV/ Type III transitions. Therefore, the even inversion may reduce the link power dissipation as well. The scheme compares the current data with the previous one to decide whether odd, even, full, or no inversion of the current data can give rise to the link power reduction.

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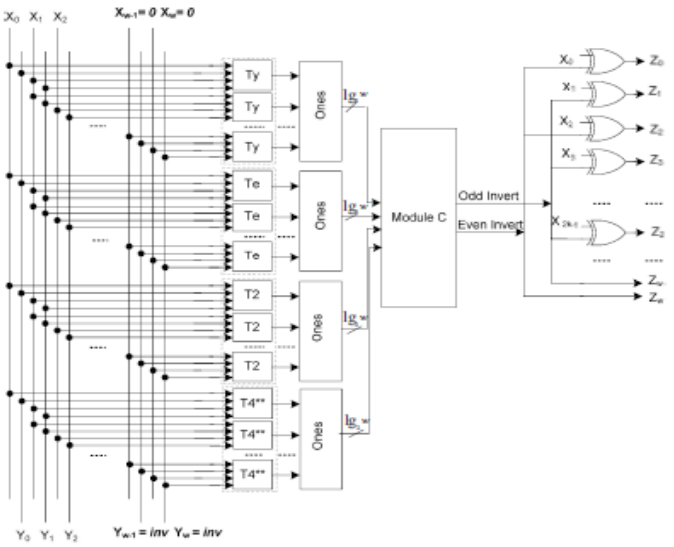

Fig.3. Encoder Architecture Scheme 3.

Scheme III Encoding Architecture: The operating principles of this encoder are similar to those of the encoders implementing Schemes I and II. The proposed encoding architecture, which is based on the even invert condition, the full invert condition, and the odd invert condition, is shown in Fig. 4. The wth bit of the previously encoded body flit is indicated by inv which shows if it was even, odd, or full inverted (inv = 1) or left as it was (inv = 0). The first stage of the encoder determines the transition types while the second stage is formed by a set of 1s blocks which count the number of ones in their inputs. In the first stage, the Te block is added which determine if any of the transition types of T2, , and is detected for each pair bits of their inputs.

For these transition types, the even invert action yields link power reduction. Again, we have four Ones blocks to determine the number of detected transitions for each Ty, Te, T2, , blocks. The output of the Ones blocks are inputs for Module C. This module determines if odd, even, full, or no invert action corresponding to the outputs "10,""01," "11," or "00," respectively, should be performed. Similar to the procedure used to design the decoder for scheme II, the decoder for scheme III can be designed.

5. DECODING SCHEMES:

The generic circuit diagram of decoder is shown in fig.4 below.

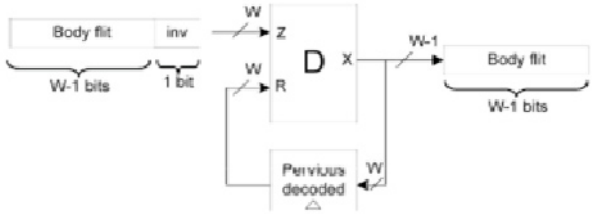

Fig.4 Generic circuit diagram of decoder.

The circuit diagram of decoder for all the schemes remains same. The internal block diagram of block D of decoder circuit changes according to each scheme.In decoders the inverse operation of encoder takes place. There is need of only one block Ty to determine which action has to be taken.

5.1. SCHEME 1:

The internal block diagram for block D in the generic circuit diagram for scheme 1 is as shown below.

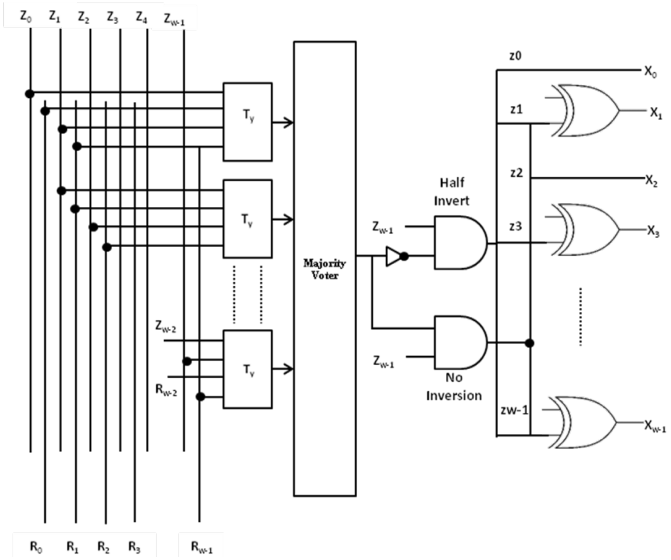

Fig.5. Decoder Architecture Scheme 1.

The wth bit of the body flit is indicated by inv which shows if it was inverted (inv = 1) or left as it was (inv = 0) i.e. no inversion has taken place. For the decoder, we only need to have the Ty block to determine which action has been taken place in the encoder. Based on the outputs of these blocks, the majority voter block checks the validity of the inequality. If the output is "1" ("0") and the inv = 0, it means that half (no) inversion of the bits has been performed.

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5.2. SCHEME 2:

The internal block diagram for block D of scheme 2 decoder is shown below.

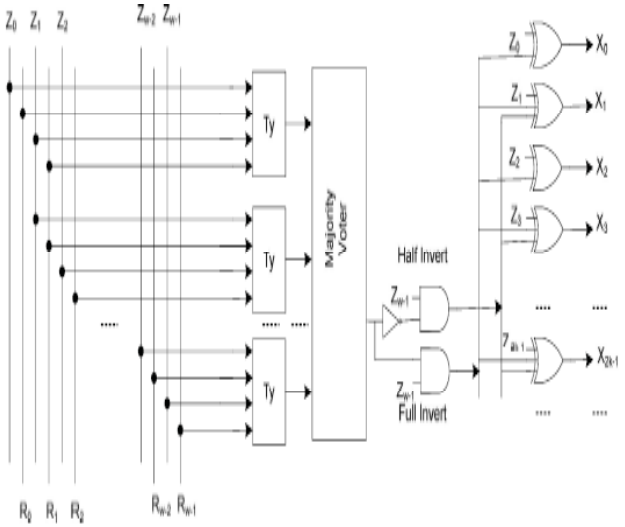

Fig.6. Decoder Architecture Scheme 2.

The w bits of the incoming (previous) body flit are indicated by Zi (Ri), i = 0, 1, . . . ,w − 1. The wth bit of the body flit is indicated by inv which shows if it was inverted (inv = 1) or left as it was (inv = 0). For the decoder, we only need to have the Ty block to determine which action has been taken place in the encoder.

Based on the outputs of these blocks, the majority voter block checks the validity of the inequality. If the output is "0" ("1") and the inv = 1, it means that half (full) inversion of the bits has been performed. Using this output and the logical gates, the inversion action is determined. If two inversion bits were used, the overhead of the decoder hardware could be substantially reduced.

5.3. SCHEME 3:

The internal block diagram for block D in the generic circuit diagram for scheme 3 is as shown below.

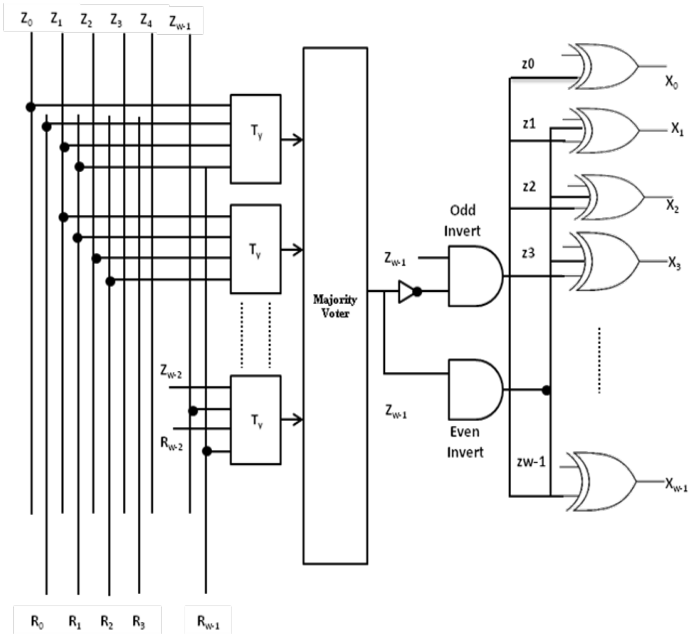

Fig.7. Decoder Architecure Scheme 3.

The wth bit of the body flit is indicated by inv which shows if it was inverted (inv = 1) or left as it was (inv = 0) i.e. no inversion has taken place. For the decoder, we only need to have the Ty block to determine which action has been taken place in the encoder. Based on the outputs of these blocks, the majority voter block checks the validity of the inequality. If the output is "1" ("0") and the inv = 1, it means that even (odd) inversion of the bits has been performed.

6. EXPERIMENTAL RESULTS:

By simulation and synthesis the following results are obtained for each scheme. Here Xilinx tool is used in order to synthesize and simulate the design process and also the netlist generation.

A. Simulation Results:

Fig.8. shows the simulation result of scheme 1 encoder architecture.

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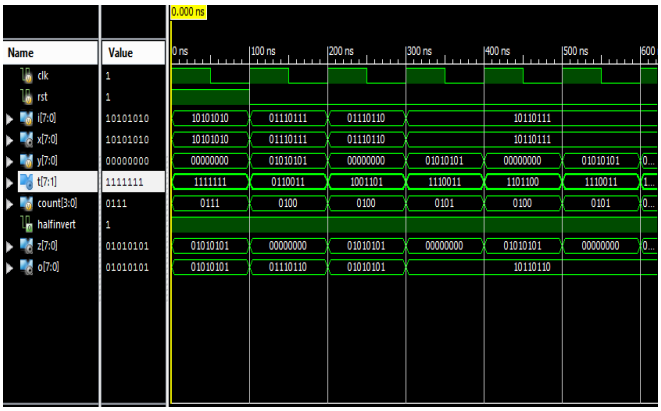


Fig.8. Scheme 1 Encoder.

Encoder Scheme 2:

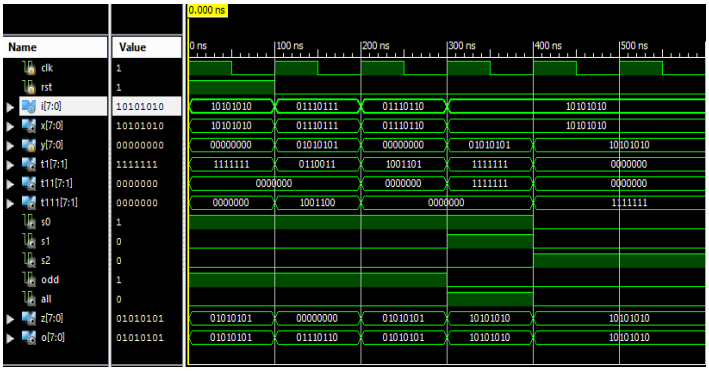


Fig.7. Scheme 2 Encoder.

Encoder Scheme 3:

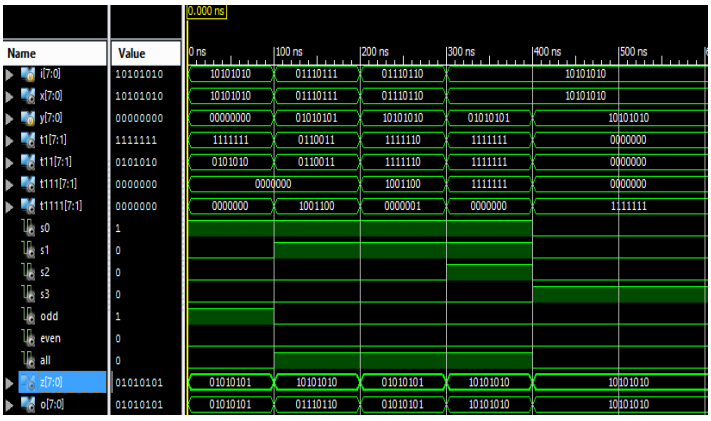


Fig.8. Scheme 3 Encoder.

Decoder Scheme 1:

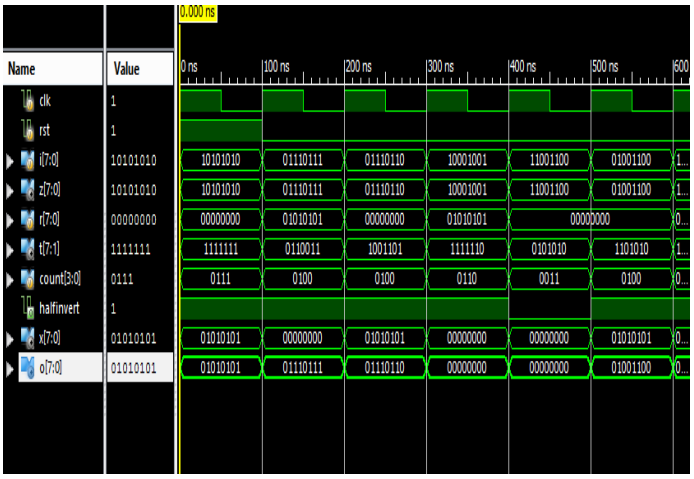
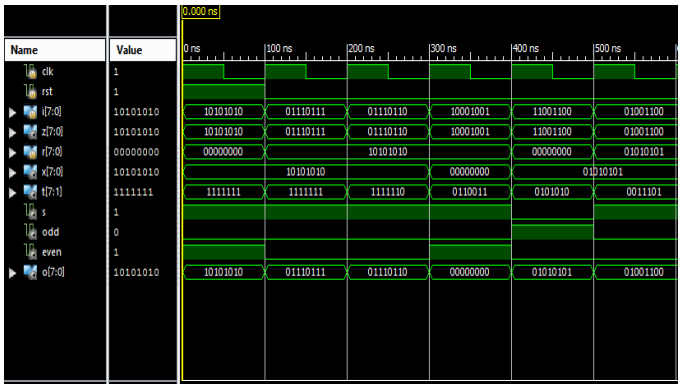


Fig.9. Scheme 1 Decoder.



Decoder Scheme 2:

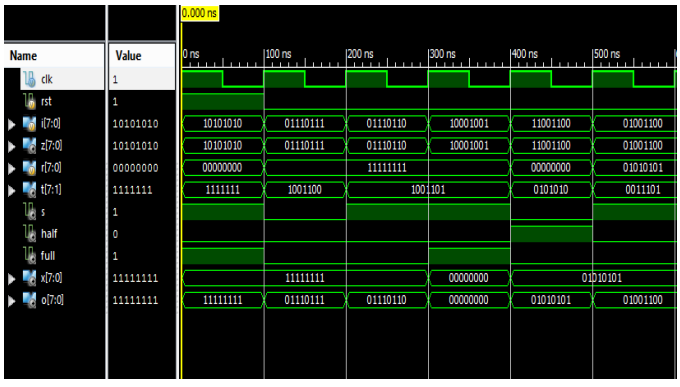


Fig.10. Scheme 2 Decoder.

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Decoder Scheme 3:

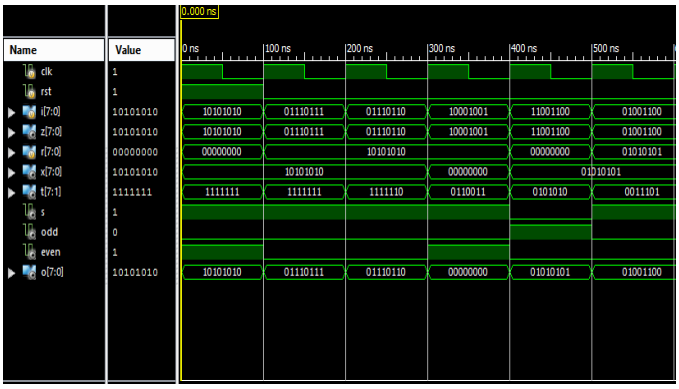

Fig.11. Scheme 3 Decoder

Area Report:
Encoder Area Report

```
Device utilization summary:
---------------------------

Selected Device : 6slx16csg324-2


Slice Logic Utilization:
 Number of Slice Registers:              4  out of  18224     0%
 Number of Slice LUTs:                  36  out of   9112     0%
    Number used as Logic:               36  out of   9112     0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:    37
   Number with an unused Flip Flop:     33  out of     37    89%
   Number with an unused LUT:            1  out of     37     2%
   Number of fully used LUT-FF pairs:    3  out of     37     8%
   Number of unique control sets:        1

IO Utilization:
 Number of IOs:                        18
 Number of bonded IOBs:                18  out of    232     7%

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:              1  out of     16     6%
```

Fig.12. Encoder Area Report

Decoder Area Report

```
Device utilization summary:
---------------------------

Selected Device : 6slx16csg324-2


Slice Logic Utilization:
 Number of Slice Registers:              2  out of  18224     0%
 Number of Slice LUTs:                  22  out of   9112     0%
    Number used as Logic:               22  out of   9112     0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:    22
   Number with an unused Flip Flop:     20  out of     22    90%
   Number with an unused LUT:            0  out of     22     0%
   Number of fully used LUT-FF pairs:    2  out of     22     9%
   Number of unique control sets:        1

IO Utilization:
 Number of IOs:                        18
 Number of bonded IOBs:                18  out of    232     7%

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:              1  out of     16     6%
```

Fig.13. Decoder Area Report

Timing Report:
Encoder Timing Report

```
Timing Summary:
---------------
Speed Grade: -2

   Minimum period: 5.624ns (Maximum Frequency: 177.809MHz)
   Minimum input arrival time before clock: 6.668ns
   Maximum output required time after clock: 9.247ns
   Maximum combinational path delay: 10.291ns
```

Fig.14. Encoder Area Report

Decoder Timing Report

```
Timing Summary:
---------------
Speed Grade: -2

   Minimum period: 1.723ns (Maximum Frequency: 580.383MHz)
   Minimum input arrival time before clock: 5.804ns
   Maximum output required time after clock: 6.337ns
   Maximum combinational path delay: 10.418ns
```

Fig.15. Decoder Timing Report

7. CONCLUSION:

A set of data encoding and decoding schemes aimed at reducing the power dissipated by the links of an NoC has been proposed in this paper. In fact, links are responsible for a significant fraction of the overall power dissipated by the communication system. In addition, their contribution is expected to increase in future technology nodes. The rationale behind the proposed schemes is to minimize not only the switching activity, but also the coupling switching activity which is mainly responsible for link power dissipation in the deep submicronmeter technology regime. The proposed encoding schemes are agnostic with respect to the underlying NoC architecture in the sense that their application does not require any modification neither in the routers nor in the links. An extensive evaluation has been carried out to assess the impact of the encoder and decoder logic in the NI. The encoders implementing the proposed schemes have been assessed in terms of power dissipation and silicon area. The decoders are implemented to perform the reverse operation of encoders and hence to recover the data.

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ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
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