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A PV System with Transistor Clamped H- Bridge Based Cascaded Multilevel Inverter -MPPT Implementation

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ABSTRACT:

Multilevel inverter is one of the most recent and popular type of inverter founds its applications in the system based on renewable energy. This paper describes a transistor-clamped h-bridge multilevel inverter for PV application with new method of capacitor voltage balancing. Multi-carrier phase-shifted pulse-width modulation method is used to achieve balanced power distribution among the power cells. A new method to balance the midpoint capacitor voltage in each cell is developed and tested. The analysis of the output voltage harmonics and the total power losses covering the conduction and the switching power losses are carried out and this inverter is fed from a solar PV. Simulation work is done using the MATLAB/ SIMULINK software which validates the proposed method and finally Total Harmonic Distortion is analyzed.

Index Terms:

Cascaded neutral-point clamped inverter, five-level inverter, multicarrier phase-Shifted pulse-width modulation (CPS-PWM), multilevel inverter, transistor-clamped converter.

I.INTRODUCTION:

In recent years, solar-energy power-generation systems have increased significantly their capacity. Nowadays Photovoltaic growth is gradually increased in India. Multilevel inverters are mainly utilized to synthesis a desired single or three phase voltage waveform. The desired multi-staircase output voltage is obtained by combining several dc voltage sources. Solar cells, fuel cells, batteries and ultra-capacitors are the most common independent sources used.

One important application of multilevel converters is focused on medium- and high-power conversion. Nowadays, there exist three commercial topologies of multilevel voltage-source inverters: Neutral Point Clamped (NPC), Cascaded H-Bridge (CHB), and Flying Capacitors (FCs). Among these inverter topologies, cascaded H-bridge inverter reaches the elevated output voltage & power levels and the higher reliability due to its modular topology. Diode-clamped multilevel inverters are complicates the design and raises reliability and cost concern. They are also utilized in oil mills, metal works places, power generations, mining process and chemical industry. They have been reported to be used in a back-to-back configuration for regenerative applications. Flying capacitor multilevel converters have been used in high-bandwidth high-switching frequency applications [5]. Finally, cascaded H-bridge multilevel inverter has been used for both high power and medium power application. Furthermore, one of the growing applications of cascade H-bridge multilevel inverter is used in Uninterruptible Power Supplies (UPS) and PV [3].For increasing voltage levels the number of switches also will increase in number. Hence the voltage stresses and switching losses will increase and the circuit was becomes complex. By using the proposed topology number of switches will reduce significantly and hence the efficiency will improve.

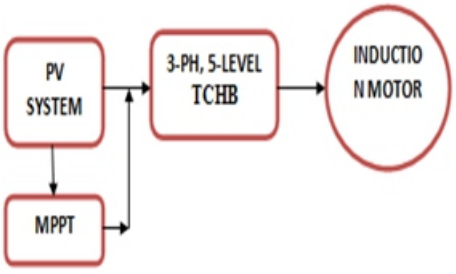

Fig .1 .Proposed system block diagram

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In this paper, the proposed inverter is evaluated for medium voltage drive application, in which based on the standard voltages, 2.3 kV to 13.8 kV and the power range 400 kW to 40 MW [36]. With more output levels, in addition to better output quality, the possibility of motor insulation failure as a result of steep voltage wave fronts (dv/dt) across the motor terminals is reduced, compared to the conventional CHB with similar cell configuration [29]. Focus was more on constant speed drive applications such as fans, blowers, pumps, and compressors, since these comprise 97% of currently installed medium-voltage drives [37]. It is found in various industries such as production plants, process industries, as well as in the oil and gas sectors. Simulation and experimental results are presented for verification.

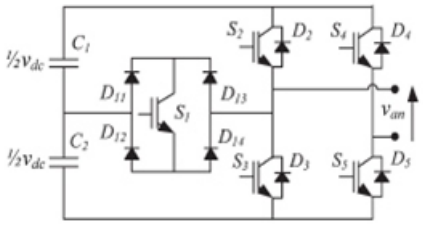

Fig. 2: five-level transistor-clamped H-bridge for each cell.

II. MODELING OF THE SOLAR CELL:

Thus the simplest equivalent circuit of a solar cell is a current in parallel with a diode. The output of the current source is directly proportional to the light falling on the cell. During darkness, the solar cell is not an active device; it works as a diode, i.e. a P-N junction. It produces neither a current nor a voltage. However, if it is connected to an external supply (large voltage) it generates a current Id, called diode current or dark current. The diode determines the V-I characteristics of the cell.

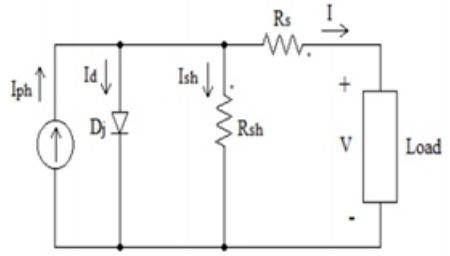

Fig. 3.Equivalent Circuit of a Solar Cell

Fig. 3 shows the equivalent circuit of a solar cell, where, RS is the very small series resistance and Rsh is the quite large shunt resistance.

Dj is the ideal P-N diode, Iph expresses as the photocurrent source generated proportionally by the surface temperature and insolation. V and I represent the output voltage and output current of the solar cell, respectively. According to the physical property of the P-N semiconductor, the I-V characteristics of PV module could be expressed.

$$I\left(1+\frac{Rs}{Rsh}\right)=\eta_p I_{ph}-\eta_p I_{sat}\left[exp\left\{\left(\frac{q}{AkT}\right)\left(\frac{V}{n_s+IR_s}\right)\right\}-1\right]-\frac{(V-n_s)}{R_{sh}} \quad (1)$$

In addition, the modules reverse saturation current Isat.

$$I_{sat}=I_{rr}\left(\frac{T}{T_r}\right)^3 exp\left\{\frac{q\,E_{gap}}{kA}\left(\frac{1}{T_r}-\frac{1}{T}\right)\right\} \quad (2)$$

The Iph is expressed in (3) represents the photocurrent proportionally produced to the level of cell surface temperature and radiation, where ISSO is the short-circuit current, Ki is the short circuit current temperature coefficient, and Si is the solar radiation in W/m 2 [3].

$$I_{ph}=\{I_{sso}+k_i(T-T_r)\}\frac{S_i}{1000} \quad (3)$$

2.1 Maximum Power Point Tracking Method

The change of environment condition would affect the output power of the PV array. By installing the MPPT in the PV system, it is possible to always ensure the maximum output power under the corresponding environment condition. There are many MPPT algorithms proposed in the research publications. The Perturbation & Observation (P&O) method will be presented. Figure 4.shows the characteristic power curve for a PV array. This characteristic curve would change for different environment conditions. Then the core idea of the MPPT technique is to automatically adjust its output voltage and current in terms of VMP P and IMP P under which the PV array can output the maximum power.

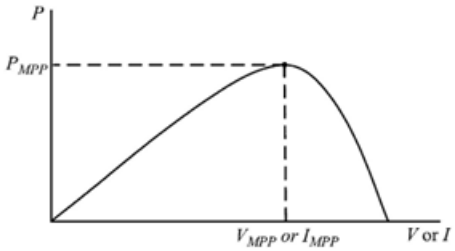

Fig. 4. Characteristic PV array power curve

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In Perturbation & Observation method, the operating voltage of the PV array is the value which is to be increased or decreased in the MPPT [15]. In Figure 4, it can be seen that when the operating points are on the left side of the MPP, increasing the operating voltage of the PV array would increase the output power and decreasing the operating voltage would decrease the output power. However, when the operating point are on the right side of MPP, increasing the operating voltage of the PV array would reduce the output power and decreasing the operating voltage of the PV array would increase the output power. Hence, it would be kept the same if the output power is increased while the direction of the perturbation should be changed if the output power is decreased. The algorithm is shown in Table 1.

Perturbation	Power	Next Perturbation
Increasing	Increasing	Increasing
Increasing	Decreasing	Decreasing
Decreasing	Increasing	Decreasing
Decreasing	Decreasing	Increasing

Table 1. Algorithm

When the operating voltage reaches MPP; it will oscillate around the MPP. The selection of the perturbation size is just the tradeoff between this oscillation and the response time of the MPPT. By using small perturbation size, the oscillation around MPP would be very small but the response time of MPPT would be very long. Some solutions for this problem have already be proposed. For example, in [16], [17], the perturbation size can adjust automatically which ensure large perturbation size far way from MPP and relatively small perturbation size around MPP.

2.1.1. BOOST Converter :

The boost converter topology sketch, inductor L1 charges when Q1 turns on. When Q1 turns off, L1 discharges into the battery via D1. Performing this simple operation thousands of times per second results in appreciable output current. It is also called inductive discharge. For this to function, the input voltage must be lower than the output voltage. Also, with a solar panel source, energy storage in the form of a capacitor (C1) is required so that the solar panel may continue to output current between cycles.

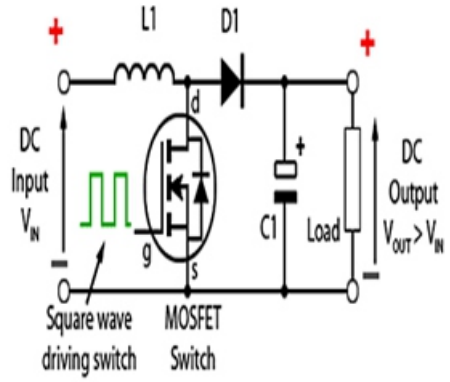

Fig. 5: Booster regulator for mppt.

III. PROPOSED INVERTER CONFIGURATION:

Fig. 6 is the general configuration of the proposed inverter, comprising Nc series-connected five-level TCHB cells.

S_1	S_2	S_3	S_4	S_5	v_{an}
0	1	0	0	1	v_{dc}
1	0	0	0	1	$\frac{1}{2}v_{dc}$
0	0 or 1	1 or 0	0 or 1	1 or 0	0
1	0	0	1	0	$-\frac{1}{2}v_{dc}$
0	0	1	1	0	$-v_{dc}$

(Switch ON = 1, Switch OFF = 0)

Table2. Five-level transistor-clamped h-bridge output voltage

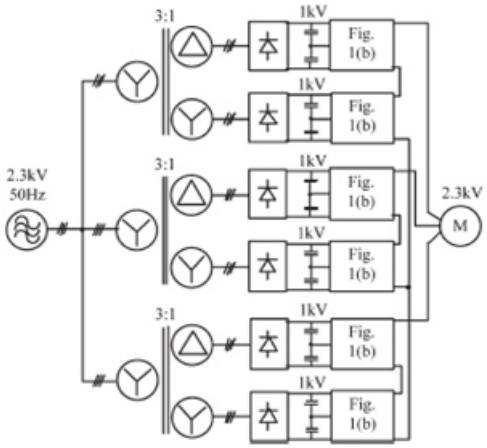

Fig. 6: Basic configuration for medium-voltage drive application.

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Fig. 2 shows the cell with the additional one bidirectional switch connected between the first leg of the H-bridge and the capacitor midpoint, enabling five output voltage levels (±Vdc,±(1/2)Vdc, 0) to be produced based on the switch combinations given in Table 2. The basic configuration for a 2.3-kV medium-voltage drive is shown in Fig. 6 where each power switch is a single 1.7-kV IGBT. The number of power cells required depends mainly on the operating voltage and production cost. In this case, a two-cell configuration is sufficient to produce a high-quality output with up to 17-voltage levels.In general, the maximum levels in the phase and line voltages of the proposed inverter, based on NC cells, are given by the following equations:

$$np = 4NC + 1 \quad (4)$$
$$nl = 8NC + 1. \quad (5)$$

Based on valid switch combinations, S1 − S5 in Table 2, the cell output voltage van can be represented by

$$Van = Vdc\ (S5n-S4n)\ \{1/2\ S1n+|S2n-S4n|.|S3n-S5n|\} . \quad (6)$$

Summation of all the power cell voltages gives the phase-to neutral voltage, Van and line voltage, Vab, respectively, as

$$v_{aN} = \sum_{n=1}^{N_C} v_{an} \quad (7)$$
$$v_{ab} = v_{aN} - v_{bN} . \quad (8)$$

IV. PWM MODULATION STRATEGY:

The modulation index M of the proposed multilevel inverter is defined by

$$M = \frac{1}{2}\frac{V_{ref}}{V_{Cr}} \quad (9)$$

where Vref is the amplitude of the voltage reference and Vcr is the amplitude of the carrier signal.Multicarrier phase-shifted PWM (CPS-PWM) modulation is used to generate the PWM signals. The amplitude and frequency of all triangular carriers are the same as well as the phase shifts between adjacent carriers. Depending on the number of cells, the carrier phase shift for each cell θCr,n can be obtained from

$$\theta_{Cr,n} = \frac{2\pi(n-1)}{N_C}, \quad n = 1, 2 \ldots N_C. \quad (10)$$

For signal generation in each cell, two voltage references and one carrier signal are used [18]. The references, Vref1 and Vref2 are derived from a full-wave voltage reference, Vref defined by

$$Vref = M \sin \omega t \quad (11)$$
$$Vref1 = |Vref| \quad (12)$$
$$Vref2 = Vref1 - 1/2. \quad (13)$$

Both references are identical but displaced by an offset equal to the carrier's amplitude which is 1/2. When the voltage reference is between $0 < Vref \leq (1/2)$, Vref1 is compared with the triangular carrier and alternately switches S1 and S3 while maintaining S5 in the ON state to produce either (1/2)Vdc or 0.Whereas, when the reference is between $(1/2) < Vref \leq 1$, Vref2 is used and alternately switches S1 and S2 while maintaining S5 in the ON state to produce either (1/2)Vdc or Vvdc. As for the reference between $-(1/2) < Vref \leq 0$, vref1 is used for comparison which alternately switches S1 and S2 while maintaining S4 in the ON state to produce either −(1/2)Vdc or 0. For a voltage reference between $-1 < Vref \leq -(1/2)$, vref2 is compared with the carrier to produce either −(1/2)Vdc or −Vdc alternately switches S1 and S3, maintaining S4 in the ON state. It is noted that two switches, S4 and S5, only operate in each reference half cycle. This implies that both switches operate at the fundamental frequency while the others operate close to the carrier frequency. This allows the dc voltage to be switched at a low frequency so as to reduce the switching losses.

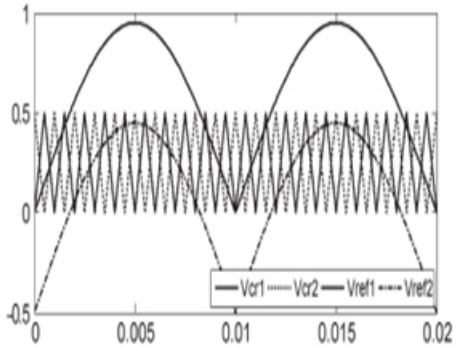

Fig. 7. Multicarrier phase-shifted PWM for two-cell configuration

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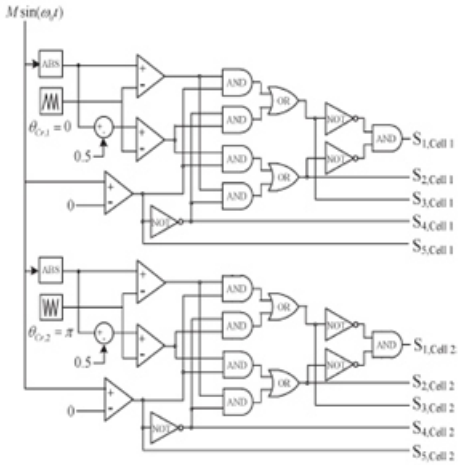

Fig. 8. PWM signal generation with multicarrier phase-shifted modulation for phase a

	v_{a1}	v_{a2}	v_{aN}
$0<v_{ref}\leq 1/2$	0	0	0
	$\frac{1}{2}v_{dc}$	0	$\frac{1}{2}v_{dc}$
	0	$\frac{1}{2}v_{dc}$	$\frac{1}{2}v_{dc}$
	$\frac{1}{2}v_{dc}$	$\frac{1}{2}v_{dc}$	v_{dc}
$1/2<v_{ref}\leq 1$	$\frac{1}{2}v_{dc}$	$\frac{1}{2}v_{dc}$	v_{dc}
	v_{dc}	$\frac{1}{2}v_{dc}$	$\frac{3}{2}v_{dc}$
	$\frac{1}{2}v_{dc}$	v_{dc}	$\frac{3}{2}v_{dc}$
	v_{dc}	v_{dc}	$2v_{dc}$
$-1/2<v_{ref}\leq 0$	0	0	0
	$-\frac{1}{2}v_{dc}$	0	$-\frac{1}{2}v_{dc}$
	0	$-\frac{1}{2}v_{dc}$	$-\frac{1}{2}v_{dc}$
	$-\frac{1}{2}v_{dc}$	$-\frac{1}{2}v_{dc}$	$-v_{dc}$
$-1<v_{ref}\leq -1/2$	$-\frac{1}{2}v_{dc}$	$-\frac{1}{2}v_{dc}$	$-v_{dc}$
	$-v_{dc}$	$-\frac{1}{2}v_{dc}$	$-\frac{3}{2}v_{dc}$
	$-\frac{1}{2}v_{dc}$	$-v_{dc}$	$-\frac{3}{2}v_{dc}$
	$-v_{dc}$	$-v_{dc}$	$-2v_{dc}$

Table 3.Phase-to-neutral voltage for two-cell configuration.

Fig. 7 shows the modulation scheme used for the proposed two-cell configuration and Fig. 8 shows a detail block diagram for generating the PWM signals. The phase-to-neutral voltage Van obtained based on the voltage reference magnitude and the combination of cell voltages, va1 and va2, are listed in Table 2.From Table 3, a total of nine-levels (±2Vdc,±(3/2)Vdc, ±Vdc,±(1/2)Vdc, 0) phase-to-neutral voltages are produced when both cells are cascaded with CPS-PWM modulation. When Vref is within 0 < Vref ≤ (1/2), each cell can only produce 0 or (1/2)Vdc; therefore, Van has three possible outputs which are 0, (1/2)Vdc, and Vdc. In the case of (1/2)<Vref ≤1, each cell can produce either (1/2)vdc or vdc which result in three possible vaN outputs also, vdc, (3/2)vdc, and 2vdc. For negative vref , the outputs are similar but with the opposite polarity. As the phase voltages are displaced by (2/3)π from each other, higher levels of line voltages will be generated where for vab, obtainable from (5).

SIMULATION RESULTS:

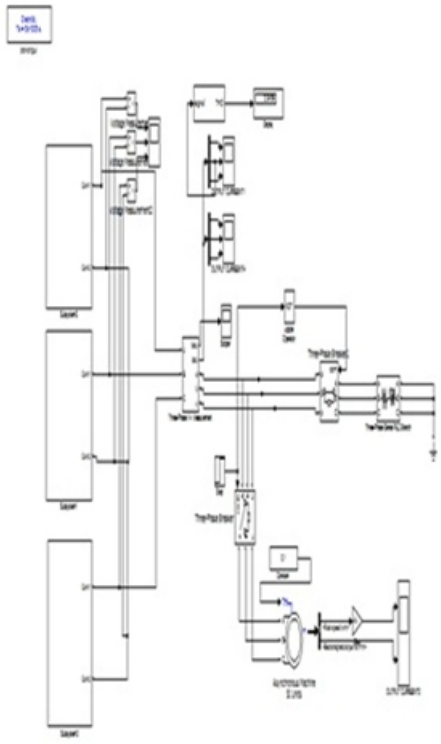

Fig 9.Simulation circuit

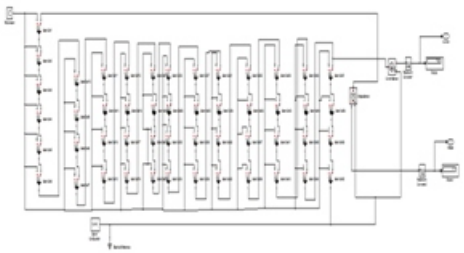

Fig 10.Solar System

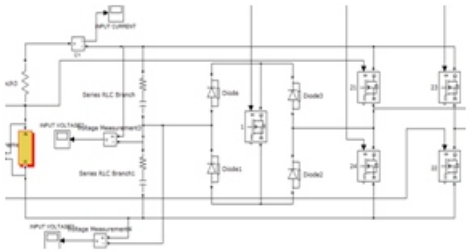

Fig 11.Five-level transistor-clamped H-bridge

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WAVE FORMS:

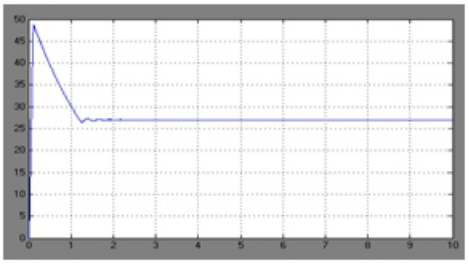

Fig 12.Solar output voltage

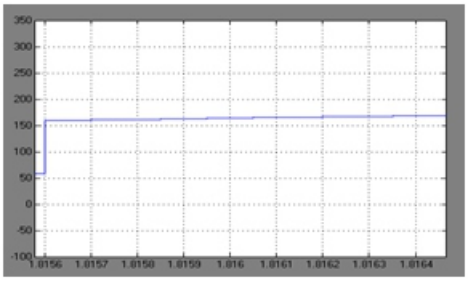

Fig 13.Solar output current

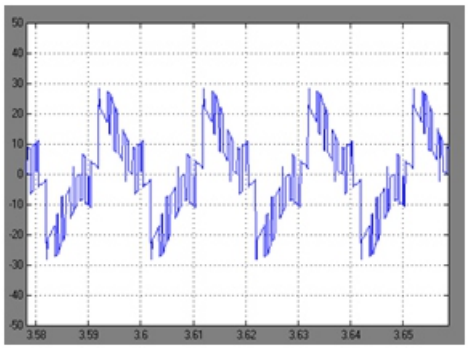

Fig 14.Output voltage Van

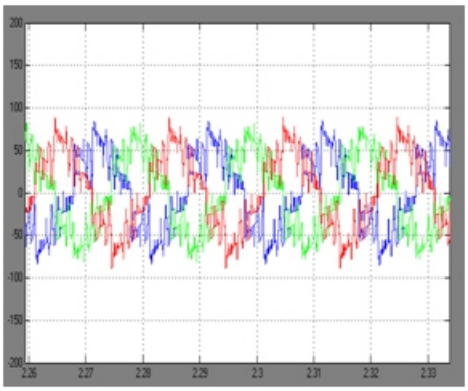

Fig 15.Output phase voltages

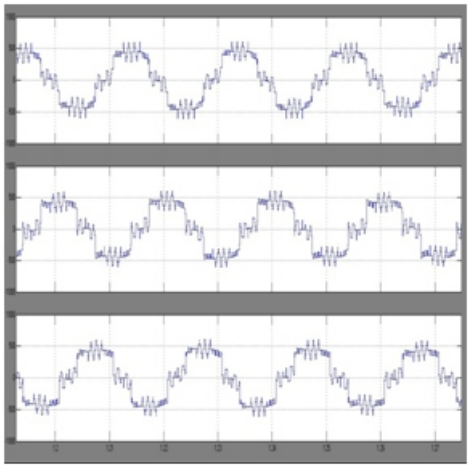

Fig 16.Output line voltages

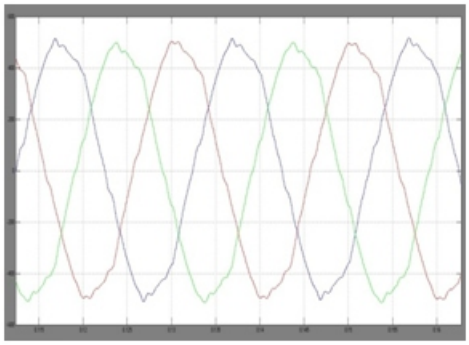

Fig 17.Output line currents

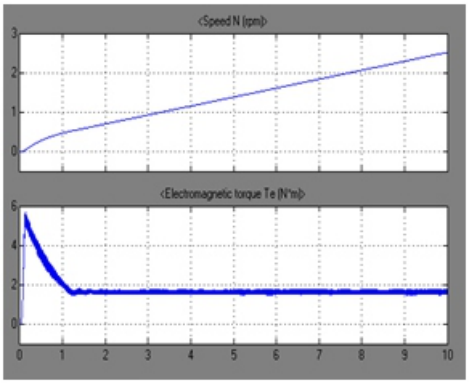

Fig 18.Machine speed and Torque

CONCLUSION:

In this paper, transistor-clamped h-bridge multilevel inverter for PV application with new method of capacitor voltage balancing is presented. A new method to balance the midpoint capacitor voltage in each cell based on third harmonic offset injection was developed and tested.

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The output voltages of the proposed inverter were presented in a double Fourier integral form to determine their harmonics at various operating conditions. The proposed inverter is found potential not only for medium-voltage drive application but also other applications demanding higher output quality.

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