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An Innovative MTCMOS Technique Based Reduction of Leakage Power in Full Subtractor

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Abstract:

As the increasing amount of Area, Power and Speed are considered as the major concerns of the upcoming VLSI era. All of them must be reduced to a greater extent to yield a better device. Combinational logic has extensive application in quantum computing low power VLSI design and optical computing. Power dissipation has become a prime constraint in high performance applications, especially in portable and battery ASIC systems. So it is necessary to reduce power consumption. Scaling the threshold voltage can limit this performance loss to some extent but results in increased leakages. Reducing power dissipation is one of the most principle subjects in VLSI design today. But Scaling causes sub threshold leakage currents to become a large component of total power dissipation. Using MTCMOS approach compare leakage current and leakage power of full subtractor in active mode. Leakage current in conventional full subtractor is 228.7fA and proposed full subtractor is 271. Low-power design techniques proposed to minimize the active leakage power in nanoscale. So the this paper presents an innovative a full subtractor using MTCMOS technique design based full substractor for reduction of leakage power.

Key words:

Full substractor, MTCMOS approach.

I. INTRODUCTION:

Power dissipation has become a prime constraint in high performance applications, especially in portable and battery ASIC systems. So it is necessary to reduce power consumption. Scaling the threshold voltage can limit this performance loss to some extent but results in increased leakages.

The advantage of GDI technique two-transistor implementation of complex logic functions and in-cell swing restoration under certain operating conditions, are unique within existing low-power design techniques. The leakage power is expected to reach more than 50% of total power in sub 100nm technology generation. The power reduction must be achieved without trading-off performance which makes it harder to reduce leakage during normal (runtime) operation. Power gating is one such well known technique where a sleep transistor is added between actual ground rail and circuit ground (called virtual ground). This device is turned off in the sleep mode to cut-off the leakage path. It has been shown that this technique provides a substantial reduction in leakage at a minimal impact on performance. Process and environment parameter variations are posing greater challenges in the design of reliable integrated circuits in scaled CMOS technologies.

Since the invention of the first Integrated Circuit (IC) four decades ago, silicon technology down scaling continues to meet the increasing demands for higher functionality and better performance at a lower cost. Power dissipation, though not entirely ignored, has been of little concern until recently. The advances in VLSI integration technology have made it possible to put a complete System on a Chip (SoC) which facilitates the development of portable systems. Portable battery- powered applications such as notebook computers, cellular phones, Personal Digital Assistants (PDAs), and military equipments profile power dissipation as a critical parameter in digital VLSI design. With the increasing prominence of portable systems, it is important to prolong the battery life as much as possible, since it is the limited battery lifetime that typically imposes strict demands on the overall power consumption of such systems. Although the battery industry has been making efforts to develop batteries with a higher energy capacity than that of conventional Nickel-Cadmium (NiCd) batteries, a revolutionary increase of the energy capacity does not seem imminent.

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Power dissipation is also crucial for Deep Sub-Micron technologies. To further improve the performance of the circuits and to integrate more functions on a chip, the feature size has to continue to shrink. As a result, the power dissipation per unit area grows, increasing the chip temperature. Since the dissipated heat needs to be removed to maintain an acceptable chip temperature, large cooling devices and expensive packaging are required in portable devices and high-performance digital systems such as microprocessors. A recently announced Pentium IV 1 CPU, operating at a 3.4GHz frequency and 1.3V supply voltage, consumes 130W of power.Another important reason for low-power design is reliability. As technologies continue to scale, not only does the power density increase, but also the current density increases. Large current densities cause serious problems such as electro- migration and hot-carrier induced device degradation. In addition, the heat gradient across the chip causes thermal and mechanical stress leading to early breakdown. Therefore, the reliability can only be enhanced if power consumption is reduced Although power dissipation is important for modern VLSI design, performance (speed) and area are still the main requirements of a design. However, low-power design usually involves making tradeoffs such as timing versus power and area versus power.

Increasing performance, while the power dissipation is kept constant, is also considered to be a low-power design problem.The accuracy of estimating the variations relates to the manufacturing cost of an integrated circuit. Results in a conservative design with increased design effort, thereby delaying the time-to-market and degrading performance. Alternatively, an underestimation of variations compromises reliability and functionality, thereby degrading yield. Increasing within-die parameter fluctuations and the complexity in estimating the variations requires new design methodologies for suppressing the effects of process and environment parameter fluctuations in future technology generations. Because of the imbalanced utilization and diversity of circuitry at different sections of an Integrated circuit, temperature can vary significantly from one die area to another. Furthermore, environmental temperature fluctuations can cause significant variations in die temperature. For example, electronic systems mounted on the automobile engines operate at a temperature range from 27°C to 107°C. Temperature variations affect the device characteristics of MOSFETs thereby varying the performance of integrated circuits.

Propagation delay of a circuit is a function of the drain current produced by active transistors. Performance of an Integrated circuit under temperature fluctuations is determined by a set of device parameters. Temperature fluctuations alter threshold voltage, carrier mobility, and saturation velocity of a MOSFET. Temperature fluctuation induced variations in individual device parameters have unique effects on MOSFET drain current. There exists a bias voltage for which device parameter variations counter balance each other's effect on MOSFET current when the temperature fluctuates.

II. PROPOSED WORK:

MTCMOS Technique- The critical dimensions of semiconductor devices are miniaturized with complementary metal-oxide-semiconductor (CMOS) technology scaling. Increasing numbers of transistors are crammed onto integrated circuits, thereby enhancing the operating frequency and functionality. The power consumption of integrated circuits increases with larger number of transistors and higher operating frequency. Excessive power consumption is a primary hindrance to the advancement of CMOS integrated circuits. Leakage currents are important sources of power consumption in modern nanoscale CMOS integrated circuits. Suppressing sub-threshold leakage currents in large scale integrated circuits is essential for achieving green computing and facilitating the proliferation of portable electronics.Multi-threshold CMOS (MTCMOS), which is also known as power/ground gating, is the commonly used leakage power suppression technique in state-of-the-art integrated circuits. Significant power and ground distribution network noise is produced when an MTCMOS circuit blocks transitions from sleep mode to active mode. Mode transition noise is the most important reliability issue in MTCMOS circuits. The generation mechanisms of mode transition noise in MTCMOS circuits are explored in this dissertation. The effectiveness of different noise-aware combinational MTCMOS circuit techniques to deal with the mode transition noise phenomenon is evaluated. An intermediate relaxation mode is investigated to gradually dump the charge stored on the virtual ground wire to the real ground distribution network during the sleep to active mode transitions. Novel noise-aware sequential MTCMOS circuits are presented. A low-leakage data retention sleep mode is implemented with smaller centralized sleep transistors to suppress the mode transition noise produced during the reactivation events in sequential MTCMOS circuits.

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Threshold voltage tuning techniques are typically utilized for leakage power reduction or performance enhancement in integrated circuits. A new application of the threshold voltage tuning methodology is proposed to lower the re-activation noise with smaller sleep transistors and shorter reactivation delay in MTCMOS circuits. The principal mechanism of noise reduction and silicon area compaction in threshold voltage tuned MTCMOS circuits is investigated. Threshold voltage tuning is also effective in mitigating the reactivation noise in sequential MTCMOS circuits.

A new dynamic forward body bias technique is presented to alleviate the mode transition noise in sequential MTCMOS circuits without sacrificing the data retention capability in low-leakage sleep mode.Sleep signal slew rate modulation is an alternative technique that is effective for suppressing the reactivation noise in MTCMOS circuits. A triple-phase sleep signal slew rate modulation technique with a novel digital sleep signal generator is proposed in this dissertation. With the new digital triple-phase sleep signal slew rate modulation technique, fast and energy efficient mode transitions are achieved with negligible reactivation noise in MTCMOS circuits.

The leakage currents that are produced by on-chip memory increase the power consumption of high performance microprocessors. Furthermore, the data stability and write ability of static random-access memory (SRAM) cells are degraded with lower supply voltage, shrinking dimensions of transistors, and exacerbated process variations in each new CMOS technology generation. Compact, robust, and energy efficient memory design is pivotal in deeply scaled CMOS integrated circuits.

The application of MTCMOS technique to SRAM circuits for leakage power suppression is investigated in this dissertation. Various novel asymmetrically ground-gated MTCMOS SRAM circuits are proposed for providing a low-leakage sleep mode with data retention capability. With the new asymmetrical power and ground gating techniques, the data stability is significantly enhanced during both read operations and idle status. Specialized write assist circuitry are also proposed to provide wider write voltage margins with the new memory cells.

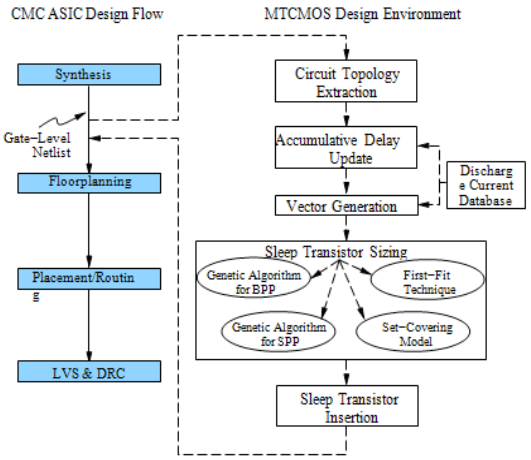

Figure 1: The pictorial view of the point to point wiring connection.

Multi-threshold Voltage CMOS Circuit Technique:

Multi-threshold voltage transistors are typically provided in advanced CMOS technologies to achieve higher performance with a limited power consumption budget. Low-|Vth| transistors are employed on the critical signal delay paths to enhance the speed of a circuit as shown in Fig. 11. Alternatively, high-|Vth| transistors are utilized on the non- critical signal delay paths to suppress the leakage power consumption of the circuit. Due to the utilization of high-|Vth| transistors in the circuit blocks, the leakage power consumption of the circuit is suppressed whenever the high-|Vth| transistors are cut-off. With multi-threshold voltage CMOS, the performance of an integrated circuit is maintained while the leakage power consumption is significantly reduced as compared to standard high-speed circuits that are composed of purely low-|Vth| transistors.

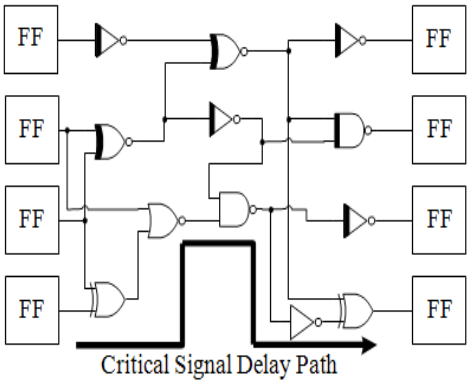

Figure 2: A synchronous circuit with dual threshold voltage logic gates.

ISSN No: 2348-4845
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The critical signal delay path is indicated with a bold line. High-|Vth| CMOS logic gates are represented with thick lines in the gate symbols. Identifying the critical signal delay paths in a high performance chip is a challenging task. State-of-the-art EDA tools are typically required for the timing analysis with integrated circuits that are composed of billions of transistors. Provided that three different threshold voltages are available in a CMOS technology (HVT: high threshold voltage, SVT: standard threshold voltage, and LVT: low threshold voltage), logic gates with standard threshold voltage are typically utilized for implementing the circuits at the initial design stage. After verifying the functionality of the circuit, the critical signal delay paths are identified. Some of the standard threshold voltage logic gates on the critical signal delay paths are replaced by low threshold voltage logic gates to provide a slack on the specified timing requirements.

Alternatively, some of the standard threshold voltage logic gates on the non-critical signal delay paths are replaced by high threshold voltage logic gates (depending on the amount of available timing slack) for leakage power savings. The percent utilization of different threshold voltage transistors in IBM z196 is shown in Fig. 15. Logic gates with four different threshold voltages (super HVT, HVT, SVT, and LVT) exist in this processor. By tuning the threshold voltage of the logic gates during physical design with EDA tools, leakage power consumption is reduced by approximately 10% in this IBM microprocessor.A full subtractor is a combinational circuit that performs a subtraction between two bits taking into account that a 1 may have been borrowed by a lower significant stage. This circuit has three inputs and two outputs. The three inputs A, B and C denote the minuend, subtrahend and previous borrow respectively.

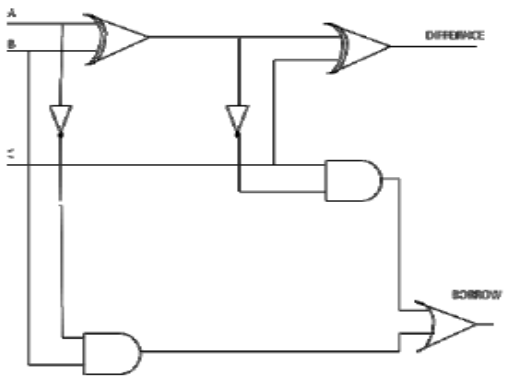

Figure 2: Figure of Full Substractor at gate level.

TABLE I TRUTH TABLE OF FULL SUBTRACTOR

A	B	C	DIFF.	BORROW
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Figure 4: Figure of truth table for full-subtractor.

The two outputs D and BORROW represent the difference and borrow, srespectively. The logic circuit for full subtractor and the truth table for the full subtractor are shown above. The simplified Boolean functions for the outputs can be obtained directly from the truth table. The simplified logic equations are:

$$D = A'B'C + A'BC' + AB'C' + ABC$$

$$BORROW = C(A'B' + AB) + A'B$$

The low-power and high performance design requirements of modern VLSI technology can be achieved by using MTCMOS technology. This technique uses low, normal and high threshold voltage transistors in designing a CMOS circuit. Supply and threshold voltages are reduced with the scaling of CMOS technologies. Lowering of threshold voltages leads to an exponential increase in the sub threshold leakage current. The low-threshold voltage transistors which have high performance are used to reduce the propagation delay time in the critical path. The high-threshold voltage transistors which have less power consumption are used to reduce the power consumption in the shortest path. The multi threshold CMOS technology has two main parts. First, “active” and “sleep” operational modes are associated with MTCMOS technology, for efficient power management. Second, two different threshold voltages are used for N channel and P channel MOSFET in a single chip. These apply on between the low threshold voltage (low-Vt) gates from the power supply and the ground line via cut-off high threshold voltage (high-Vt) sleep transistors is also known as “power gating”. A full subtractor subtracts with three bits (A-B-C). The third bit C is the borrow from previous stage. From the truth table of the full subtractor it can be seen that DIFF = (A B C) and borrow = A’B + BC + CA’. This logic has been implemented.

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Digital Logic

Since Boolean functions are expressed in terms of AND, OR & NOT operations, it is easier to implement a Boolean function with these types of gates. The possibility of constructing gates for other logic operations is of practical interest. Factors to be weighted when considering the constructing of other types of logic gates are

•The feasibility and economy of producing the gate with physical components,

•The possibility of extending the gate to more than two inputs,

•The basic properties of the binary operator, such as commutativity and associativity .

•The ability of the gate to implement Boolean functions alone or in conjunction with other gates.

III. PERFORMANCE ANALYSIS:

In this proposed model, the main aim is to provide MTCMOS technique of full substractor for reduction of leakage power

(a) Top Module Schematic of the substractor

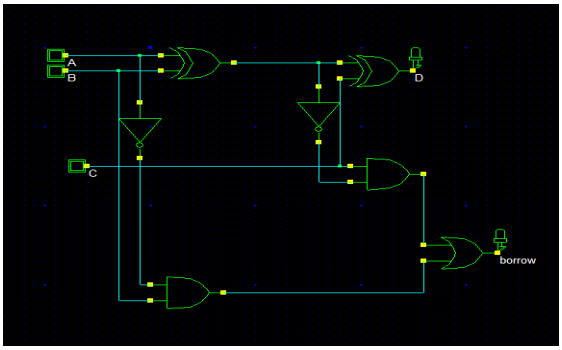

Figure5: Figure of Schematic of Subtractor

The schematic represents the gate design of the proposed substractor .the schematic is drawn using dsch software . The above simulation shows the A,B,C input of the subtractor .d is the difference calculated and the borrow is the carry left .The difference is the substraction between a and b in the above truth table .the carry left is the borrow.

(b)Truth table of Substractor

TABLE I TRUTH TABLE OF FULL SUBTRACTOR

A	B	C	DIFF.	BORROW
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Figure6: Truth table of Subtractor

(c) Substractor using MT cmos technique

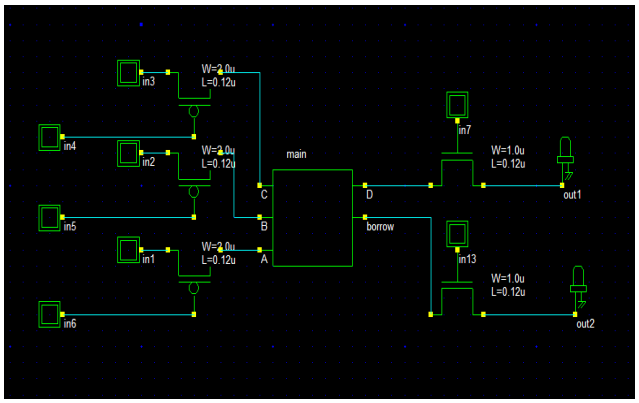

Figure7: Figure of MTCMOS Subtractor schematic

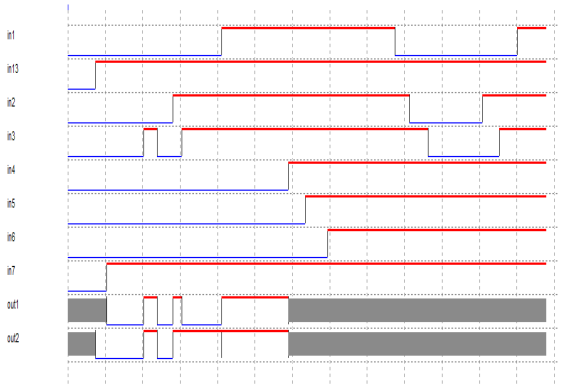

Figure8: Figure of MTCMOS Subtractor Simulation

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(d)Layout design

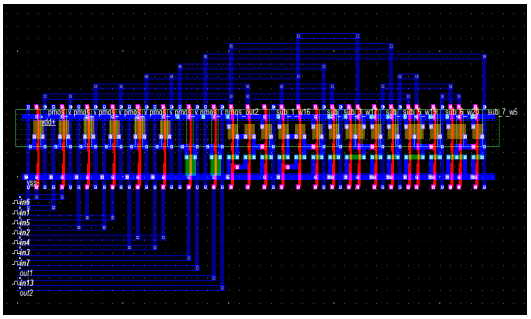

Figure 9: Layout of full subtractor

A full subtractor subtracts 3input bits and gives the output in the form of difference and borrows. We design the transistor level full subtractor using

III. SIMULATION RESULTS:

1.Simulation Power report:

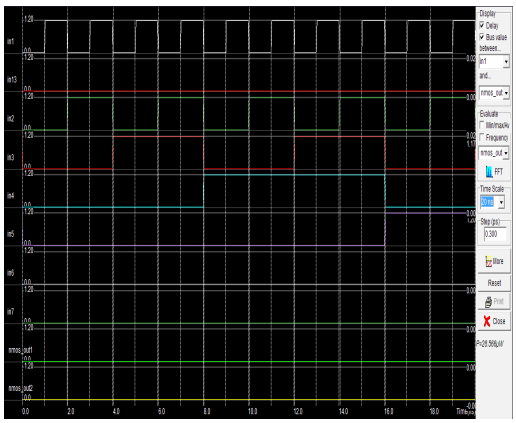

Figure 10: Figure of Power consumed in the microwind software.

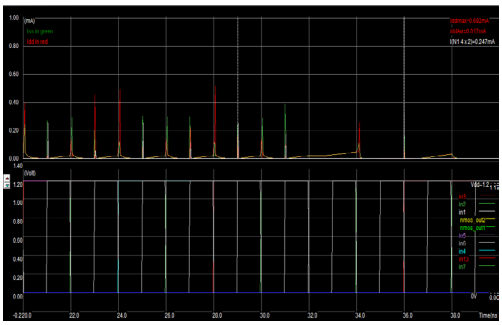

Figure 11: Figure of Power consumed.

cadence virtuoso tool in 45 nm technology and simulate it giving the inputs and get output. By applying the MTCMOS technique in 45nm technology reduction in current and power.The multi threshold CMOS technology has two main parts. First, "active" and "sleep" operational modes are associated with MTCMOS technology, for efficient power management. Second, two different threshold voltages are used for N channel and P channel MOSFET in a single chip voltage vs current graph.

2.Simulation of Logical output

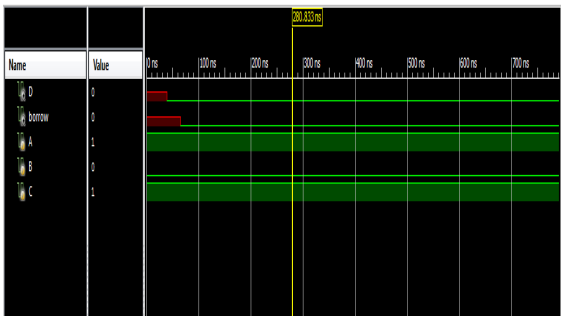

Figure 12: Figure of output

3.Rtl schematic

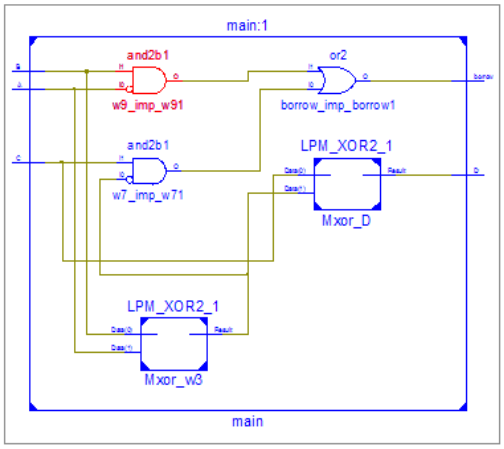

Figure 12: Figure of Schematic diagram in Rtl

IV CONCLUSION:

The existed paper presents "An Innovative MTCMOS Technique Based Reduction of Leakage Power in Full Subtractor" has been successfully designed and the Simulation results are shown in reduction of leakage power using cadence tool in 45nm technology.

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Using 45nm technology for designing of full subtractor reduces in leakage power as well as area compared to conventional full subtractor. Reduction in leakage current is 15.63% and power is 95% compare to the conventional full subtractor.The results are compared with the previous work and we shown that Power is saved 92%, 1% of leakage current and 15% of noise margin. We have performed simulations using 45 Nanometer (nm) Micro wind 3 CMOS layout CAD Tool for design. Further power can be saved by using reduction of parasitic capacitance and by using various parameters.

REFERENCES:

[1] S. Goel, M. A. Elgamel and M. A. Bayoumi, ―Design-nMethodologies Transl. on Circuits and Systems—I: Regular Papers, vol. 53, No. 4, April 2006.

[2] P. M. Lee, C. H. Hsu and Y. H. Hung, ―Novel 10-T full addersrealized by GDI structure‖, Proc. on Intl. Symp. on Integrated Circuits (ISIC2007), pp.115-118.

[3] Jun Cheol Park and Vincent J. Mooney‖ Sleepy Stack Leakage Reduction‖ IEEE transactions on very large scale integration (vlsi) systems, vol.14, no.1. november 2006.

[4] Harmander Singh, Kanak Agarwal, Dennis Sylvester, Kevin J.Nowka,‖Enhanced Leakage Reduction Techniques Using Intermediate Strength Power Gating,‖IEEE Transactions on VLSI Systems, Vol.15, No.11, November2007.

[5] Suhwan Kim, Chang Jun Choi, Deog-Kyoon Jeong,Stephen V.Kosonocky, Sung Bae Park,‖ Reducing Ground-Bounce Noise and Stabilizing the Data-Retention Voltage of Power-Gating Structures,‖IEEEtransactionson Electron Devices,Vol.55,No.1,January2008.

[6] Charbel J. Akl, Rafic A. Ayoubi, Magdy A. Bayoumi, ―An effective staggered-phase damping technique for suppressing power-gating resonance noise during mode transition,‖ 10th International Symposium on Quality of Electronic Design,pp.116-119, 2009.

[7] K. Kawasaki et al., ―A sub-us wake-up time power gating technique with bypass power line for rush current support,‖ IEEE J. Solid-State Circuits , vol.44, no. 4, pp.146–147, Apr. 2009.

[8] Ku He, Rong Luo, Yu Wang, ―A Power Gating Scheme for Ground Bounce Reduction During Mode Transition, ‖ in ICCD07, pp. 388-394, 2007.

[9] Deepa Sinha, Tripti Sharma, K.G.Sharma, Prof.B.P.Singh Design and analysis of low power 1 bit full adder cell IEEE paper 2011 ,978-1-4244 -8679-3/11/$26.00 ©2011 IEEE

[10] S. Borkar, T. Karnik, S. Narendra, J. Tschanz, A. Keshavarzi and V. De, ―Parameter Variation and Impact on Circuits and Micro Architecture,‖ Proceedings of the IEEE/ACM International Design Automation Conference, pp. 338-342,June 2003.

[11] R. Kumar and V. Kursun, ―Voltage Optimization For Temperature Variation Insensitive CMOS Circuits, "Proceedings of the IEE International Midwest Symposium onCircuits and Systems, pp. 476-479, August 2005.

[12] Y. Cheng, K. Imai, M. C. Jeng, Z. Liu, K. Chen, and C. Hu,―Modeling Temperature Effects of Quarter MicrometreMOSFET in BSIM3v3 for Circuit Simulation,‖ SemiconductorScience Technology, Vol. 12, pp. 1349-1354, November 1997.

[13] Y. P. Tsividis, Operation and Modeling of the MOS Transistor,McGraw-Hill, New York, 1999.

[14] R. W. Johnson et al., ―The Changing Automotive Environment: High Temperature Electronics,‖ IEEE Transactions on Electronics Packaging Manufacturing, Vol. 27, No. 3, pp. 164-176, July 2004.

[15] I.M. Filanovsky and A. Allam, ―Mutual Compensation of Mobility and Threshold Voltage Temperature Effects with Applications in CMOS Circuits,‖ IEEE Transactions on Circuits and Systems I, Vol. 48, No. 7, pp. 876-884, July 2001.

[16] D. A. Antoniadis, I. Aberg, C. N. Chléirigh, O. M. Nayfeh,A. Khakifirooz, and J. L. Hoyt, "Continuous MOSFET performance increase with device scaling: The role of strain and channel materialinnovations," IBM J. Res. Develop., vol. 50, no. 4, pp. 363–376,Jul. 2006.

[17] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deepsubmicrometerCMOS circuits," Proc. IEEE, vol. 91, no. 2, pp. 305– 327,Feb. 2003.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

[18] Himanshu Thapliyal, Sumedha K. Gupta, "Design of Novel Reversible Carry Look-Ahead BCD Subtractor", 9th International Conference on Information Technology (ICIT'06), 2006.

[19] S. Dutta, S. Nag, K. Roy, "ASAP: A Transistor Sizing toolfor speed, area, and power optimization of static CMOS circuits", IEEE
International Symposium on Circuits andSystems, pp. 61-64, June, 1994.

[20] Mutoh S et al, "1-V Power supply high-speed digital circuit technology with multithreshold- voltage CMOS",IEEE J. Solid State Circuits, Vol.30, pp. 847-854, August 1995.

[21] Hemantha S,Dhawan A and Kar H ,"Multi-threshold CMOS design for low power digital circuits",TENCON 2008-2008 IEEE Region 10 Conference,pp.1-5,2008.

[22] H. Thapliyal, M.B Srinivas and H.R Arabnia,"Reversible Logic Synthesis of Half, Full and ParallelSubtractors", Proc.of the 2005 Intl. Conf. on Embedded Systems and Applications, Las Vegas,pp.165-181, 2005.

[23] Phanikumar M and N. Shanmukha Rao, "A Low Power and High Speed Design for VLSI Logic Circuits Using Multi-Threshold Voltage CMOS Technology", International Journal of Computer Science and Information Technologies (IJCSIT), Vol. 3(3), pp- 4131-4133, 2012.

[24] Dong Whee Kim, Jeong Beom Kee, "Low-Power Carry Look-Ahead Adder With Multi-Threshold Voltage CMOS Technology", in Proceeding of ICSICT International Conference on Solid-State and Integrated-Circuit Technology, pp. 2160-2163, 2008 .

[25] H. Thapliyal and N. Ranganathan, "Conservative QCAGate (CQCA) for Designing Concurrently Testable Molecular QCA Circuits", Proc. of the 22nd Intl. Conf.on VLSI Design, New Delhi, India, pp. 511-516, 2009.

[26] Majid Mohammadi, Mohammad Eshghi, Majid Haghparast and Abbas Bahrololoom, "Design and Optimization of Reversible BCDAdder/Subtractor Circuit for Quantum and Nanotechnology BasedSystems", World Applied Sciences Journal, vol. 4, no. 6, pp. 787- 792, 2008.

[27] Zimmermann R. and Fichtner W., Low-power logic styles: CMOS versus pass-transistor logic, IEEE J. Solid-State Circuits, Vol. 32, No. 7, 1079–1090, 1997.

[28] J. Kao, A. Chandrakasan, and D. Antoniadis, "Transistorsizing issues and tool for multi-threshold CMOStechnology," in Proc. 34th DAC, pp. 409–414, 1997.

[29] A. Monpapassorn, "Programmable wide range voltage adder/subtractor and its applications an encoder," IEE Proceeding of Circuits Devices and Systems, vol. 152, pp. 697–702, 2005.

[30] Neil Weste and D. Harris, "CMOS VLSI Design: A Circuit and System Perspective," Pearson Addition Wesley, third Edition, 2005.

[31] R. Fried and C. C. Enz, "Simple and accurate voltageadder/subtractor," Electronics Le tters, vol. 33, pp. 944–945.