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A Novel Approach for Designing Testable Reversible Sequential Circuits

V.Harshavardhan Kumar
M.Tech (VLSI Design)
Srinivasa Ramanujan Institute of Technology
Rotarypuram Village, B K Samudram Mandal,
Anantapur, A.P-515701.

M.Ramireddy
Associate Professor,
Srinivasa Ramanujan Institute of Technology
Rotarypuram Village, B K Samudram Mandal,
Anantapur, A.P-515701.

Abstract:

In this paper, we tend to propose conservative logic gates based two vector testable sequential circuits. The conservative logic gates based sequential circuit proposed outperforms the classical conventional based sequential circuits in terms of testability. By using only two test vectors for classical unidirectional stuck-at faults any conservative logic gates based sequential circuit can be tested, all 0's and 1's are the two test vectors. The two vectors testable designs of latches, master-slave flip-flop's and DET (Double edge triggered) flip-flop is presented. The works significance lies in the fact that it provides completely testable reversible sequential circuits design for any stuck-at-fault(S-A-F) by only two test vectors i.e. all 0's and 1's which eliminates the necessitate for any type of scan path access to internal memory cells. The DET (Double edge triggered) flip-flop reversible design is proposed for the first time in the literature. The proposed approach provides 100% fault coverage for any single missing or additional cell defect in the QCA (quantum-dot cellular automata) of the Fredkin gate. We are also presenting a new conservative logic gate called MX-cqca (multiplexer conservative QCA gate) that is not reversible in nature but has properties similar to the Fredkin gate of working as 2:1 multiplexer. The proposed MX-cqca gate excels the Fredkin gate in terms of complexity (the number of majority voters), speed, and area.

Index Terms— ***Cellular automata, conservative logic, Fredkin gate, quantum-dot, reversible logic.***

I. INTRODUCTION

CONSERVATIVE logic may be a logic family which exhibits the property of equal number of 1's within the outputs as there are within the inputs. Conservative logic are often reversible in nature or might not be reversible in nature in certain cases. Reversibility is that the property of circuits in which inputs and outputs exhibits one to-one mapping. In other words for every input vector there's a unique output vector and similarly for every unique output vector there exists a unique input vector. Conservative logic is termed as reversible conservative logic whenever there exists a injective mapping in between the inputs and the outputs vectors in conjunction with the property that there's equal range of 1's within the outputs as within the inputs. Conservative logic circuits aren't reversible, if injective mapping in between the inputs and the outputs vectors isn't preserved.

Further, QCA is one among the rising nanotechnologies in which it is feasible to realize reversible logic gates. QCA(quantum dot cellular automata) makes it feasible to attain circuit densities and clock frequencies beyond the boundaries of present CMOS technology. In QCA(quantum dot cellular automata) logic states of one and zero are depicted by the position of the electrons within the QCA(quantum dot cellular automata) cell as elucidated in above Fig 1. There's no tangible discharging of the capacitor as in typical CMOS when the bit is flipped from one to zero. Hence, QCA doesn't ought to dissipate all of its signal energy during transition phase. Further, propagation of the polarization from one to another cell is attributable to interaction of the electrons in adjoining QCA(quantum dot cellular automata) cells. There's no current flow as there's no movement of electrons from one QCA(quantum dot cellular automata) cell to the other QCA cell,. Therefore in QCA no dissipation occurs in signal propagation. So QCA has important benefit in comparison with cmos technology in terms of power dissipation. Because of high error rates in nano-scale manufacturing technologies, QCA and alternative nanotechnologies aims at dropping device error rates.

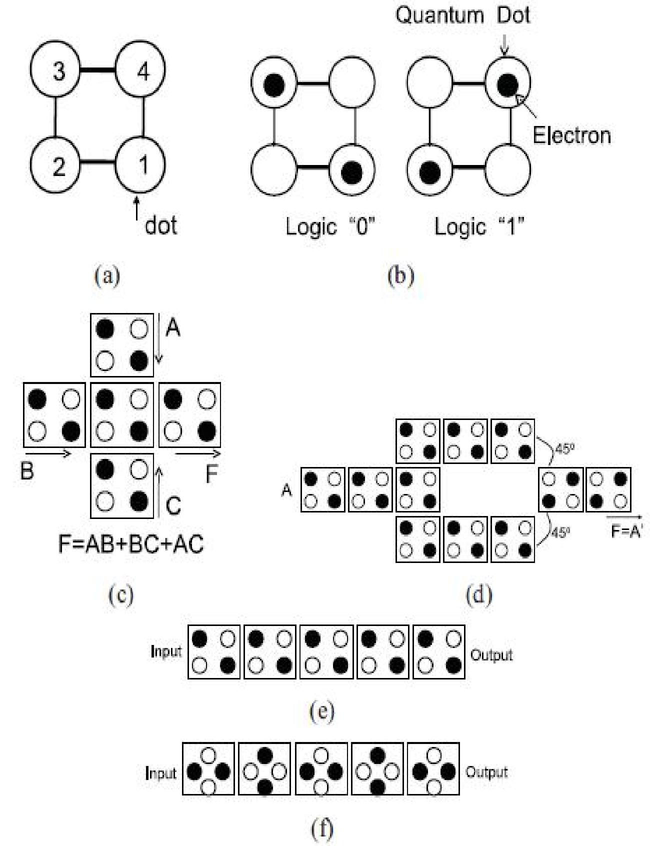

Fig. 1. Basic QCA devices. (a) QCA 4 Dots structure (b) QCA cell as logic "1" & logic "0" (c)MV (majority voter). (d) INV (e) Binary wire (f) INV chain

This paper tends to propose the design of testable sequential circuits supported by conservative logic gates. The proposed technique can watch out the fan-out at the reversible latches output which may additionally disrupts the feedback to make them appropriate for testing only by two test vectors, all 0's and 1's. In alternative words, circuits can have feedback when functioning in the normal mode. Nevertheless, in order to find faults within the test mode, our proposed technique can disrupt feedback to form combinational circuits from conservative reversible latches testable. In the projected technique aimed towards the design of two vectors testable flip-flops like master-slave flip-flops, double edge triggered (DET) flip-flops. This work is critical as it was providing the design of reversible sequential circuits which are completely testable for unidirectional stuck-at faults by only two test vectors i.e. all 0's and 1's. Further, we tend to enforce the Fredkin gate within the QCA technology and ascertained that all 0's and 1's test vectors cannot offer 100 percent fault coverage for any single missing or additional cell defect within the QCA(quantum dot cellular automata) layout of the Fredkin gate. Therefore, to possess the 100 percent fault coverage for any single missing or additional cell defect by all 0s & 1's test vectors, it was detected the QCA devices within the QCA layout of the Fredkin gate which can be replaced with their fault tolerant components so as to provide 100 percent fault coverage. Further, when designing QCA sequential circuit, the designer could typically choose to sacrifice the reversibility to save number of QCA cells whereas keeping the test strategy to be a similar. Thus, we also additionally propose a new conservative QCA gate (MX-cqca) that's not reversible in nature however has similar properties because the Fredkin gate of operating as 2:1 multiplexer. The proposed MX-cqca gate excel the Fredkin gate in complexity, area, and speed.

This paper is organized as follows. Section II deals with the background on conservative logic, the basics of QCA computing. Section III deals with the testable reversible latches design, Section IV presents testable reversible master-slave flip-flops design, Section V describes testable reversible DET flip-flop design, Section VI describes the proposed MX-cqca(multiplexer conservative QCA gate), Section VII presents the design methodology for non reversible circuits based on MX-cqca gate, and Section VIII provides presents conclusions.

II. BACKGROUND

A conservative logic gate may be a multiple-output device in which the number of 1's in the inputs is equal to that of the corresponding 1's at the outputs. A conservative logic circuit are often considered as a directed graph whose nodes are conservative logic gates where as the edges are wires of arbitrary lengths. FO (fan out) at the output isn't allowed in conservative logic circuits.

A conservative logic network is often reversible in nature if the injective mapping is maintained between the inputs and the outputs, whereas it'll be irreversible in nature if injective mapping isn't preserved. In a conservative logic the two test vector sets all 1's & 0's, offer 100 percent fault coverage to unidirectional stuck-at-faults. For any stuck-at-1(S-A- 1) fault with the conservative logic circuit are often detected by giving all inputs to 0's and checking the outputs for the presence of any 1's. Similarly any stuck-at-0(S-A- 0) faults are often detected by giving all inputs to 1's and checking the outputs for the presence of any 0's.

i. Conservative Reversible Fredkin Gate

Fredkin gate first proposed by Fredkin and Toffoli is one of the popularly used reversible conservative logic gate. The Fredkin gate depicted in Fig. 2 are often described as a mapping of A, B, C to P = A, Q = A_B + AC, R = AB + A_C. Here A, B, C are the inputs where as P, Q, R are the outputs, severally. The Fredkin gate truth table is illustrated in fig, that reveals that Fredkin gate is both reversible and conservative in nature. i.e. it has distinctive input and output mapping and additionally has a similar number of 1's within the outputs as within the inputs.

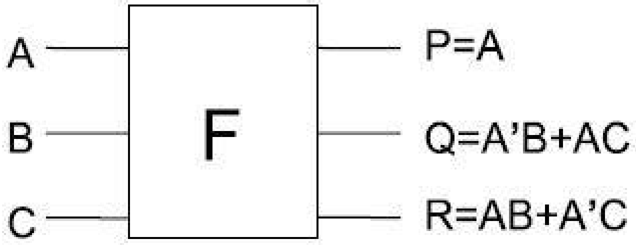

Fig.2.Fredkin gate.

ii. Basics of QCA Computing

The conservative logic gates are enforced within the QCA nanotechnology. Each QCA(quantum dot cellular automata) cell is a coupled dot system where four dots are at the vertices of a square. Each cell further has two additional electrons that occupy the diagonals among the cell because of electrostatic repulsion. This is depicted in Fig 1(a) and (b) which displays the four quantum dots in a QCA(quantum dot cellular automata) cell, the implementation of logic "0" and logic "1" in a QCA cell, severally.

The fundamental QCA device is that the MV or majority gates, that is depicted as F = AB + BC + AC. Another vital gate in QCA is that the INV. There are often many ways in designing the QCA INV, one among that is depicted in Fig 1(d). Signal transfer in QCA computing is created through wires that are of 2 types: 1) INV chain and 2) binary wire. The binary wire is depicted in Fig. 1(e). The INV chain is depicted in Fig 1(f). In QCA(quantum dot cellular automata), when a binary wire crosses the INV chain or vice versa, there's no interaction between the two; thus, the signals within the INV chain and binary can pass over one another.

In QCA (quantum dot cellular automata) computing the clock signal aids in the synchronization of circuits and in addition provides the power needed for functionality. QCA(quantum dot cellular automata) clocking system consists of four phases like switch, hold, release, and relax.

III. DESIGN OF TESTABLE REVERSIBLE LATCHES

The D latch characteristic equation is often written as Q+ = D • E + Ē• Q.

Here enable (E) cites to the clock which is employed interchangeably in the place of clock. The value of the input D is mirrored at the output when the enable signal (clock) is 1, that's Q+ = D. When E = 0 the latch remains in its previous state, i.e. Q+ = Q. The two of its outputs of reversible Fredkin gate are operating as

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2:1 MUxes, The D latch characteristic equation might be mapped to the Fredkin gate. The realization of the reversible D latch using the Fredkin gate is depicted in fig.3(a).

However FO isn't allowed in conservative reversible logic because the design can't be tested by two input vectors i.e. all 0's and 1's due to feedback, as the output Q would latch to one if the inputs are toggled from all ones to all zeros and will be misinterpreted as stuck-at-1(S-A-1) fault.

As depicted in Fig.3(b) here another Fredkin gate is cascaded to output Q. The design has 2 control signals, C1 and C2. The design functions in two modes one is normal mode and other is the test mode.

1) Normal Mode: The normal mode is depicted in Fig.3(c) during which we can have control signals C1C2 = 01 and that makes design functioning as a D latch and fan-out problem can be eliminated.

2) Test Mode : In this mode, once control signals C1C2 = 00, it makes possible for the design testable with all 0's input vector as output T1 will become 0 leading it to be testable with all 0's input vectors as depicted in Fig.3(d). Thus, any stuck-at-1(S-A-1) fault are often detected.

When C1C2 = 11 as depicted in Fig.3(e), the output T1 would become 1 and also the design can be testable with all of its input vectors as 1's for any stuck-at-0(S-A-0) fault. The feedback in the test mode and the fan out in the normal mode is done by the control signals C1 and C2. Therefore proposed design functions as a reversible D latch and may be tested with only two test vectors i.e. all 0's and 1's for any stuck-at-fault by employing the property of conservative reversible logic.

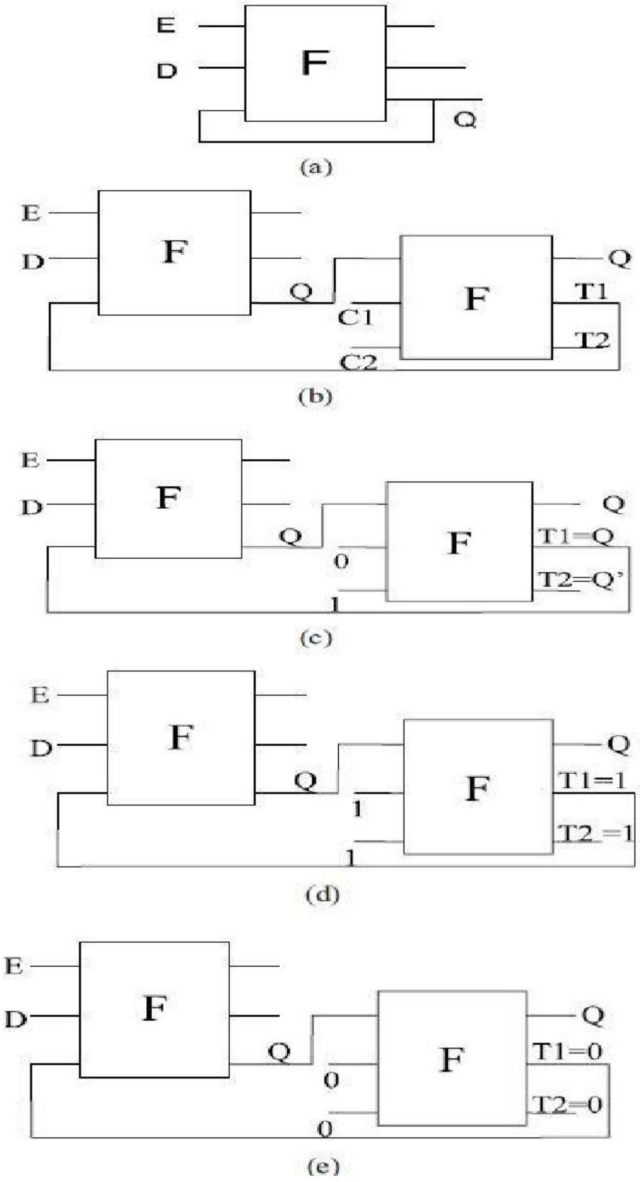


Fig. 3. (a) D latch using Fredkin gate (b) D latch using Fredkin gate with control signals C1 &C2 (c) D latch using Fredkin gate in normal modes C1 = 0 & C2 = 1 (d) D latch using Fredkin gate in test modes for stuck-at-0 fault C1 = 1 & C2 = 1 (e) D latch using Fredkin gate in test modes for stuck-at-1 fault C1 = 0 & C2 =0.

A. Design of Testable Negative Enable Reversible D Latch:

When E = 0, negative enabled reversible D latch can propagate the input D to the output Q. Otherwise it remains in a similar state. The characteristic equation of the negative enabled D latch is $Q+ = D\bullet\overline{E}+E\bullet Q$.

The negative enable reversible D latch characteristic equation are often mapped on to the Fredkin gate second output as depicted in Fig.4. The second Fredkin gate within the design take cares of the Fan out. The second Fredkin gate within the design additionally helps in creating the design which is testable by only two test vectors i.e. all 0's and 1's by disrupting feedback based on control signals C1 and C2 values same as explained for the positive enable reversible D latch. It in designing testable reversible master-slave flip-flop's negative enabled D latch can be useful, because as it works as a slave latch within the testable reversible master-slave flip-flops during which no clock inversion is needed. The main points of it are mentioned within the section describing reversible master-slave flip-flop's.

This makes the outputs mT1 and sT1 equals to 1 and make the design testable with all input vectors as 1's for any stuck-at-0 (S-A-0) fault by disrupting the feedback.

The other master-slave flip-flops are testable master-slave T flip-flop's, testable master-slave JK flip-flop's, and testable master-slave SR flip-flop's. These are also designed in the same method in which master is designed with the positive enable latch, whereas the slave is designed with the negative enable D latch based on fredkin gate. For instance, master-slave design of T flip-flop has the master designed with the positive enable T latch, whereas the slave by the negative enable T latch.

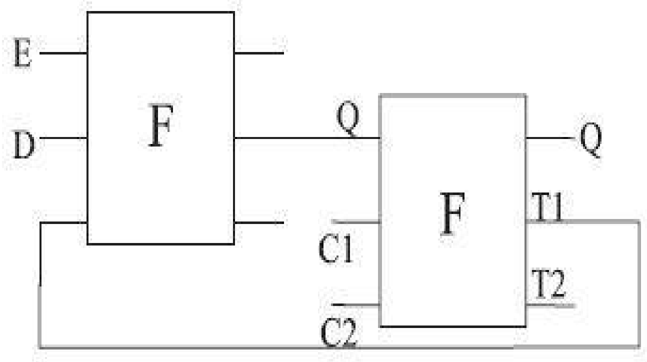


Fig.4. Negative enable testable D latch using Fredkin gate.

IV. DESIGN OF TESTABLE MASTER-SLAVE FLIP-FLOPS

In the existing literature, By utilising the master-slave strategy with one latch as a master and also the alternative latch as a slave is employed to design the reversible flip-flop's.

Here the design of testable flip-flop's is proposed employing the master slave strategy which will be tested for any stuck-at fault's utilising two test vectors only i.e., all 0's and 1's. The Fig.5 depicts the design of D flip-flop in master- slave mode, during which we have used positive enabled Fredkin gat e-based testable D latch depicted in fig.3(b) as the master latch, whereas the slave latch is designed from the negative enabled Fredkin gate-based testable D latch depicted earlier in fig.4. It has four control signals which are mC1,mC2, sC1, and sC2. In which mC1 and mC2 controls the modes for the master latch, whereas sC1 and sC2 controls slave latch modes. In the normal mode, master-slave flip-flop has controls signals values as mC1 = 0 & mC2 = 1, sC1 = 0 & sC2 = 1 (similar to the control signals C1 and C2 represented earlier for the testable D latch).

In the Test mode:

1) The values for the controls signals are going to be mC1 = 0 and mC2 = 0, sC1 = 0 and sC2 = 0, to enable design testable with all 0's input test vectors for any stuck-at-1(S-A-1) fault,. It makes the outputs mT1 and sT1 as 0, makes the design to be testable with all 0's input vectors for any stuck-at-1(S-A-1) fault by disrupting the feedback.

2) The values of the control signals are going to be mC1 = 1, mC2 = 1, sC1 = 1, and sC2 = 1 to facilitate the design to be testable with all input test vectors as 1's for any stuck-at-0 (S-A-0) fault.

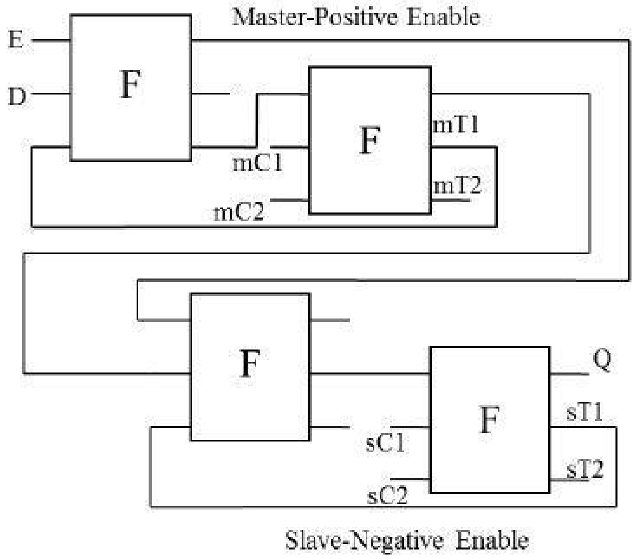


Fig 5. Testable reversible master-slave D flip-flop using Fredkin gate.

V. DESIGN OF TESTABLE REVERSIBLE DET FLIP-FLOPS

The DET flip-flop is a computing circuit which samples and stores the information at each edge of the clock, that's at each of the rising and falling edges of the clock. The most common approach used in designing this flip-flop is master- slave strategy. In the planned work, E employed interchangeably used in situ of clock. When E = 1 (high clock), the master propagates the input date whereas the slave latch remains in the previous state in the negative edge triggered master-slave flip-flop. once E = 0 (clock low), the master remains in the storage state and the slave latch propagates the output of master to its output. Therefore the flip-flop doesn't sample the information at each the clock levels and waits for subsequent rising clock edge to latch the information to the master latch.

In order to overwhelm the problem, concept of DET flip-flops is introduced, which samples the information at both edges of the clock. Thus, DET flip-flops will receive and sample two data values in same clock period therefore frequency of the clock are often reduced to half the master-slave flip flop while retaining a similar data rate. The half frequency operations enable the DET flip flops substantially useful for low power computing as frequency is directly proportional to consumed power. It is outlined by connecting the 2 latches, viz., the positive enable and also the negative enable in parallel instead of in series. The output from one of these latches that is in the storage state (previous state) is transferred to output by 2X1 mux. The conventional design style of the DET flip-flop is often found. The design of the testable reversible DET flip-flop is projected in this project is depicted in Fig.6(a).

In the proposed design style of the positive enable testable reversible D latch, testable reversible DET flip-flop, and also the negative enabled testable reversible D latch are organized in parallel. The Fredkin gates labelled as 1 and 1 constitute the positive enable testable D latch, whereas the Fredkin gates which is labelled as 3 & 4 constitutes the negative enable testable reversible D latch. The Fredkin gate labelled as 6 is employed to copy the input signal D as fan-out isn't allowed in reversible logic. The Fredkin gate which is labelled as 5 functions as the 2x1 MUX which transfer the output from one among these latches which is in the storage state to the output Q. Here pC1 and pC2 are the control signals of the testable positive enabled testable reversible D latch and testable reversible negative enabled D latch has the control signals nC1 and nC2. Depending on the values of the control signals pc1, pc2, nc1, and nc2 the testable DET flip-flops functions either in test mode or within the normal mode.

1) Normal Mode: The values of control signals are pC1 = 0, pC2 = 1,nC1 = 0, and nC2 = 1 in the normal mode of the DET flip-flop is illustrated in Fig.6(b). The output of the positive enable D latch is copied when pc1 = 0, pc2 = 1, therefore avoiding the FO whereas the nc1 = 0 & nc2 = 1 help in copying the output of the negative enable D latch therefore avoiding the FO.

2) Test Mode: There are two test modes. a) All 1's input test Vectors: The value of control signals are pc1

= 1, pc2 = 1, nc1 = 1, and nc2 = 1 which is illustrated in Fig.6(d). The control signals pc1 = 1 & pc2 = 1 allows in disrupting the feedback of the positive enable D latch, similarly the control signals nc1 = 1 & nc2 = 1 allows in disrupting the feedback of the negative enable testable reversible D latch. This facilitates the design testable by all 1's input test vector for any stuck-at-0 (S-A-0) fault.

b) All 0's input test Vectors: The values of the control signals as pc1 = 0, pc2 = 0, nc1 = 0, and nc2 = 0 this mode is illustrated in Fig.6(c). The control signals pc1 = 0 and pc2 = 0 allows in disrupting the feedback of the positive enable testable reversible D latch, whereas the nC1 = 0 and nC2 = 0 allows in disrupting the feedback of the negative enable testable reversible D-latch. This makes the design testable by all 0's input test vector for any stuck-at-1 fault (S-A-1).

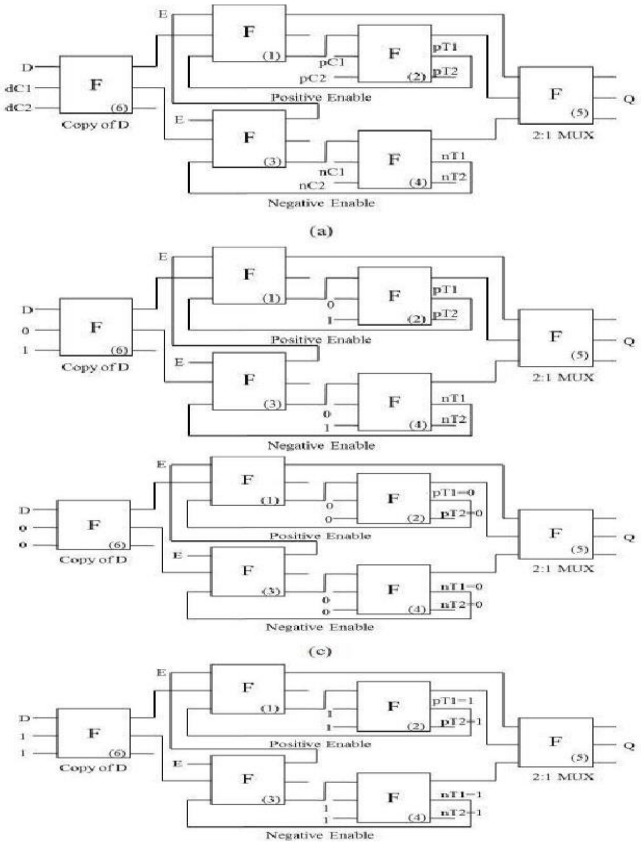


Fig..6.Fredkin gate-based DET flip-flop. (a) Fredkin gate based DET flip-flop.(b) Normal mode. (c) Test mode for stuck-at-1 fault. (d) Test mode for stuck-at-0 fault

VI. PROPOSED MULTIPLEXER CONSERVATIVE QCA GATE

For many of the design styles, the designer might probably have an interest in using the testing advantages of conservative logic but not saving the number of QCA cells. Thus, in this project, we tend to propose a new conservative logic gate that's conservative in nature however isn't reversible. The proposed conservative logic gate is termed as multiplexer conservative QCA gate.

It has 3 inputs and 3 outputs. MX-cqca has one of its outputs operating as a multiplexer which will facilitate in mapping the sequential circuits based on it, whereas the other 2 outputs work as AND and OR gates, severally. The mapping of the inputs to outputs of the MX-cqca is: $P = AB$; $Q= A\overline{B}+BC$;$R = B + C$, where A, B, and C are the inputs while P, Q, R are the outputs, severally.

Fig.7 depicts the diagram of the MX-cqca gate. Table V depicts the truth table of the MX-cqca gate. The table verifies the gate’s conservative logic nature, i.e., that the number of 1's within the inputs is equal to the number of 1's within the outputs.

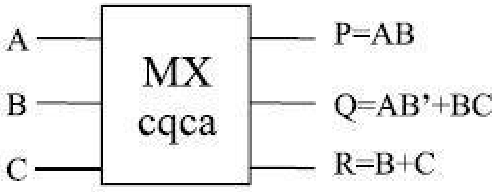


Fig. 7 Proposed MX-cqca gate.

VIII. DESIGN METHODOLOGY FOR NONREVERSIBLE TESTABLE DESIGN BASED ON MX-cqca GATE

The proposed conservative logic gate MX-cqca is helpful to design any majority logic and multiplexer logic-based testable non-reversible sequential circuits. In the existing literature, 13 standard functions are proposed to represent all three-variable Boolean functions. These 13 functions are wide employed in QCA and majority logic-based synthesis. so as to design any complicated function supported by MX-cqca, the proposed design methodology is often summarized within the following 3 steps.

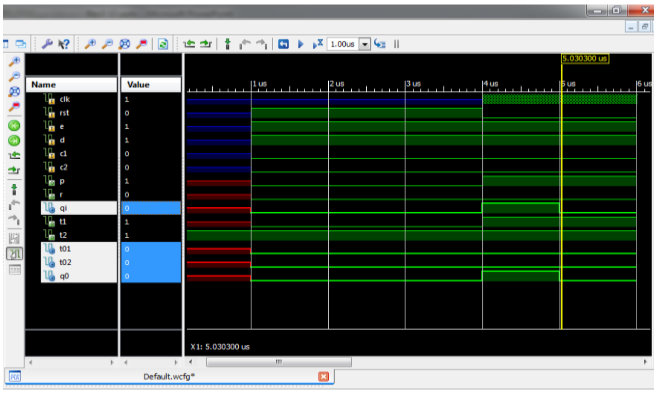
Step 1: The input performs is decomposed into the Boolean network in which each node has virtually 3 variables. This step is analogous to the design methodology proposed.

Step 2: The 3 variable functions generated at each node in Step one is mapped to its MX-cqca based implementation. The mapping relies on the library of thirteen standard functions enforced using the MX-cqca

Step 3: The nodes that have fan-out of greater than 1 are identified, and MX-cqca gates are used to form the copy of these signals, that have fan-out of greater than 1.

FINAL RESULTS:

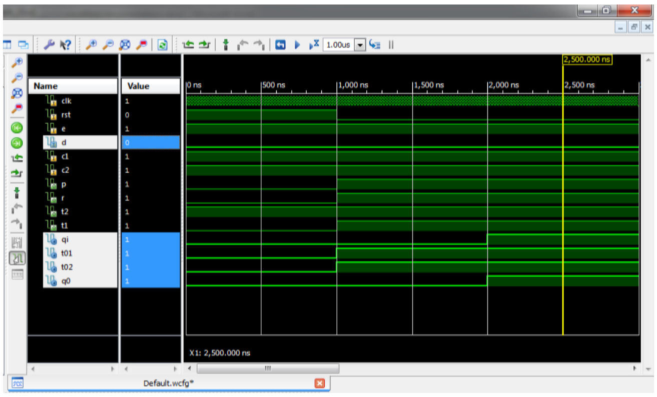
S-A-1:



Name	Value
clk	1
rst	0
e	1
d	1
c1	0
c2	0
p	1
r	0
qi	0
t1	1
t2	1
t01	0
t02	0
q0	0

X1: 5.030300 us

S-A-0:



Name	Value
clk	1
rst	0
e	1
d	0
c1	1
c2	1
p	1
r	1
t2	1
t1	1
qi	1
t01	1
t02	1
q0	1

X1: 2,500.000 ns

IX. CONCLUSION:

The paper proposed reversible sequential circuits based on conservative logic that is testable by using only two test vectors i.e. all 0's and 1's for any unidirectional stuck-at-faults. The projected sequential circuits which are based on conservative logic gates outperform the sequential circuit implemented in classical conventional gates in terms of testability. The sequential circuits implemented using conventional classic gates do not provide inherited support for testability. Hence, a conventional sequential circuit needs modification in the original circuitry to provide the testing capability. Also as the complexity of a sequential circuit increases the number of test vector required to test the sequential circuit also increases. For example, to test a complex sequential circuit thousand of test vectors are required to test all stuck-at-faults, while if the same sequential circuit is build using proposed reversible sequential building blocks it can be tested by only two test vectors i.e. all 0's and 1's. Thus, the main advantage of the proposed conservative reversible sequential circuits compared to the conventional sequential circuit is the need of only two test vectors to test any sequential circuit irrespective of its complexity. The reduction in number of test vectors minimizes the overhead of test time for a reversible sequential circuit. The proposed work has the limitation that it cannot detect multiple stuck-at-faults as well as multiple missing/additional cell defects. In conclusion, this paper advances the state-of-the-art by minimizing the number of test vectors needed to detect stuck-at-faults as well as single missing/additional cell defects.

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