ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Implementation of Quantum Cost Optimization on Reversible Sequential Circuits

A.Krishna Mayukha
VLSI & ES(ECE),
Department of ECE,
Prakasam Engineering College
Kandukuru, Prakasamdt, A.P.

Dr.CH.Ravi Kumar, M.Tech, Ph.D
HOD,
Department of ECE,
Prakasam Engineering College
Kandukuru, Prakasamdt, A.P.

Abstract:
In this paper, we look forward Reversible design offers sequential circuits by using the adder. Sequential circuits synthesis of reversible very new research area. As such circuits can be implemented using quantum dot cellular automata found that emerging technologies. The work will use traditional designs in the past, and their reversible sequential circuits, flip-flops and gates replaced counterparts. Ancilla inputs in terms of the quantum of work in front of our cost and replacement technique has proven to be better than the direct feedback that is used without any flip-flops. The work of our direct feedback method, which uses a different approach to sequential circuits, an improved version of the mapping is reversible. Ancilla inputs cost in terms of the quantum of proposed method of design examples and the results will be better than our previous method.

Conservative logic inputs are an equal number of 1s are the products that display the logic of the family property. Conservative logic may be reversible in nature or may not be reversible in nature. Risk of recurrence and vice versa inputs and a single output vector for each input vector is a mapping between the output vectors, one of the circuits in which the property is located. 1s there are an equal number of inputs and outputs as inputs and outputs vectors of property mapping from each other when the Conservative logic is the logic of the conservative reversible. Conservative unique mapping between logic circuits vectors of inputs and outputs, if not preserved, are reversible.

INTRODUCTION:
In this paper, we explore two vector conservative logic gates based on the proposed design of sequential circuits. Conservative in terms of the music, the gates of logic gates based on the implementation of the proposed testability of sequential circuits Sequential circuits outperform. Any sequential circuit based on the conservative logic gates at the two test vectors are difficult to test the music using unidirectional faults. The two test vectors all 1s, and all are 0s. Master-slave flip-flops and latches of the two vector testable models of double edge (DET) performed triggered flip-flops. By any difficulty at fault just two test vectors, thereby eliminating the need for any type of internal memory cells in the scan-path access to the importance of the proposed research design is the fact that testable, reversible sequential circuits. DET reversible design of the flip-flop has been proposed in the literature for the first time.

We also quantum- dot cellular automata gate Friedkin (QCA) in the layout of the missing / extra cell deficiency showed a 100% fault coverage to the application of the proposed approach. 1 Multiplexer: We also Conservative QCA gate Multiplexer (MX-cqca), a new conservative logic gate similar in nature will not be repeated, but 2 is characterized as the work is performed by the gate Friedkin. The complexity of the proposed MX-cqca gate (the vast majority of the number of voters), speed, and surpasses the gate in terms of land Friedkin. Conservative logic inputs are an equal number of 1s are the products that display the logic of the family property. Conservative logic may be reversible in nature or may not be reversible in nature.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

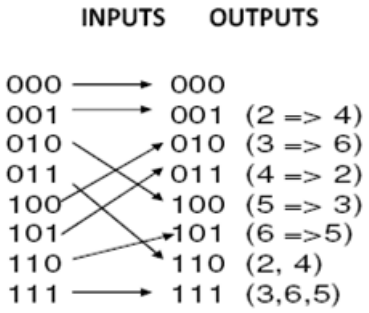
There is a risk of recurrence of a mapping between input and output vectors, there is a single output vector is the vector of input circuits of each property and vice versa. Inputs and outputs as inputs, outputs, along with the property that there is an equal number of 1s and one-to-one mapping between the vectors are reversible when the Conservative logic is the logic of the conservative. Conservative unique mapping between logic circuits vectors of inputs and outputs, if not preserved, are reversible. Researchers have proved that, if the calculation is performed with an irreversible manner, KTln2 Joules of thermal energy is lost every bit of information will be generated. From a thermodynamic point of view, it also carried out a census of the kTln2 power dissipation in a reversible way, it was proved that. Due to the destruction of information, such as the amount of energy dissipated by the system heat dissipation is an important aspect of the quantum dot cellular automata (QCA) computing, optical computing and logic flow superconductor family, etc. Nanotechnologies are emerging. Therefore, reversible logic is the fact that one of the primary motivations for the adoption of the energy dissipated in the destruction of information that are beyond the scope of Nanotechnologies KTln2 for the ultralow-power circuit design is an important factor in the design of a logic provides the total heat dissipation system. Furthermore, QCA is reversible, it is possible to implement logic gates, one in which the developing Nanotechnologies

DESIGN OF TESTABLE REVERSIBLE SEQUENTIAL CIRCUITS

BASIC GATES - BASIC REVERSIBLE GATES USED:

1. 4*4 IG Gate.
2. 3*3 F2G Gate.
3. 3*3 FG Gate.
4. 3*3 NG Gate.
5. 3*3 TG Gate.

Reversible circuits or gates are those which have one-to-one mapping between vectors of inputs and outputs. This allows the vector of output states to be used to reconstruct the vector of input states. Reversible logic can be obtained by the following relation as shown below:



2.1 IG GATE:

This paper includes a 4*4 parity preserving reversible gate, IG, as depicted in Fig. 3. The gate is one-through, which means one of the input variables is also used as the output variable.

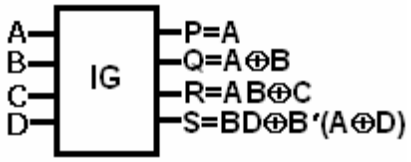


Fig 1: 4*4 IG Gate.

The truth table of this IG gate is shown in Table.1, which shows that this gate allows to uniquely determine the input pattern corresponding to particular output pattern. As the Reversible IG gate is parity preserving. This property can be verified by comparing the input parity **A** XOR **B** XOR **C** XOR **D** to the output parity **P** XOR **Q** XOR **R** XOR **S**. This Reversible IG gate is universal as it can be used to implement any arbitrary Boolean function.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Table I: Truth Table For Parity Preserving IG GATE.

A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	0
0	1	1	1	0	1	1	1
1	0	0	0	1	0	0	0
1	0	0	1	1	0	0	1
1	0	1	0	1	0	1	0
1	0	1	1	1	0	1	1
1	1	0	0	1	1	0	0
1	1	0	1	1	1	0	1
1	1	1	0	1	1	1	0
1	1	1	1	1	1	1	1

2.2 F2G GATE:

A 3*3 Double Feynman gate [18][3].The input vector is I (A, B, C) and the output vector is O (P, Q, R). The outputs are defined as

P = **A**

Q= **A** xor**B**

R=**A** xor**C**

Then the Quantum cost of double Feynman gate is 2.

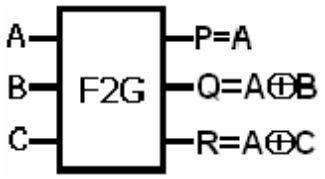


Fig 2: 3*3 Feynman Double Gate

Feynman Double gate is used as the fault tolerant copying gate when the input lines B and C are set to some constants may be '0' or '1' or as a combination of both '0' and '1'.

Table II : Truth Table For FEYNMAN DOUBLE GATE.

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

QUANTUM COMPUTER:

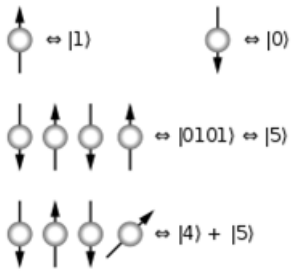
A quantum computer (also known as a quantum supercomputer) data, such as superposition and entanglement to perform operations, the direct use of quantum mechanical phenomena acomputation device. Quantum computers, digital computers are based on transistors are different. Digital computers, the data may be superpositions of states, however, binary digits (bits), two specific states (0 or 1) of quantum computational qubits (quantum bits see) one is always in use, each of which is encoded into. The quantum Turing machine is a theoretical model, known as the universal quantum computer. Quantum computers are computers that are involuntary and theoretical probability comparisons; The state has the ability to be at once an example. executed. continued and a number of both practical and theoretical research funding agencies, national governments and the military cryptanalysis, civilian and national security purposes in quantum computing research to support the development of both the quantumcomputers. Large-scale quantum computers, Shor's algorithm or the simulation of quantum many body systems using the best currently known algorithms such as integer factorization using will be able to solve certain problems much more quickly than any classical computer. Probability is possible to run applications faster than traditional algorithm Simon's algorithm, such as quantum algorithms.Given the appropriate computing resources, however, a scientific computer to simulate a quantum algorithm that could be made; Quantum computation does not violate the Church-Turing thesis.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

A good computer bits, each bit represents either a one or zero, which is made up of a memory. Performs a sequence of qubits in a quantum computer. A single qubit, a zero, or a superposition of the two qubit quantum state contains; Moreover, qubits in a pair of 4 states, and 8, three qubits in any superposition is a quantum superposition, qubits in a quantum computer (up to an arbitrary number of different states at the same time, the super is to be one of these states at the same time, this compares to the simple computer). The problem is in the hands of a quantum computer represents the initial stage of a controlled qubits and quantum logic gates by setting is managed by a fixed sequence of those qubits. The sequence is called a quantum algorithm to be applied to the gates. The calculation of pure states, each qubit system of qubits is completely zero or one where one pile, a measure expires. And most classical bits of information is at the outcome. They know that only a certain quantum algorithms to provide the optimal solution with probability, often have to be drawn.

Bits vs. qubits:

Given the number of qubits in a quantum computer on a classical computer that has the same number of bits of music is fundamentally different. For example, a classical computer to represent the state of an n-qubit system needs to store 2n complex modules. This is exponentially more information than the fact that qubits that can hold their science may seem to indicate that, of all the possible care qubits states, should not overlook the fact that the super-only. When measured in the final state of the qubits, they can only be found in one of the possible configurations, they are in front of the measurement. Moreover, it was the only measure directly affect the results of the calculation, the central provinces, from the fact that the measure before the Super as a separate state was wrong to think of qubits. Qubits are made up of controlled particles and the means of control (e.g. devices that trap particles and switch them from one state to another).[10]



qubits can be in a superposition of all the clasically allowed states

REVERSIBLE CELLULAR AUTOMATON:

A reversible cellular automaton is a cellular automaton, which is located in front of each design is unique. Reversible cellular automaton is a time-reversed dynamics is always a big neighbor, perhaps, be described by another cellular automaton rule. Reversible cellular automata that many methods are known for defining the rules; However, two or more dimensions of the arrays, which are not defined by these methods for cellular automata, the reversibility is undecidable risk test. Reversible computing is a natural model of reversible cellular automata, ultra-low-power technology that could lead to the formation of computing devices.

Quantum cellular automata, a way of performing calculations using the principles of quantum mechanics, often need to be withdrawn. In addition, one of the best gas or magnetic charges, such as the physical model of the motion of the molecules in the alignment of the many problems with icing model, naturally reversible and reversible cellular automata can be simulated by.

ENCRYPTION:

Kari (1990) anencryption system proposed using as multidimensional reversible cellular automata. Kari's proposal, cellular automaton rule is the encryption key, the encryption is performed by running the rule is a step forward, and decryption is performed by running it as a step backward. In principle, the attack automatically, undecidability of the test because of the (forward rule will be given) the encryption key from the encryption key (to reverse the rule) could not determine:

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Chai, Cao and Zhou (2005), a one-dimensional cellular automaton encryption key for each cell to determine the local administration to propose an alternative to the encryption system, and the second order is based on the principle that an automaton run by several rounds of input to output encrypted becomes transformed. Automaton relapsing feature ensures that the encrypted message can be decrypted run against the same system. In this system, the keys must be done in secret because the same key is used for both encryption and decryption.

QUANTUM COMPUTING:

Quantum cellular automata are arrays of automata whose states and state transitions obey the laws of quantum dynamics. Quantum cellular automata were suggested as a model of computation by Feynman (1982) and first formalized by Watrous (1995). Several competing notions of these automata remain under research, many of which require that the automata constructed in this way be reversible.

QUANTUM PROGRAMMING:

Quantum Quantum algorithm susing high-level programming constructs that allow the expression of a set of computer programming languages. Each point of the quantum of languages, provides a tool for programmers, but Quantum reason formally about the algorithms for calculating the quantum of work and not so much to provide the tools to understand how researchers.Quantum Quantum is imperative programming languages, programming languages and applications: One can single out the two main groups of quantum programming languages. The first group are the most prominent representatives of the QCL and LanQ. Quantum computing efforts are underway for the development of functional programming languages. Examples are QPL of Selinger, and by Grattage Altenkirch and Haskell-like language QML. Higher-order quantum programming languages, based on the lambda calculus, Van Tonder, Selinger and Valiron proposed by and by Arrighi and Dowek. Simon Gay Quantum Programming Languages The survey of the state of research and a comprehensive bibliography of resources in 2007, Quantum provides information about programming.

IMPERATIVE QUANTUM PROGRAMMING LANGUAGES:

Quantum pseudocode:

E. Knill's Quantum Quantum algorithms pseudocode description of the first principles of the language. It was introduced, moreover, tightly Quantum Random Access Machine (QRAM) was connected with a model of the quantum machine.

Quantum computing language:

QCL (Quantum Computation Language) is one of the first to run the quantum programming languages. Syntaxresembles C programming language and the syntax of C. One primitive data types, data types for its music, the same program can be combined with scientific code and are similar to the quantum code.
Built-in data type, primary QCL Quantum qureg (see quantum register) is. It qubits (quantum bits to look at) can be interpreted as a series.

Quipper:

Quipper 2013 was published in, which is the language of the host using Haskell, an embedded language is executed. For this reason, the quantum of the programs are provided by Quipper using libraries written in Haskell.
For example, the following code implements the preparation of superposition import Quipper

```
spos :: Bool ->Circ Qubit
spos b = do
    q <- qinit b
    r <- hadamard q
return r
```

QUANTUM GATE:

Especially quantum computing and quantum circuit model of computation, a quantum gate (or quantum logic gate) is an important quantum circuit is operating in a small number of qubits. They are quantum circuits, such as music, logic gates are the building

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

blocks of a conventional digital circuits. Apart from scientific logic gates, quantum logic gates are reversible. However, the music is performed using computing only reversible gates. For example, all of the Boolean functions can be reversible Toffoli gate. The gate circuits of the classical quantum circuits can perform all operations performed by the quantum equivalent of a live show is. Quantum logic gates are represented by unitary matrices. The most common quantum gates, one or two qubits to work in places of work in the general scientific logic gates, such as one or two bits. As the matrix, quantum gates 2 × 2 or 4 × 4 unitary matrices characterized by the means.

STUCK-AT FAULT:

A stuck-at fault is a manufacturing defect within an integrated circuit to simulate the fault simulation and automatic test pattern generation (ATPG) tools to a specific fault model. Personal signs and pins, which are assumed to remain at logical '1', '0' and 'X'. For example, an output behavior can be seen in the type of error to ensure that the test is a specific test pattern generation is linked to the logical 1 state. Similarly, the output will not change its output pin to model the behavior of a defective circuit could be associated with a logical 0. All faults stuck-at fault model cannot be analyzed. Static risks, are signs of the branches, compensation for the use of this model as a circuit untestable. Also, redundant circuits as a result of the same mistake will not be any change to any output by design, because it cannot be tested using this model. At the same installment of the line A wrong model uses a single hard-line digital circuits. Test design, testing is used for the preparation of the post. The model in the digital circuit node to a line or stuck at a low logic assumes a high or logic. When a line is difficult, it is wrong.

Digital circuits can be divided into:

1. Gate level or the combination consisting of the storage circuits (latches and / or flip-flops), but Nand, OR, XOR, etc., only the gates
2. Sequential circuits consisting of storage.

The error model of the gate-level circuits, or can be separated from the storage elements, it applies to a block of one of the series circuit. Wrong is wrong even if it is difficult to model input into a gate, a test that can detect a single error could make it easier to find multiple faults, one assumes that the time is wrong. This error model, in turn, each input pin of each gate-to-use, considered to be grounded, and the circuit is wrong to refer to the development of a test vector. The test vector of bits applied to the inputs of a collection of circuits, and at the output of the circuit is expected to be a collection of bits. If the gate is grounded in consideration of the pin, the test vector is applied to the circuit, the output bits do not agree with at least one test vector corresponding to the output bit. After obtaining the test vectors for the grounded pins, each pin in turn is connected to a logic one and another set of test vectors can be used to identify faults that occur in these situations. Each of these faults in a row at the same stuck-at 0 or 1 fault is the same difficulty. faults. CMOS test pattern is the same for the working medium, it can detect all possible faults in CMOS. Bus connections to drive array models, the pins of the adjacent structures, bridging between the lines of the signal fails to detect faults. However, the most widely used one is difficult at the faults, and has allowed for some additional tests, feeling bad for the industry to transport a small number of circuits is acceptable.

This model is based on the examination of the many things can be achieved by:

1. In the same stuck-at faults in a test, the other stuck-at fault is often the development of a large number of finds.
2. tests for stuck-at faults are often completely through serendipity, such a stuck-open faults and other faults, you will find a large number. It is sometimes a "windfall" is the wrong coverage.
3. IDDQ test another type of test that measures the path of the integrated circuit changes when applied to a small number of test vectors are changing slowly, a CMOS power supply current. So it draws very little

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

power when CMOS static investment, any increase in the current indicates a potential problem.

Simulation Results

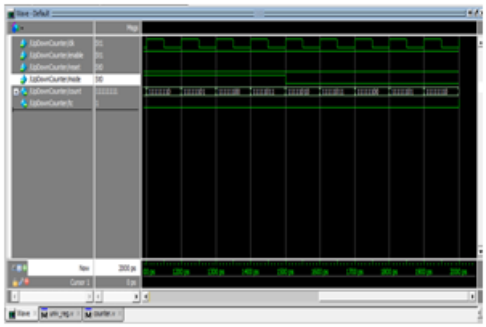


Fig: Updown Counter waveform

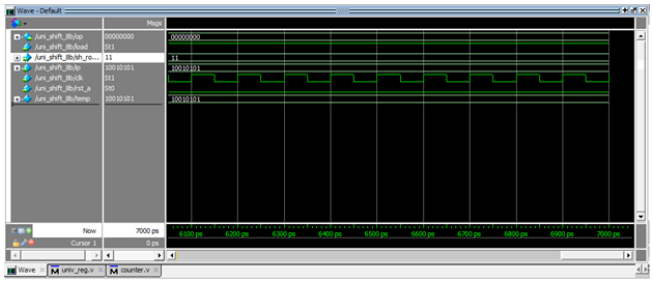


Fig: wave form for universal register

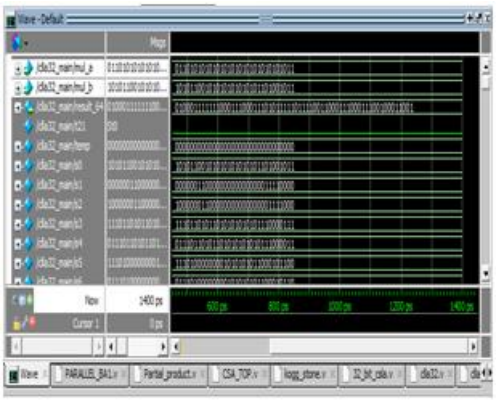


Fig: simulation result for CLAA reversible circuit

Conclusion:

An improved synthesis of this work will be displayed in sequential reversible circuits. Four examples of design is asynchronous loading it down with a bit of a falling-edge counter / triggered and shown four bit falling edge triggered Universal Register. We spent Quantum and that are offered in two variants, with the ancilla compare inputs.

The design of the new counter design when compared to the same number of inputs and quantum ancilla cost savings of 21.28% The design of the new register over a 16.67% increase in the quantum of inputs ancilla cost savings of 33.93%. Automation of process mapping and testability are under consideration for future work.

TABLE III. COMPARISON OF CIRCUIT COMPLEXITY OF THE PROPOSED METHOD WITH THAT IN [3]

Circuit	Present work		Work in [3]		% Improvement over [3]	
	QC	AI	QC	AI	QC	AI
Four-bit falling-edge trigered up/down counter with asynchronous load	74	8	94	8	21.28	0
Four-bit falling-edge triggered universal register	74	14	112	12	33.93	-16.67

QC = quantum cost, AI = ancilla inputs

REFERENCES:

[1] T. Toffoli, “Reversible computing,” MIT Lab. Comput. Sci., Cambridge, MA, USA, Tech. Rep. MIT/LCS/TM-151, 1980.

[2] H. Thapliyal, N. Ranganathan, and S. Kotiyal, "Design of testable reversible sequential circuits," IEEE Trans. VLSI Syst., vol. 21, no. 7,pp. 1201-1209, 2013.

[3] M. H. A. Khan, "Design of reversible synchronous sequential circuitsusing pseudo Reed-Muller expressions," IEEE Trans. VLSI Syst., vol.22, no. 11, pp. 2278-2286, 2014.

[4] V. V. Shende, A. K. Prasad, I. L. Markov, and J. P. Hayes, “Synthesis of reversible logic circuits,” IEEE Trans. on Computer-Aided Designof Integrated Circuits and Systems, vol. 22, no. 6, pp. 710–722, Jun.2003.

[5] J. E. Rice, “A new look at reversible memory elements,” in Proc. IEEE ISCAS, May 2006, pp. 243–246.

[6] S. K. S. Hari, S. Shroff, S. N. Mohammad, and V. Kamakoti, “Efficient building blocks for reversible sequential circuit design,” inProc. 49th IEEE MWSCAS, Aug. 2006, pp. 437–441.\

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

[7] H. Thapliyal and A. P. Vinod, "Design of reversible sequential elements with feasibility of transistor implementation," in Proc. ISCAS, 2007, pp. 625–628.

[8] M.-L. Chuang and C.-Y. Wang, "Synthesis of reversible sequential elements," ACM J. Emerg. Technol., vol. 3, no. 4, pp. 1–19, 2008.

[9] H. Thapliyal and N. Ranganathan, "Design of reversible sequential circuits optimizing quantum cost, delay and garbage outputs," ACM J. Emerg. Technol. Comput. Syst., vol. 6, no. 4, pp. 14:1–14:35, 2008.

[10] M. Haghparast and M. S. Gharajeh, "Design of a nanometric reversible 4-bit binary counter with parallel load," Austral. J. Basic Appl. Sci., vol. 5, no. 7, pp. 63–71, 2011.