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Design of Low Power and Area Non-Redundant Radix-4 Signed-Digit (NR4SD) Encoding

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Abstract:
In this paper, we present an engineering of pre-encoded multipliers for Digital Signal Processing applications based on disconnected encoding of coefficients. To this augment, the Non-Redundant radix-4 Signed-Digit (NR4SD) encoding method, which utilizes the digit values {-1, 0, +1, +2} or {-2,-1,0,+1} is proposed prompting to a multiplier outline with less unpredictable incomplete items execution. Broad trial examination confirms that the proposed pre-encoded NR4SD multipliers, including the coefficients memory, are more area and power productive than the traditional Modified Booth plot.

Keywords: ***Digital Signal Processing, Fourier Transform, Modified Booth Encoding, Pre-encoded Multipliers, NR4SD***

1. Introduction:

Multimedia and Digital Signal Processing (DSP) applications (e.g., Fast Fourier Transform (FFT), sound/video CoDecs) complete a substantial number of augmentations with coefficients that don't change amid the execution of the application. Since the multiplier is a fundamental part to implement computationally escalated applications, its design genuinely influences their execution. Consistent coefficients can be encoded to contain the slightest non-zero digits utilizing the Canonic Signed Digit (CSD) representation [1]. CSD multipliers contain the least non-zero fractional items, which in turn diminishes their exchanging action. Be that as it may, the CSD encoding includes genuine constraints. Collapsing method [2], which diminishes silicon region by time multiplexing numerous operations into single practical units, e.g., adders, multipliers, is not doable as the CSD-based multipliers are hard-wired to particular coefficients. In [3], a CSD-based programmable multiplier configuration was proposed for gatherings of pre-decided coefficients that share certain elements. The extent of ROM used to store the gatherings of coefficients is fundamentally diminished and in addition the region and power utilization of the circuit. Nonetheless, this multiplier configuration needs adaptability since the fractional items era unit is composed particularly for a gathering of coefficients and can't be reused for another gathering. Likewise, this strategy can't be effectively stretched out to vast gatherings of pre-decided coefficients accomplishing at the same time high proficiency. Adjusted Booth (MB) encoding [4]–[7] handles the previously mentioned restrictions and diminishes to a large portion of the number of incomplete items coming about to diminished territory, basic deferral and power utilization. Be that as it may, a devoted encoding circuit is required and the incomplete items era is more mind boggling. In [8], Kim et al. proposed a strategy like [3], for planning productive MB multipliers for gatherings of pre-decided coefficients with similar restrictions portrayed in the past section.

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In [9], [10], multipliers incorporated into butterfly units of FFT processors utilize standard coefficients put away in ROMs. In sound [11], [12] and video [13], [14] CoDecs, altered coefficients put away in memory, are utilized as augmentation information sources. Since the estimations of steady coefficients are known ahead of time, we encode the coefficients disconnected in light of the MB encoding and store the MB encoded coefficients (i.e., 3 bits for every digit) into a ROM. Utilizing this procedure [15]–[17], the encoding circuit of the MB multiplier is precluded. We allude to this outline as pre-encoded MB multiplier. At that point, we investigate a Non-Redundant radix-4 Signed- Digit (NR4SD) encoding plan developing the serial encoding systems of [6], [18]. The proposed NR4SD encoding plan utilizes one of the accompanying arrangements of digit values: {-1,0,+1,+2} or {-2,-1,0,+1}. All together to cover the dynamic scope of the 2's supplement shape, all digits of the proposed representation are encoded as per NR4SD aside from the most huge one that is MB encoded. Utilizing the proposed encoding recipe, we pre-encode the standard coefficients and store them into a ROM in a consolidated shape (i.e.,2 bits for each digit). Contrasted with the pre-encoded MB multiplier in which the encoded coefficients require 3 bits per digit, the proposed NR4SD plot lessens the memory estimate. Likewise, contrasted with the MB frame, which utilizes five digit values{-2,-1,0,+1,+2}, the proposed NR4SD encoding utilizes four digit values.

Consequently, the NR4SD-based pre-encoded multipliers incorporate a less complex partial products generation circuit. We investigate the productivity of the previously mentioned pre-encoded multipliers considering the size of the coefficients' ROM.

2. Modified Booth Algorithm:

Modified Booth (MB) is a redundant radix-4 encoding technique [6], [7]. Considering the multiplication of the 2's complement numbers A, B, each one consisting of n=2k bits, B can be represented in MB form as:

$$B = (b_{n-1} \dots \dots \dots \dots b_0)_{2's}$$

$$= -b_{2k-1}2^{2k-1} + \sum_{t=0}^{2k-2} b_t 2^t$$

$$= \left(b_{k-1}^{MB} \dots \dots \dots \dots b_0^{MB}\right)MB = \sum_{j=0}^{k-1} b_j^{MB} 2^{2j}$$

Digits $b_j^{MB} \in \{-2,-1,0,+1,+2\}, 0 \le j \le k-1$, are formed as follows:

$$b_j^{MB} = -2b_{2j+1} + b_{2j} + b_{2j-1}$$

whereb_{-1}. Each MB digit is represented by the bits s, one and two (Table 1). The bit s shows if the digit is negative (s=1) or positive (s=0). One shows if the absolute value of a digit equals 1 (one=1) or not (one=0). Two shows if the absolute value of a digit equals 2 (two=1) or not (two=0). Using these bits, we calculate the MB digits b_j^{MB} as follows:

$$b_j^{MB} = (-1)^{sj}.(one_j + 2two_j)$$

Equations (4) form the MB encoding signals.

$$s_j = b_{2j+1}, one_j = b_{2j-1} + b_{2j}$$

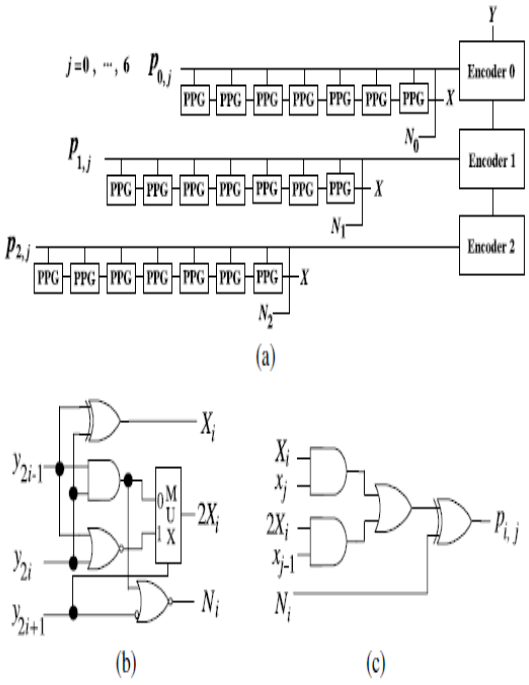

Fig 1: × 6 modified Booth multiplier: (a) interconnection of encoders and PPG's, (b) Booth encoder, and (c) PPG circuit.

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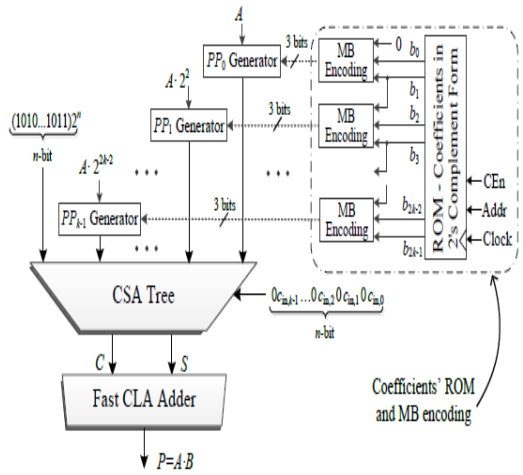

Fig 2: System Architecture of Conventional MB Multiplier

3. Proposed Algorithm:

We present the Non-Redundant radix-4 Signed-Digit (NR4SD) encoding technique. As in MB form, the number of partial products is reduced to half. When encoding the 2's complement number B, digits b_j^{NR-} take one of four values {-1,0,+1,+2}or b_j^{NR+} {-2,-1,0,+1} at the NR4SD or NR4SD+algorithm, respectively. Only four different values are used and not five as in MB algorithm, which leads to 0 j k 2. As we need to cover the dynamic range of the 2's complement form, the most significant digit is MB encoded (i.e., b_{k-1}^{MB} -2,-1,0,+1,+2)The NR4SD and NR4SD+encoding algorithms are illustrated in detail in Fig. 1 and 2, respectively.

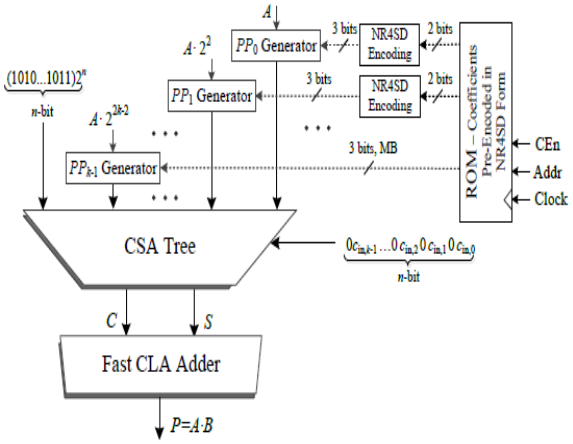

Fig 3: System Architecture of the NR4SD Multipliers

2's Complement	10000000	10011010	01011001	01111111
Integer	-128	-102	+89	+127
Modified Booth	$\bar{2}000$	$\bar{2}2\bar{1}\bar{2}$	$12\bar{2}1$	$200\bar{1}$
NR4SD$^-$	$\bar{2}000$	$\bar{1}\bar{2}\bar{1}\bar{2}$	$2\bar{2}\bar{2}1$	$200\bar{1}$
NR4SD$^+$	$\bar{2}000$	$\bar{2}122$	1121	$200\bar{1}$

Table 1: Numerical Examples of the encoding Techniques

NR4SD-- Algorithm

Step 1: Consider the initial values j = 0 and C_0=0.

Step 2: Calculate the carry C_{2j+1} and the sum n_{2j}^+ of a Half Adder (HA) with inputs b_{2j} and c_{2j} (Fig. 1a).

$$c_{2j+1} = b_{2j} \wedge c_{2j}, \quad n_{2j}^+ = b_{2j} \oplus c_{2j}.$$

Step 3: Calculate the positively signed carry $c_{2j+1}(+)$ and the negatively signed sum $n_{2j+1}^-(-)$of a Half Adder* (HA*) with inputs $b_{2j+1}(+)$ and $c_{2j+1}(+)$ (Fig. 1a). The outputs $c_{2j+1}$and n2j+1of the HA* relate to its inputs as follows:

$$2c_{2j+2} - n_{2j+1}^- = b_{2j+1} + c_{2j+1}.$$

The following Boolean equations summarize the HA* operation:

$$c_{2j+2} = b_{2j+1} \vee c_{2j+1}, \quad n_{2j+1}^- = b_{2j+1} \oplus c_{2j+1}.$$

Step 4: Calculate the value of the bNRj digit.

$$\mathbf{b}_j^{NR-} = -2n_{2j+1}^- + n_{2j}^+.$$

Equation (5) results from the fact that n_{2j+1}^- is negatively signed and n_{2j}^+ is positively signed.

Step 5: j := j + 1.

Step 6: If (j < k-1), go to Step 2. If (j = k-1), encode the most significant digit based on the MB algorithm and considering the three consecutive bits to be $b_{2k-1}, b_{2k-2} and\ c_{2k-2}$(Fig. 1b). If (j = k), stop.

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4. Results

The results after implementation have been shown below. The time analysis, power analysis reports, RTL Schematic diagrams are been showed. By which we can state the speed of the system and the area is given by stating the number of device utilization summary.

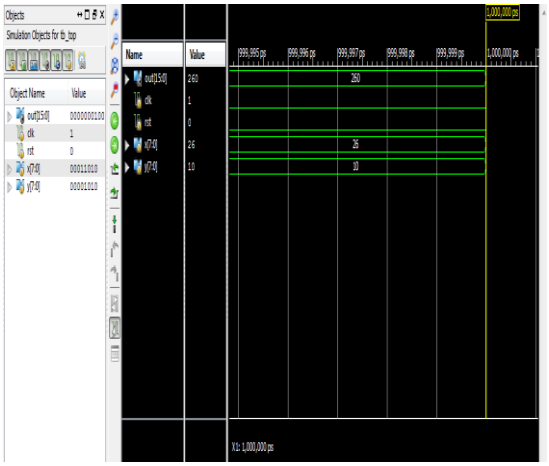

Fig 4: Output

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Latches	8	1,920	1%	
Number of 4 input LUTs	209	1,920	10%	
Number of occupied Slices	118	960	12%	
Number of Slices containing only related logic	118	118	100%	
Number of Slices containing unrelated logic	0	118	0%	
Total Number of 4 input LUTs	209	1,920	10%	
Number of bonded IOBs	34	66	51%	
IOB Flip Flops	15			
Number of BUFGMUXs	1	24	4%	
Average Fanout of Non-Clock Nets	3.75			

Fig 5: Number of LUTs, Flipflops, Latches etc used in the circuit.

```
--------------------------------------------------------------------------------
Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'
  Total number of paths / destination ports: 15 / 15
--------------------------------------------------------------------------------
Offset:              4.040ns (Levels of Logic = 1)
  Source:            out_14 (FF)
  Destination:       out<14> (PAD)
  Source Clock:      clk rising

  Data Path: out_14 to out<14>
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDR:C->Q              1   0.514   0.357  out_14 (out_14)
     OBUF:I->O                 3.169          out_14_OBUF (out<14>)
    ----------------------------------------
    Total                      4.040ns (3.683ns logic, 0.357ns route)
                                       (91.2% logic, 8.8% route)

==========================================================================
```

Fig 6: Timing analysis

```
2.3. Power Supply Summary
-------------------------------------------------
|          Power Supply Summary                 |
-------------------------------------------------
|                | Total | Dynamic | Quiescent |
-------------------------------------------------
| Supply Power (mW) | 33.59 | 0.00  |  33.59    |
-------------------------------------------------


-----------------------------------------------------------------------------------------------
|                                    Power Supply Currents                                    |
-----------------------------------------------------------------------------------------------
|   Supply Source   | Supply Voltage | Total Current (mA) | Dynamic Current (mA) | Quiescent Current (mA) |
-----------------------------------------------------------------------------------------------
| Vccint            |          1.200 |               8.20 |                 0.00 |                   8.20 |
| Vccaux            |          2.500 |               8.00 |                 0.00 |                   8.00 |
| Vcco25            |          2.500 |               1.50 |                 0.00 |                   1.50 |
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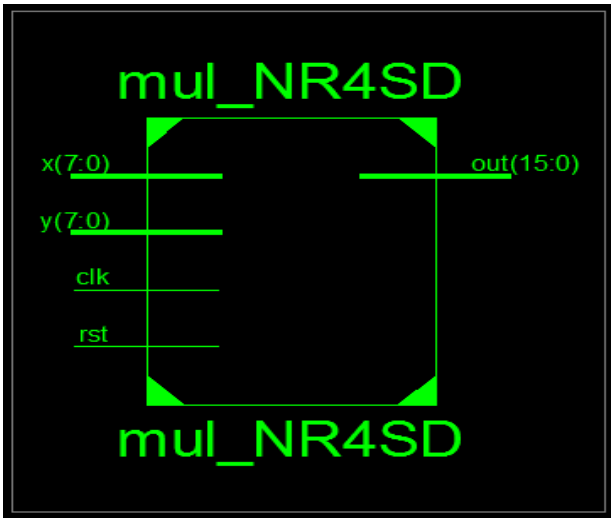
Fig 7: Power report



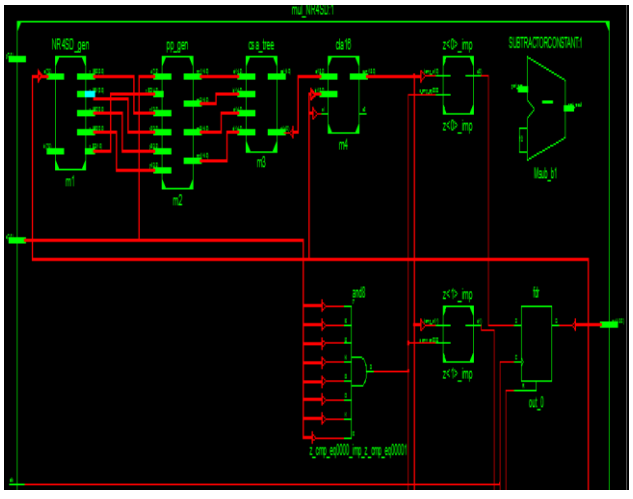


Fig 8: RTL Schematic diagram

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5. Conclusion:

New outlines of pre-encoded multipliers are investigated by disconnected encoding the standard coefficients and putting away them in framework memory. We propose encoding these coefficients in the Non-Redundant radix-4 Signed-Digit (NR4SD) shape. The proposed pre-encoded NR4SD multiplier plans are more territory and power effective contrasted with the customary and pre-encoded MB outlines. Broad exploratory examination checks the additions of the proposed pre-encoded NR4SD multipliers regarding range many-sided quality and power utilization contrasted with the customary MB multiplier.

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