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Implementation of a Low-Noise CMOS Front-End Amplifier Based on Auto Correction Feedback for Biomedical Systems

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ABSTRACT

A low-power low-noise CMOS front-end amplifier with high input impedance and high common mode rejection ratio (CMRR) is proposed in this paper, which is applied to biomedical electronics such as EEG, ECG and neural recording. By using capacitor-coupled topology, wide input common mode range and low power consumption is achieved. Chopping and auto correction feedback loop (ACFB) are employed simultaneously to reduce the low frequency noises and output ripples. The front-end amplifier has been implemented in O.ISflm process. Simulation results show that a DC gain of 117.47dB, a GBW of 1.12MHz and input impedance more than SOMO is achieved with a supply voltage of I.SV and a load capacitor of 5pF. The equivalent input noise power spectrum density (PSD) is 50.56nV/□Hz around 100Hz.

Keywords*-low noise, chopping, ripple cancellation, front-end amplifier.*

I. INTRODUCTION

Advances in microelectronics and biomedical technologies have made it possible to realize body area networks, brain computer interfaces and other kinds of implantable systems. Some important applications of these systems are to analyze EEG, ECG or neural signals for further medical diagnosis and scientific research [I]. And as revealed by biological study neural signals are typically 10-l000flV in amplitude and span a bandwidth of O. IHz-lO kHz. Due to the electrochemical effects on the surface of electrodes while being implanted in human body, a quite large DC offset will arise, which greatly challenges the design of precise front-end amplifiers featuring low noise, high CMRR, high input impedance and electrode DC offset suppression.

Meanwhile, power consumption should be minimized and bandwidth could be set wide enough for neural signals. Four gm-stage amplifiers, auto correction feedback (ACFB) loop and capacitor- coupled topologies have been used in the proposed amplifier. The capacitor-coupled topology has several merits over others such as high input impedance, raiI-to-raiI sensing and high power efficiency[l]. Meanwhile, good matching between capacitors also improves the gain accuracy and CMRR. Chopping technique is widely used for high precision CMOS amplifiers to achieve low offset and low noise, which consequently brings about high frequency ripple. On-chip filters can alleviate the ripple effectively [2], but they require more area and power consumption.

The ACFB loop which consumes less power and area, can achieve appreciable reduction of noise and ripples [3].

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II. ARCHITECTURE

Figure I shows the block diagram of the proposed amplifier. The system consists of a main amplifier based on ripple-cancellation technique, a capacitor feedback loop and impedance boosting loop [4]. The closed loop gain is fixed as 40dB by feedback capacitors Ctb and input capacitors Cin' A notch filter is utilized in the ripple-cancellation loop to suppress the ripple introduced by chopping the electrode DC offset into high frequency region.

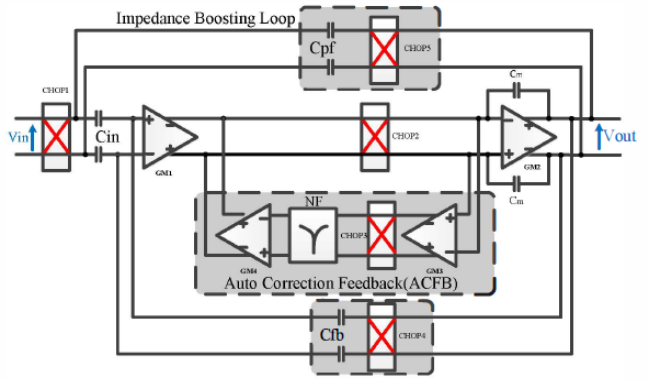

Figure I: Architecture of the whole amplifier

The Main Amplifier with ACFB The main amplifier employs ACFB loop to achieve low DC offset and low-frequency noise suppression, so the introduced ripple caused by the chopping can be reduced. The two stages of the main amplifier and the ripple cancellation loop is shown in the Figure 2. There is an unwanted initial input offset voltage associated with G_{m1}, it will be modulated by CHOP2 only, which finally appears as ripple at the output. The ripple can be attenuated by an off chip post low pass filter at the cost of reducing the bandwidth available for the signal[3]. Furthermore, it requires additional components, area and cost for its implementation. There have already been a lot of papers reported the on-chip ripple cancellation techniques. One is to employ both auto zeroing and chopping [1], whose drawback is that it requires two input stages working in ping-pong mode so that wasting much more power and chip area for input stages. Some others also employ a switched-capacitor filter in its signal path to filter the ripple out, which consequently introduces the noise penalty due to aliasing and requires complicated design for compensation network. Amplifiers employing ACFB loop are propose in this paper. [t senses the modulated ripple at its output, and forms a local feedback loop to null out the initial offset.

The proposed method is shown in Figure 1. A transconductance amplifier, paralleled to the output of the CHOP2, is employed to sense the modulated ripple, which will be demodulated down to DC by a third chopping (CHOP3) that operates with the same clock as the CHOPI and CHOP2. Then the DC signal gets through the notch filter creating a null voltage at the output of the NF. Finally the DC offset at the output of G_{ml} will be nulled by the null voltage.

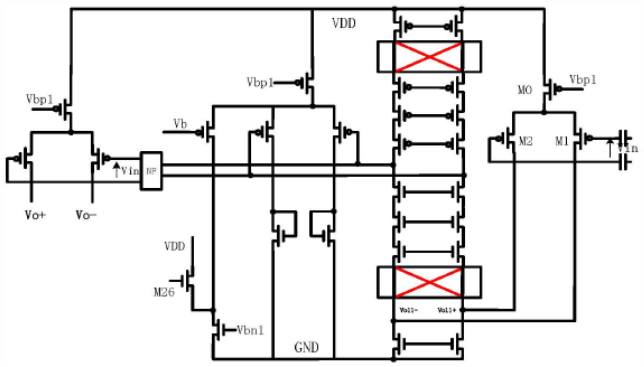

Figure 2: ACFB loop

The ACFB loop needs a really large Gm3 to ensure the whole system working in right mode. However, it will waste too much power to get this done through normal amplifier topology. So, we use a forth cascade amplifier to achieve its high gain. As shown in Figure 2, Gm3 has a gain of more than I60dB with a current below 4flA, which senses the output ripple well. M26 is working as a compensation current source to adjust the phase margin of the common mode feedback of the ACFB loop to make sure the sensed ripple will not cause oscillation. When the loop transfer function is concerned, the loop gain can be analyzed by breaking the loop into two parts. The first part is the gain from the output of notch filter to the output of CHOP2. According to Kirchhoff's voltage law:

$$\frac{G_{m4}}{2\pi j f_{chop} C_m} V_{in} + \frac{G_{m2} V_{chop}}{2\pi j f_{chop} C_L} = V_{chop} \qquad (1)$$

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Here Vchop is the output voltage of CHOP2 responding to the test voltage of Vi,,, CL is the load capacitance while Cm is the miller capacitance of Gm2. The second part is the gain from the output of CHOP2 to the breaking point. The characteristic of the sinc filter is described in [5], and the combined gain is shown in (2)

$$ACFB_2 \approx \frac{G_{m3}}{2\pi jfC_{NF}} \frac{\sin\left(\frac{\pi}{2}\frac{f}{f_{chop}}\right)}{\frac{\pi}{2}\frac{f}{f_{chop}}} \quad (2)$$

The DC gain of ACFB2 is limited by the output resistance of Gm3. So the cascode topology is essential to make it large enough to suppress the residual ripple [6]. At the same time we should take care not to have much capacitance at the output of Gm3 for it creates the conductance together with CHOP3. The overall loop gain of ACFB is

$$ACFB = \frac{G_{m4}}{(2\pi jf_{chop}C_L - G_{m2})} \frac{C_L}{C_m} \frac{G_{m3}}{2\pi jfC_{NF}} \frac{\sin\left(\frac{\pi}{2}\frac{f}{f_{chop}}\right)}{\frac{\pi}{2}f} \quad (3)$$

Chopping

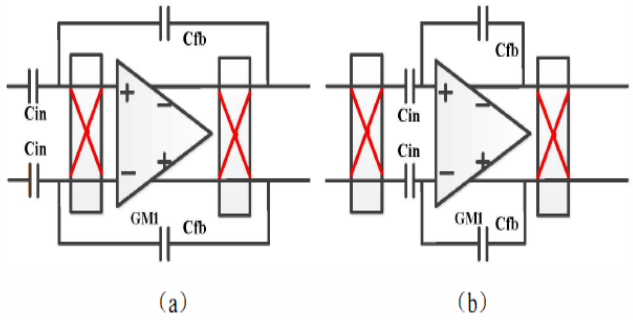

Figure 3: Two types of the location of choppers

The location of the chopping in this topology has a large influence on the performance of the front-end amplifier. As is proposed in the Figure 3(a), despite that the input offset can be filtered by the Cin, Cin has to be at least hundreds of pF to avoid noise performance deterioration, which will cost too much area. As a result we choose the topology in the Figure 3(b), in which Cin can only be several pF. Nevertheless, the unfiltered DC offset will be modulated into ripple. Thus, additional DC cancelling loop is needed.

Impedance Boosting Loop

Input impedance of Figure 1 is limited by fch' When Cin is 10pF and fch 40kHz, Rin is 1.25MO, which is too small for bio-interface. So in this topology we employed a positive feedback loop offering current to the input capacitance to boost input impedance as shown in Figure I.Here Cpf is set close to Cfb to boost impedance.

Offset Isolation Capacities

As shown in the Figure 2, in the ACFB loop what we need is a large Gm3. While the DC offset in the input of Gm2, wherever it comes from, may satisfy the third transconductance amplifier easily that would made the whole work of ACFB loop crash in vain. So in the input of Gm3 we employed two isolation capacities to separate the DC offset.

III. SIMULATION RESULTS

The Periodic-AC simulation result is shown in Figure 4 indicating that the closed-loop DC gain is 39.99dB; the bandwidth is about 10 KHz. The simulated Periodic-Noise displayed in Figure 5 shows that input referred noise within the bandwidth is 50. 56nV/'I'Hz. CMRR is more than 200dB within 10 kHz and the input impedance is boosted to more than 80MO. The ACFB loop gain and phase is showed in Figure 6, which has a pretty low bandwidth. The GBW is nearly 4.34 kHz with a phase margin of about 82.38degrees.

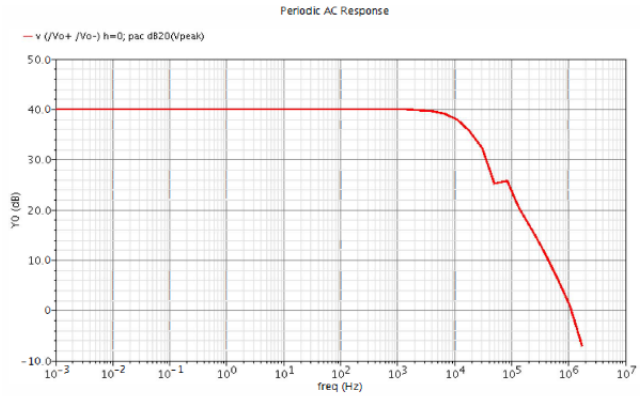

Figure 4: PAC analysis result

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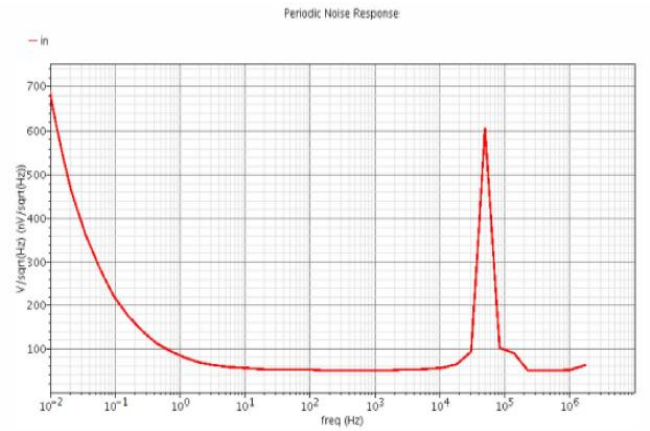

Figure 5: P-noise

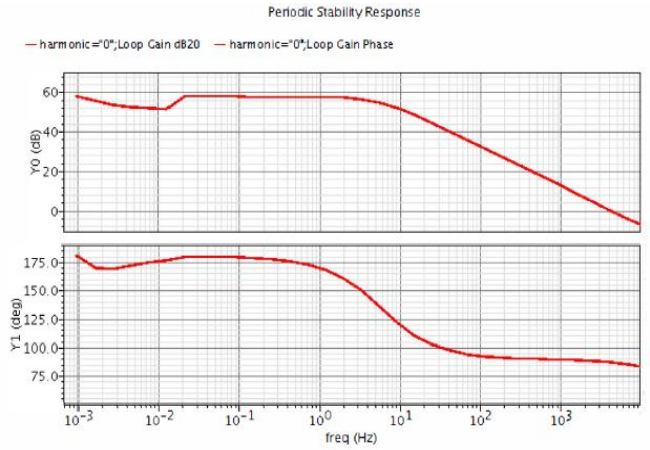

Figure 6: ACFB loop Periodic-AC result

The comparison with other amplifier is summarized in Table 1, from which it could be concluded that this proposed front-end amplifier offers technical advantages of reasonable low power, low noise, high input impedance and high CMRR for bio-signal.

IV. CONCLUSION

A front-end amplifier utilizing auto correction feedback, chopping and capacitors coupled technique is proposed, which achieves a DC gain of 40dB, a GBW of 1.2MHz and input noise as 50.561nV/'I'Hz with a load capacitance of 5pF, while consuming a total current of 72/lA with a supply of 1.8V. In comparison with some published works recently, the proposed OTA has quite good performances, which indicates that it is suitable for biomedical electronics such as EEG, ECG and neural recording.

Table 1 comparison with state -of- the -art works

	This work	[1]	[3]	[4]
Process (μm)	0.18	0.18	0.18	0.5
Voltage (V)	1.8	1	1	5.5
Current(μA)	72	3.7	500	1700
Noise (nV/√Hz)	50.56	42	50	27
CMRR (dB)	200	128	-	142
GBW (Hz)	1.12M	100k	100M	800k
Input impedance(Ω)	>80M	>80M	-	-

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