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Design and Implementation of Low Power LUT Based on Nonvolatile RRAM

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Abstract:
Emerging nonvolatile memories (NVMs), such as MRAM, prom, and RRAM, as well as a wide array of field-programmable gate for greater security and immediate energy arrays (FPGAs) have been investigated in place of SRAM configuration bits. However, NVMs and variations inherent in the process of modern logic, FPGAs bring to a matter of credibility. This is neither a matter of credibility, tolerating diversity to overcome a low-power nonvolatile lookup table (nvLUT) circuit contact. Because of the large ROFF / RON, 1T1R RRAM cell configuration bit and a reference resistor provides a sufficient margin of sense. The clamp voltage without impairing the reliability of a single-stage sense amplifier is employed to reduce power and area. Matched the forecast path for reliable sensing the parasitic RC proposed to reduce the imbalance. A reduction of 22% to 38% reduction in the delay in the evaluation of the power, and reliability of the 2.5 × typical RON or ROFF tolerance

Keywords:
low power, high speed, RRAM, FPGA- (Field Programmable Gate Array), non-volatile SRAM (nvSRAM).

INTRODUCTION:

Such MRAM, PROM, and RRAM primary NVMs, logic compatibility of good quality and have been checked. FPGAs in the core building block of logic-in-memory concept, but the inconsistency has been introduced based on the lookup table.

First, MRAM and RRAM various nonvolatile SRAM (nvSRAM) structures have been proposed to replace the non-volatile SRAM to achieve the classic look of the table. However, nvSRAM substantially larger than the cell size of the SRAM, and the writing half of the selected disturbance RRAM cells is also difficult to avoid. Refer to the table combined with the proposed use of the NVM. NVSRAM SRAM replacement of MRAM and RRAM. But the drawback is that there will be more in the area of need. Nonvolatile memory, a 2-input look at it in the run-time reconfiguration is proposed for the table. The third type MRAM is a hybrid LUT. Defective -Roff / low margin and a large area, resulting in a sense of MRAM <prom or RRAM> Ron. It is a large Roff / Ron 1T1RAM ratio has been used as a bit cell configuration and a reference to the appropriate sense resistor is used to provide the margin. And the area of the clamp voltage reduces the power used by a single-stage amplifier. At the same time, and the logic of diversity MRP lowpower, high in efficiency, and low leakage sensing against the reliable way to forecast the selected path for the MUX devised to reduce the imbalance between the parasitic RC.

1.1. Resistive Random Access Memory (RRAM):

Fabricated with 90nm CMOS technology, which is integrated into the top of the programmable resistors - the pattern of a traditional island-style FPGA (Field Programmable Gate Array) is. Apart from the configuration memory, and other components are constructed entirely with CMOS transistors. CMOS logic is interleaved across the memory array tile. Row and column decoders and sense amplifiers shared between FPGA boards, write drivers.

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Access through the transistor connected to the cell - - up or down topology 1T2R memory cells, in which the two programmable resistances (or PRS), a bit line, pulling behave like a voltage divider constructed using. 24 F2, which is just the size of the CMOS feature optimized cell surface are small compared to the PRS RRAM.

1.2. FPGAs:

An FPGA (Field Programmable Gate Array) is inherently complex digital circuits containing hundreds of thousands of logic gates that connect together to build a chip. Given below are a few steps. It is the user (customer or architect) can be set after the completion of the process of manufacturing a semiconductor device. The term "field-programmable" device to the customer, not the manufacturer to understand the program. It is designed to provide some partial re-configuration.

2. SINGLE STAGE SENSE VOLTAGE AMPLIFIER:

It has low power dissipation and a sense of basic differential amplifier in comparison to the offset voltage. The differential voltage sensing operation, providing fast loading equipment for simultaneous exchange of meaning is the primary purpose of the amplifier. SSAVC rail-to-rail voltage logic state changes the resistance of the RRAM. Outb the low end and the output clock is the clock even more sense when the precharge to VDD. CLK charges a capacitor or a waste of considerable power, as a result, when discharged to the ground. The sense amplifier may suffer reduced clamp voltage currents, large ROFF / RRAM Ron still without impairing the validity of the concept helps to preserve the margin. Compared with the previous two-stage sense amplifier, a single-stage realization of an area of the lower die. M7 and M8 on the gates of the clamp voltage Vbias, VDD is less than that applied to the inside of the selected nodes in the TMUX and MRP only (V bias Vth) to be precharged.

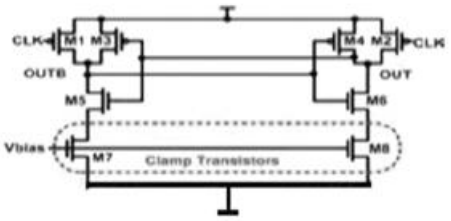

Figure 1: Single-Stage Sense Amplifier with Voltage Clamp

2.1 DESIGN OF SINGLE STAGE SENSE AMPLIFIER WITH VOLTAGE CLAMP

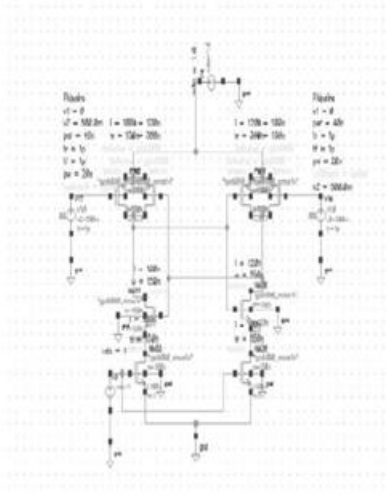

Figure 1.1: Schematic of single-stage sense amplifier with voltage clamp

Waveform:

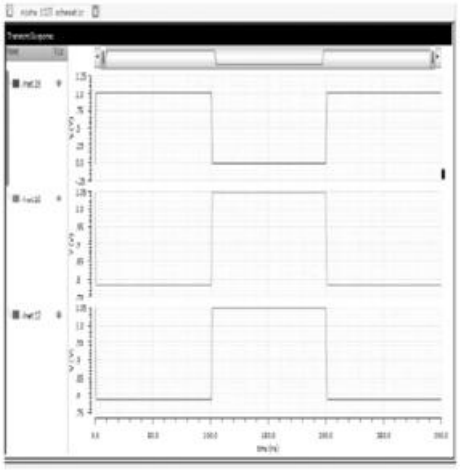

Figure 1.2: Transient Response of single-stage sense amplifier with voltage clamp

3.TERMINAL MULTIPLEXER:

TMUX is a multiplexer with select line in0 and in1 which are used to select the corresponding RRAM . Its working principle is similar to nor operation.

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IN0	IN1	OUT
0	0	R0
0	1	R1
1	0	R2
1	1	R3

EXISTING SYSTEM:

Such MRAM, PROM, and RRAM emerging NVMs, good quality and logic compatibility has been confirmed. FPGAs in the core building block of logic-in-memory concept, but inconsistency has been proposed based on the lookup table. First, MRAM and RRAM various nonvolatile SRAM (nvSRAM) structures have been proposed to replace the non-volatile SRAM to achieve the classic look of the table. However, nvSRAM substantially larger than the cell size of the SRAM, and the writing half of the selected disturbance RRAM cells is also difficult to avoid. For MRAM, Suzuki et al. Nonvolatile two-input lookup table (nvLUT) low-power current-mode logic is based on the proposed MRAM. Suzuki et al. Also acquire sufficient sensing margin of serial / parallel magnetic junctions nvLUT proposed a six input. Zhao et al. NvLUT proposed another MRAM-based run-time reconfiguration. LUT2 hybrid Wren proposed a third type of MRAM-based nvLUT. However, MRAM's ROFF / RON small PRAM or RRAM, the serial / parallel magnetic junctions, seems low compared to the margin, or as a result of a large area.

PROPOSED SYSTEM:

To illustrate the proposed design, the input nvLUT presented as shown in Fig. 1. The input is all too easily be extended to six in the current mainstream FPGA products. the format of nvLUT SSAVC, a tree Multiplexer (TMUX), a MRP, a RRAM piece, and will have an footer transistor. RRAM as a reference resistor blanks at the right-most slice of the RRAM cell configuration forms for the left and four 1T1R RRAM cells.

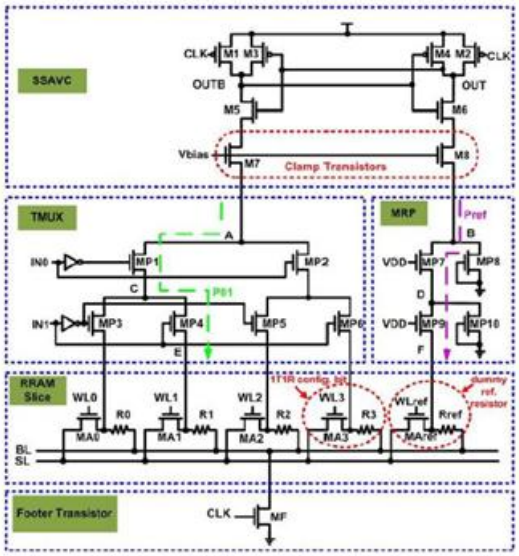
Advantages:

- reduce RC mismatch parasitic
- reduce the power

Disadvantages:

- high RC mismatch parasitic
- high power consumption

4. PROPOSED LOW POWER VARIATION TOLERANT NVLUT



To illustrate the design, the input nvLUT presented as shown in Fig. 3, the input count is even easier FPGA products in the main stream of the six, expanded. Of the total construction nvLUT a SSAVC, a tree Multiplexer (TMUX), a MRP, a RRAM piece, and will have an footer transistor. RRAM as a reference resistor blanks at the right-most slice of the RRAM cell configuration forms for the left and four 1T1R RRAM cells. The truth table logic voltage SRAM is different from the resistance of the state, ROFF or RON, will be stored in the form of a piece of RRAM. For example, a NOR gate, in order to nvLUT program, R0 RON 1, as indicated, R1, R2, and R3 ROFF represents 0. The inputs IN0 and IN1 TMUX of the RRAM cell to select the program to the program. RRT in the sense amplifier to the output 1 to be exposed to high parasitic RC bit and reference resistor, making the

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configuration of the memory margin between the resistance variation is subtle, reference may be slow discharge path.

Table
Specifications of Proposed Design

Module	Device	W/L
SSAVC	M1,M2	150nm/100nm
	M3,M4	300nm/120nm
	M5,M6	150nm/120nm
	M7,M8	150nm/100nm
TMUX	MP1 to MP6	300nm/100nm
MRP	MP7 to MP10	300nm/100nm
RRAM	MA0,MA1,MA3,MAref	300nm/100nm
Footer	MF	500nm/100nm

Simulation Results:

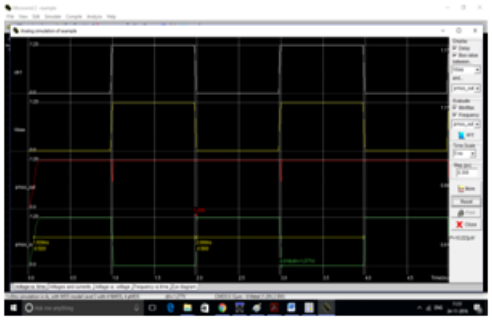

Fig: waveform for single stage sense amplifier

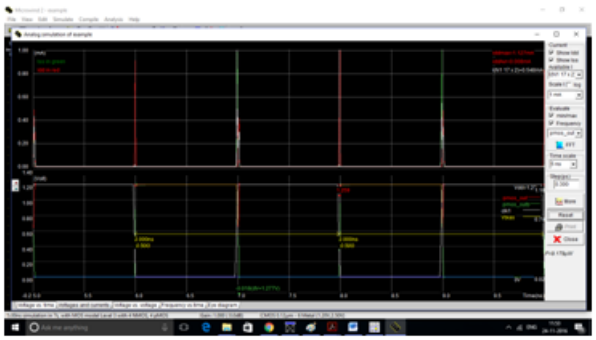

Fig: wave form for voltage vs current in sense amplifier

Fig: voltage vs time wave form for top design

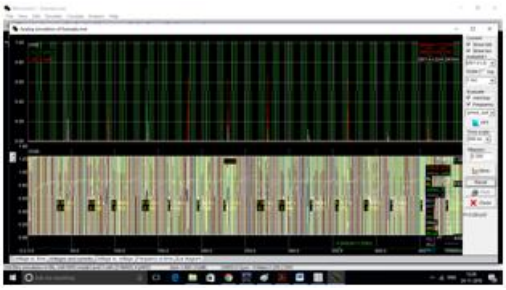

Fig: voltage vs current waveform for top design

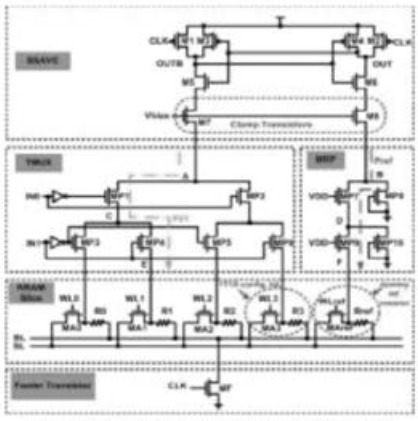

Figure 3: Low- power variation-tolerant nvLUT based on RRAM

DESIGN OF LOW-POWER VARIATION-TOLERANT NVLUT FOR RRAM:

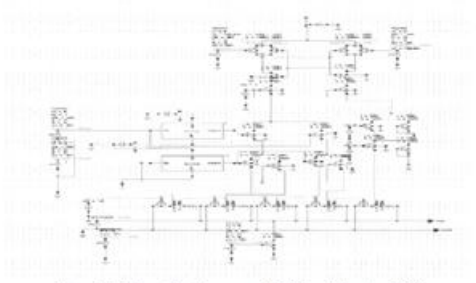

Figure 3.1: Schematic of Low-power Variation-Tolerant nvLUT

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Wave form:

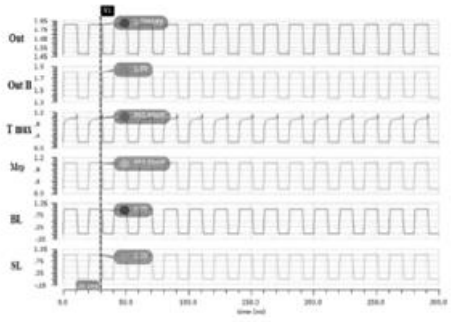

Figure 3.2: Transient Response of Low-power Variation-Tolerant nvLUT

DELAY VS VBIAS:

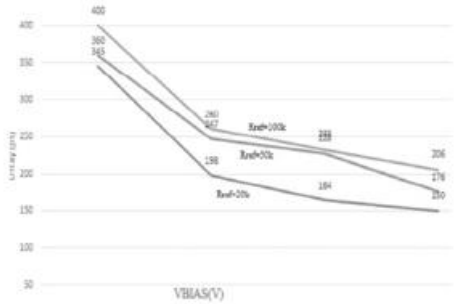

Figure 3.4: Delay of Low Power Variation Tolerant nv LUT with Vbias for different Rref value

WAVEFORM FOR DELAY CALCULATION:

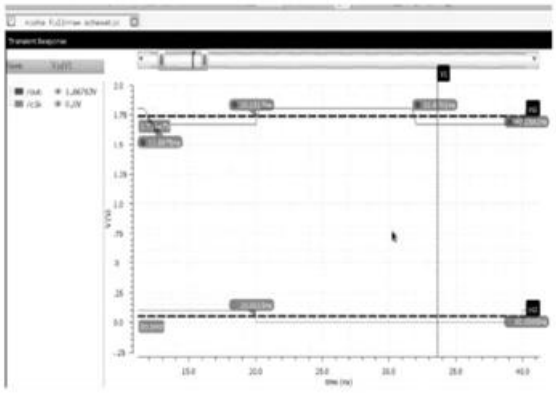

Figure 3.3: Transient Response of Delay calculation

Table 1
Delay Calculation for Rref-20K

Vbias (v)	Clock	Out	Delay(ps)
0.6	152.1062ns	151.8602ns	345ps
0.7	100.001ns	100.1706ns	198ps
0.8	100.0015ns	100.2005ns	164ps
1	100.0015	100.2165	150ps

Table 2
Delay Calculation for Rref-50K

Vbias (v)	Clock	Out	Delay(ps)
0.6	152.1062ns	151.8024ns	360ps
0.7	40.24771ns	40.00063ns	247ps
0.8	40.2285ns	40.0005ns	228ps
1	60.0014ns	60.1779ns	176ps

Table 3
Delay Calculation for Rref-100K

Vbias(v)	Clock	Out	Delay(ps)
0.6	20.00015ns	20.4727ns	400ps
0.7	40.0004ns	40.2699ns	269ps
0.8	40.00058ns	40.23375ns	233ps
1	60.0012ns	60.2086ns	206ps

POWER CALCULATION:

Table 4
Power Calculation

Vbias (v)	Rref=20K	Rref=50K	Rref=100K
	Power	Power	Power
0.5	100.6E-6	100.5E-6	100.5E-6
0.6	100.8E-6	100.7E-6	100.7E-6
0.7	101.1E-6	101.0E-6	100.9E-6
0.9	101.3E-6	101.4E-6	101.3E-6
1	101.5E-6	101.6E-6	101.6E-6

POWER VS VBIAS:

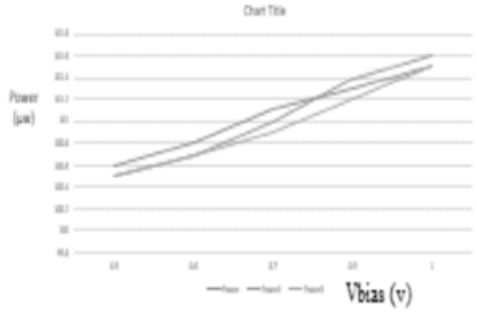

Figure 3.5: Power of Low Power Variation Tolerant nvLUT with Vbias for different Rref value

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Table 5
Product Calculation for Rref-20K

Vbias (v)	Delay(ps)	Power (μW)	Product (ps*μW)
0.6	345	100.8E-6	34.776E-15
0.7	198	101.1E-6	20.017E-15
0.8	164	101.3E-6	16.613E-15
1	150	101.5E-6	15.225E-15

Table 6
Product Calculation for Rref-50K

Vbias (v)	Delay(ps)	Power (μW)	Product (ps*μW)
0.6	360	100.7E-6	36.525E-15
0.7	247	101.0E-6	20.017E-15
0.8	228	101.4E-6	23.119E-15
1	176	101.6E-6	17.881E-15

Table 7
Product Calculation for Rref-100K

Vbias (v)	Delay(ps)	Power (μW)	Product(ps*μW)
0.6	360	100.7E-6	36.525E-15
0.7	269	100.9E-6	27.142E-15
0.8	233	101.3E-6	23.602E-15
1	206	101.6E-6	20.929E-15

PRODUCT VS VBIAS:

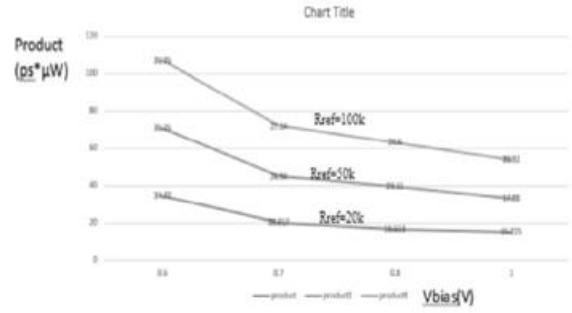
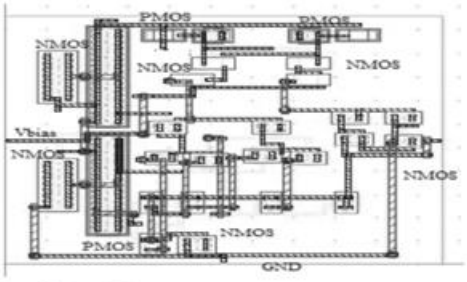


Figure 3.6: Product of Low Power Variation Tolerant nvLUT with Vbias for different Rref value

Layout OF LOW-POWER VARIATION-TOLERANT nvLUT FOR RRAM



Blue=Metal 1, Red=metal 2, yellow=polysilicon
X axis - 10.5000μm, Y axis = 10.4000μm
Area of LUT based on RRAM = 109.2 μm²

APPENDIX

Software Requirements

Micro wind/DCSH

A tool for designing and simulating the circuits Micro wind layout. Tool full editing facilities (copy, cut, past, duplicate, mobility), different views (MOS properties, 2D cross section, 3D viewer in the process), and is equipped with an analog simulator.

• DSCH software for logic design. Based on the fossil, the power circuit is built and simulated. It also includes research in the delay and power consumption.

• Silicon silicon lattice, dopants, and silicon dioxide, with emphasis, silicon atomic structure of a 3D display.
• Installation and Use
http://intrage.insatoulouse.fr/~etienne/microwind/manual_lite.pdf: User Manual - -

• http://www.microwind.org/ -Microwind3 -DSCH3 from the followings: Unzip the files to be able to work on the Micro wind . - Read the software instruction manual. - Microwind3.exe double-click to start the layout editor or Dsch3.exe the traditional start to the editor.

Tools from Micro wind:

• Micro wind
• DSCH
• Micro wind3 Editor
• Micro wind 2D viewer
• Micro wind 3D viewer
• Micro wind analog simulator
• Micro wind tutorial on MOS devices
• View of Silicon Atoms

Micro wind and DSCH : NOR Example:

• We will learn both the design flow and the CAD tools.
• The specifications we are going to see may be different for different foundry and technology.
• Design Example (3 Levels) : NOR Gate – Logic Design – Circuit Design – Layout Design

CONCLUSION:

See the table on the basis of high-density asynchronous design techniques described RRAM. RRAM is. The configuration bit and a sense of the margin, and therefore provide relief from the effects of variations in the process of memory and logic adopted as the reference resistor. Because of the high ROFF / RRAM Ron, SSAVC without impairing reliability

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helps to reduce power and area. Multiplexer MRP also forecast for reliable operation in the path of the selected path is devised to reduce the imbalance between the parasitic RC. Nonvolatile RRAM based on the layout of the proposed design for high-density asynchronous LUT is implemented using the design environment and is determined by the layout of the area is109.2 μm2.

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