ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Hybrid Control Scheme of Phase-Shift Full-Bridge Series-Resonant Converter

Katla Rajesh Reddy
M.Tech
Anurag Engineering College,
Kodad,Nalgonda.

T.Veerendar
M.Tech
Anurag Engineering College,
Kodad,Nalgonda.

ABSTRACT

This paper exhibits a mixture sort full-connect dc/dc converter with high effectiveness. Utilizing a cross breed control plan with a basic circuit structure, the proposed dc/dc converter has a half and half operation mode. Under an ordinary info run, the proposed converter works as a stage move full-connect arrangement resounding converter that gives high effectiveness by applying delicate exchanging on all switches and rectifier diodes and lessening conduction misfortunes. At the point when the info is lower than the typical information run, the converter works as a dynamic cinch venture up converter that upgrades an operation range. Because of the half and half operation, the proposed converter works with bigger stage shift esteem than the traditional converters under the ordinary information range. Subsequently, the proposed converter is fit for being intended to give high power transformation proficiency and its operation reach is expanded. A 1kW model is actualized to affirm the hypothetical investigation and legitimacy of the proposed converter.

Index Terms— Full-bridge circuit, phase-shift control, active-clamp circuit.

I. INTRODUCTION

These days, requests on dc/dc converters with a powerful thickness, high productivity, and low electromagnetic obstruction (EMI) have been expanded in different modern fields. As the changing recurrence increments to get high power thickness, changing misfortunes identified with the turn-on and turn-off of the exchanging gadgets increment. Since these misfortunes constrain the expansion of the exchanging recurrence, delicate exchanging procedures are key.

Among past dc/dc converters, a stage move full-connect (PSFB) converter is appealing in light of the fact that all essential switches are turned on with zero-voltage exchanging (ZVS) without extra assistant circuits [1]. Nonetheless, the PSFB converter has some difficult issues, for example, limited ZVS scope of slacking leg switches, high power misfortunes by circling current, and voltage ringing crosswise over rectifier diodes. Particularly, with a prerequisite of wide information extend, the PSFB converter is intended to work with little stage shift esteem under the typical info run; the outline of the PSFB converter protracts the freewheeling interim and causes the inordinate circling current which expands conduction misfortunes [2], [3].

As of late, the different PSFB converters utilizing helper circuits have been presented [4]-[12]. The PSFB converters develop ZVS run or diminish the flowing current by using extra uninvolved or dynamic assistant circuits. Be that as it may, the extra circuits result in convoluted circuit design, complex control methodology, and additional force misfortunes [13]. Likewise, some PSFB converters still require the additional snubber to counteract genuine voltage ringing issue crosswise over rectifier diodes. In [14], [15], the PSFB converters utilizing an arrangement thunderous converter have been presented, to be specific, the PSFB arrangement full converters; they have numerous preferences, for example, delicate exchanging systems of all essential switches and

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

rectifier diodes, end of flowing current, diminishment of voltage weight on rectifier diodes, and a basic circuit structure. Be that as it may, when all previously mentioned PSFB converters are required to ensure a wide operation range, regardless they work with the little stage shift esteem under the typical info range. The operation with the little stage shift esteem for the most part gives high conduction misfortunes by high pinnacle current; it brings about low influence productivity. To accomplish high effectiveness under the ordinary info range and cover the wide information run, the diverse procedures are recommended. The converters in [16], [17] change the turn proportion of the transformer by utilizing extra exchanging gadgets. Despite the fact that the methodology accomplishes high productivity and guarantees the wide information run, these strategies give circuit multifaceted nature and diminishment of the transformer use.

Dynamic cinch circuits have been generally used to assimilate surge vitality put away in spillage inductance ofa transformer. Moreover, the circuits provide a soft switching technique [18], [19]. Some studies have introduced dc/dc converters combining the active-clamp circuit and voltage doubler or multiplier rectifier [20], [21]. The circuit configuration allows achieving a step-up function like a boost converter. The voltage stresses of rectifier diodes are also clamped at the output voltage and no extra snubber circuit is required.

In this paper, a novel half and half sort FB dc/dc converter with high proficiency is proposed; the converter is gotten from a mix of a PSFB arrangement thunderous converter and a dynamic cinch venture up converter with a voltage doubler circuit. Utilizing a cross breed control plan with a basic circuit structure, the proposed converter has two operation modes. Under the ordinary information go, the proposed converter works as a PSFB arrangement resounding converter. The proposed converter yields high proficiency by applying delicate exchanging strategies on all the essential switches and rectifier diodes and by lessening conduction misfortunes. At the point when the info voltage is lower than the ordinary information go, the converter works as a dynamic cinch venture up converter. In this mode, the proposed converter gives a stage - up capacity by utilizing the dynamic cinch circuit on the essential side and the voltage doubler rectifier on the optional side. Because of the cross breed operation, the proposed converter works with bigger stage shift esteem than the routine PSFB converters under the ordinary info range. In this way, the proposed converter has the accompanying points of interest:

1) Under the normal input range, the proposed converter can be designed to optimize power conversion efficiency.
2) When the input is lower than the normal input range, the proposed converter performs a step-up function, which enhances the operation range.
3) Without complex circuit structures, the converter have high efficiency under the normal input range and extends the operation range.

The principle operation of the proposed converter isrepresented in Section II. The relevant analysis is given inSection III. Finally, a 1kW prototype of the proposedconverter is implemented to confirm its theoretical analysisand validity.

II. PRINCIPLE OPERATION OF THE PROPOSED CONVERTER

Fig.1 shows a circuit diagram of the proposed converter. On the primary side of the power transformer *T*, the proposed converter has a FB circuit with one blocking diode *DB* and one clamp capacitor *Cc*. On the secondary side, there is a voltage doubler rectifier. The operation of the proposed converter can be classified into two cases. The one is a PSFB series-resonant converter mode and the other is an active-clamp step-up converter mode.

To analyze the steady-state operation of the proposed converter, several assumptions are made

1) All switches *S1*, *S2*, *S3*, and *S4* are considered as ideal switches except for their body diodes and output capacitors.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

2) The clamp capacitor *Cc* and output capacitor *Co* are large enough, so the clamp capacitor voltage *Vc*and output voltage *Vo* have no ripple voltage, respectively.
3) The transformer *T* is composed of an ideal transformer with the primary winding turns *Np*, the secondary winding turns *N*s, the magnetizing inductance *Lm*, and the leakage inductance *Llk*.
4) The capacitance of the resonant capacitors *Cr1* and *Cr2* is identical. Thus, *Cr1=Cr2*.

A. PSFB Series-resonant Converter Mode

Under the normal input voltage range, the proposedconverter is operated by phase-shift control. In thismode, *Vc*isthe same as the input voltage *Vd*and *DB* is conducted. Allswitches are driven with a constant duty ratio 0.5 and shortdead time. Fig. 2 and 3 show the operation waveforms andequivalent circuits, respectively. A detailed mode analysis isgiven as four modes.

Mode 1 [*t0, t1*]: Prior to *t0*, the switches *S1* and *S2* are in onstateand the secondary current *is* zero. The primary current*ip*flows through *DB*, *S1*, *S2*, and *Lm*. During this mode, theprimary voltage *vp*and secondary voltage *vs*of the transformer*T* are zero. Thus, the magnetizing current *i*m is constant andsatisfies as follows:

$$L_{ik}\frac{di_s(t)}{dt}=nV_d-v_{cr1}(t) \qquad (2)$$

$$i_s(t) = C_{r1}\frac{dv_{cr1}(t)}{dt} - C_{r2}\frac{dv_{cr2}(t)}{dt} \qquad (3)$$

Where *vcr1* and *vcr2* are the voltages across *Cr1* and *Cr2*, respectively. Since *Vo* is constant, the secondary current *is* can be obtained as

$$i_s(t) = C_{r1}\frac{dv_{cr1}(t)}{dt} - C_{r2}\frac{d(V_o - v_{cr1}(t))}{dt} = C_r\frac{dv_{cr1}(t)}{dt} \qquad (4)$$

Where the equivalent resonant capacitance *Cr* is *Cr1+Cr2*. Using Eqns. (2) and (4), the secondary current *is* can be calculated as

$$i_s(t) = \frac{nV_d - v_{cr1}(t_2)}{Z_r}\sin w_r(t-t_2) \qquad (5)$$

$$i_m(t) = i_p(t) = i_m(t_0). \qquad (1)$$

Mode 2 [*t1*, *t2*]: At *t*1, *S2* is turned off. Because *i*pflowing throughS2 is very low, *S2* is turned off with near zero-current.In this mode, *ip*charges *CS2* and discharges *CS4*.

Mode 3 [*t2*, *t3*]: At *t*2, the voltage across *S4* reaches zero. Atthe same time, *ip*flows through the body diode *DS4*. Thus, *S4* is turned on with zero-voltage while *DS4* is conducted. In thismode, *vs*is*nVd*where the turn ratio *n* of the transformer isgiven by*N*s/*N*p and the secondary current *is* begins to flowthrough*D1*. The state equation of this mode is written asfollows:

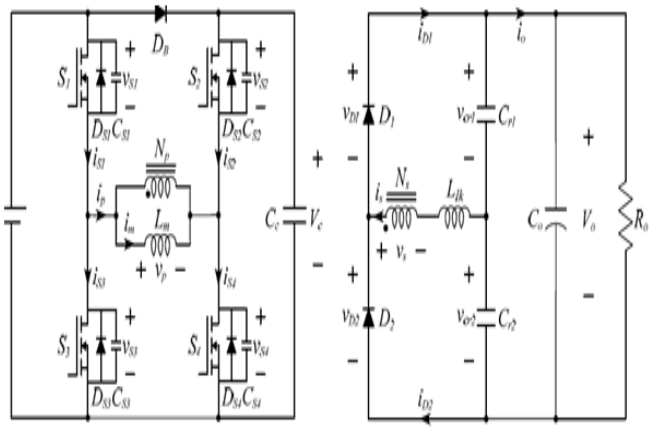

Fig. 1.Circuit diagram of the proposed hybrid-type full-bridge dc/dc converter.

The angular frequency *ωr*and characteristic impedance *Zr*are given by

$$\omega_r = \frac{1}{\sqrt{L_{lk}C_r}}, \quad Z_r = \sqrt{\frac{L_{lk}}{C_r}}. \qquad (6)$$

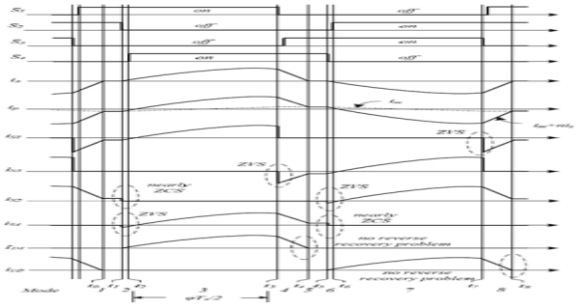

Fig. 2. Operation waveforms in the PSFB series-resonant converter mode.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

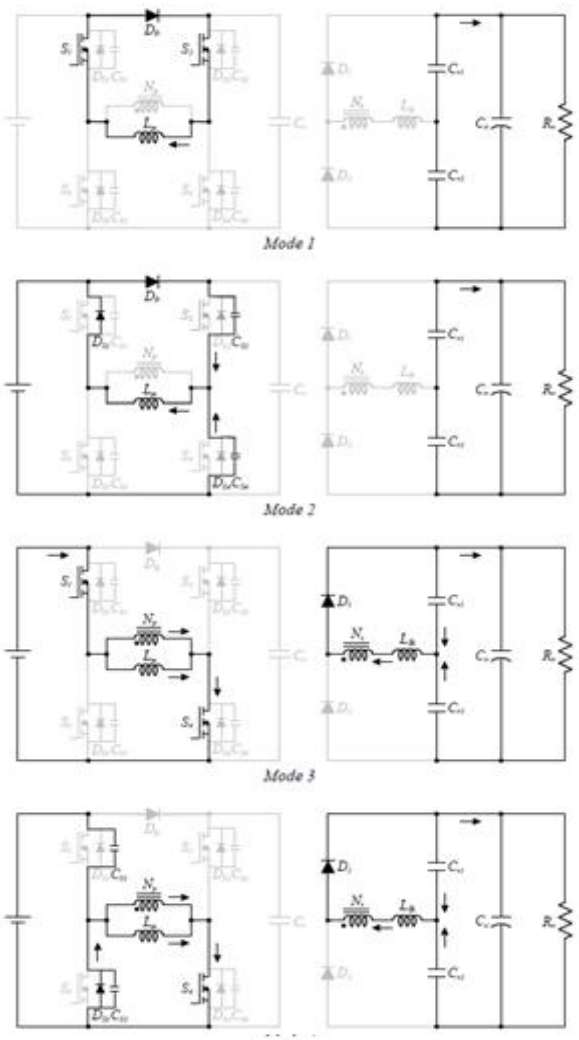

Fig. 3. Equivalent circuits during half period in the PSFB series-resonant converter mode

Mode 4 [*t3*, *t4*]: This mode begins when *S1* is turned off. Theprimary current *ip*charges *CS1* and discharges *CS3*. When thevoltage across *S3* becomes zero, *ip*flows through the bodydiode *D*S3. Thus, *S3*is turned on with zero-voltage while *DS3* isconducted. When *vp*is zero, *D1* is still conducted and *-vcr1* isapplied to *Llk*. Thus, the secondary current *is*goes to zerorapidly. End of this mode, since the secondary current is closeto zero before *D1* is reverse bias; the losses by the reverse recovery problem are small as negligible. Since operations during the next half switching period aresimilar with*Mode 1-4*, explanations of *Mode 5-8* are notpresented.

B. Active-clamp Step-up Converter Mode

As the information voltage diminishes up to a specific least estimation of the typical information go, the stage shift esteem φ increments up to its most extreme quality, 1. On the off chance that the information voltage is lower than the base estimation of the ordinary information run, the proposed converter is worked by double unbalanced heartbeat width tweak (PWM) control. The switches (S1, S4) and (S2, S3) are dealt with as switch matches and worked correlatively with short dead time. The obligation D more than 0.5 depends on (S1, S4) pair. In this circumstance, the brace capacitor voltage Vc is higher than Vd. At that point, the blocking diode DB is opposite one-sided and the proposed converter works as the dynamic clasp venture up converter. Fig. 4 and 5 demonstrate the operation waveforms and identical circuits in the dynamic clip venture up converter mode, separately.

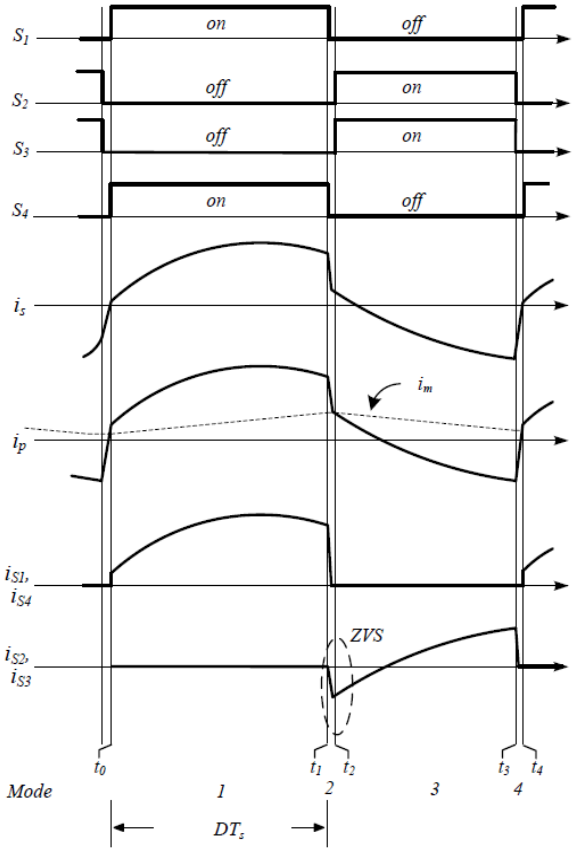

Fig. 4. Operation waveforms in the active-clamp step-up converter mode

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Mode 1 [*t0*, *t1*]: At *t0*, *S1* and *S4* are turned on. Since*Vd*isapplied to *Lm*, the magnetizing current *im* is linearly increased and is expressed as

$$\mathrm{i_m(t)} = \mathrm{i_m}\left(t_0 \frac{V_d}{L_m}(t - t_0)\right) \qquad (8)$$

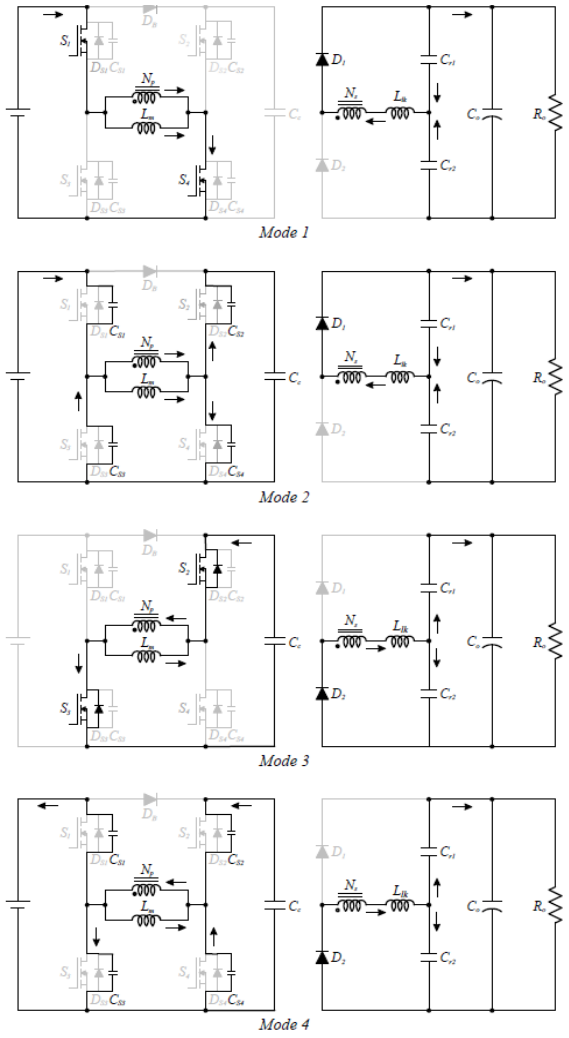

Fig. 5.Equivalent circuits during a switching period in the active-clamp step-up converter mode.

D1 is conducted and the secondary current *is* begins to resonate by *Llk*, *Cr1*, and *Cr2*. In this mode, the state equation is written as follows:

$$L_{lk}\frac{di_s(t)}{dt} = nV_d - v_{cr1}(t) \qquad (9)$$

$$i_s(t) = C_{r1}\frac{dv_{cr1}(t)}{dt} - C_{r2}\frac{dv_{cr2}(t)}{dt} = C_r\frac{dv_{cr1}(t)}{dt}. \qquad (10)$$

From Eqns. (9) and (10), the secondary current *is* can be calculated as

$$\mathrm{i_s(t)} = \mathrm{i_s}(t_3)\cos w_r(t - t_3) - \frac{nV_c - \mathrm{v_{cr2}}(t_3)}{Z_r}\sin w_r(t - t_3) \qquad (11)$$

In this mode, power is transferred from the input to the output.

Mode 2 [*t1*, *t2*]: At *t*1, *S1* and *S4* are turned off. The primary current *i*p charges and discharges the output capacitors of the switches during very short time.

Mode 3 [*t2*, *t3*]: This mode begins when the voltages across *S2* and *S3* are zero. At the same time, *i*p flows through *DS2* and *DS3*. Thus, *S2* and *S3* are turned on with zero-voltage. Since the negative voltage -*Vc*is applied to *Lm*, the magnetizing current *i*m decreases linearly as

$$\mathrm{i_m(t)} = \mathrm{i_m}(t_3) - \frac{V_c}{L_m}(t - t3) \qquad (12)$$

In this mode, the secondary current *is* begins to second resonance and the state equation is written as follows:

$$L_{lk}\frac{di_s}{dt} = v_{cr2}(t) - nV_c \qquad (13)$$

$$\mathrm{i_s(t)} = C_{r1}\frac{\mathrm{dv_{cr1}(t)}}{dt} - C_{r2}\frac{\mathrm{dv_{cr2}(t)}}{dt} = C_r\frac{\mathrm{dv_{cr2}(t)}}{dt} \qquad (14)$$

Using Eqns. (13) and (14), the secondary current is given by

$$\mathrm{i_s(t)} = \mathrm{i_s}(t_3)\cos w_r(t - t_3) - \frac{nV_c - \mathrm{v_{cr2}}(t_3)}{Z_r}\sin w_r(t - t_3) \qquad (15)$$

Mode 4 [*t3*, *t4*]: At *t3*, *S2* and *S3* are turned off. The primarycurrent *i*p charges *CS2*, *CS3* and discharges *CS1*, *CS4* during very short time.

III. ANALYSIS OF THE PROPOSED CONVERTER

In the PSFB series-resonant converter mode, *Mode 4* is neglected since the duration of *Mode 4* is relatively very short. During *Mode 3*, the secondary current *is* in Eqn. (5) flows through *D*1; the current is the same as sum of the current charging *Cr1* and current discharging *Cr2*. As shown in Fig.3, during the half switching period *Ts*/2, *Cr2* is discharged as much as

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

the load current *io* while *Cr1* is charged. Thus, the average value of the current flowing through *D*1 is the same as twice the load current during *Ts* /2. Due to the symmetric operation, the average value of the current flowing through *D2* is also twice the load current during the next half switching period. Both average values of *vcr1* and *vcr2* are *Vo*/2 and *vcr1*(*t*2) in Eqn. (5) is obtained from the ripple voltage ⩙ *vcr1* of *Cr1* as

$$v_{cr1}(t_2) = \frac{V_o}{2} - \frac{\Delta v_{cr1}}{2} = \frac{V_o}{2} - \frac{1}{2C_{r1}}\int i_{cr1}(\tau)d\tau = \frac{V_o}{2}\left(1 - \frac{T_s}{2C_{r1}R_o}\right) = \frac{V_o}{2}\left(1 - \frac{\pi Q}{2F}\right) \quad (16)$$

Where the frequency ratio *F* and quality factor *Q* are given by

$$f = \frac{f_s}{f_r},\ Q = \frac{4w_r Llk}{R_o} = \frac{4}{w_r C_r R_o} \quad (17)$$

Because the average value of the current flowing through *D1* during *Ts* /2 is the same as 2*io* and is zero during next half switching period, the average value of the current flowing through *D1* during *Ts* is equal to *io*. Thus, the load current *io* can be derived as

$$i_o = \frac{V_o}{R_o} = \frac{1}{T_s}\left[\int_{t_2}^{t_2+\varphi T_s/2} \frac{nV_d - v_{cr1}(t_2)}{Z_r}\sin\omega_r(\tau - t_2)d\tau\right] = F\left[\frac{nV_d - v_{cr1}(t_2)}{2\pi Z_r}(1 - \cos\frac{\pi\varphi}{F})\right]. \quad (18)$$

From Eqns. (16) and (18), the voltage gain in the PSFB series-resonant converter mode can be derived as follows:

$$\frac{V_o}{V_d} = \frac{2n}{\frac{\pi Q}{F(1-\cos\frac{\pi\varphi}{F})} + \left(1 - \frac{\pi Q}{2F}\right)}. \quad (19)$$

Fig. 6 shows the normalized voltage gain in the PSFB series-resonant converter mode. In the active-clamp step-up converter mode, the average voltage *Vc* for *D*> 0.5 is obtained as:

$$V_c = \frac{D}{D-1}V_d \quad (20)$$

By the volt- second balance law for the magnetizing inductance *Lm*, the following equations are derived as

$$nV_d DT_s = \frac{n^2 L_m}{n^2 L_m + L_{lk}} V_{cr2}(1-D)T_s \quad (21)$$

$$\frac{n^2 L_m}{n^2 L_m + L_{lk}} V_{cr1} DT_s = nV_c(1-D)T_s \quad (22)$$

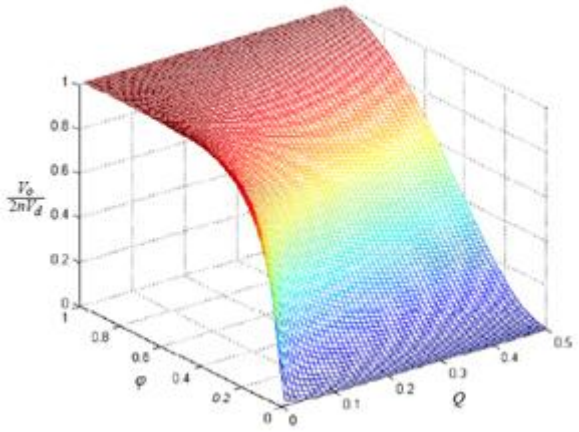

Fig. 6. Normalized voltage gain at F=1.05 in the PSFB series-resonant converter mode.

Where *Vcr1* and *Vcr2* are the average values of the voltages across *Ccr1* and *Ccr2*, respectively. The sum of *Vcr1* and *Vcr2* is *Vo*. From Eqns. (21) and (22), the average values *Vcr1* and *Vcr2* are obtained as

$$V_{cr1} = \frac{n^2 L_m + L_{lk}}{nL_m} V_d = (1-D)V_o \quad (23)$$

$$V_{cr2} = \frac{n^2 L_m + L_{lk}}{nL_m}\frac{D}{1-D}V_d = DV_o. \quad (24)$$

Assuming *Llk* is much smaller than *Lm*, the voltage gain in the active-clamp step-up converter mode can be derived as follows:

$$\frac{V_0}{V_d} = \frac{n}{1-D} \quad (25)$$

The voltage gain becomes that of an isolated boost converter. It means that the proposed converter performs step-up function in the active-clamp step-up converter mode.

In the PSFB series-resonant converter, the leading-leg switches *S1* and *S3* can be easily turned on with zero-voltage by the reflected secondary current. However, when the state of the lagging-leg switches *S2* and *S4*

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

are changed, the secondary current is zero. Thus, only the energy stored in *Lm* is involved in ZVS of the lagging-leg switches condition; it is obtained as

$$\frac{1}{2}L_m(\frac{\Delta i_m}{2})^2 = \frac{1}{2}L_m(\frac{\varphi V_d}{4L_m f_s})^2 > \frac{4}{3}C_m V_d^2 \qquad (26)$$

Where *Cm* is the output capacitance of the MOSFET switches. From Eqn. (26), the magnetizing inductance *L*m can be decided as

$$L_m < \frac{3\varphi_{min}^2}{128 C_m f_s^2} \qquad (27)$$

Where *φmin* is the minimum value of *φ*. The ZCS condition of the lagging-leg switches is related to the frequency ratio. As *F* increases, the ZCS range decreases [15]. Therefore, to guarantee both ZVS of all primary switches and ZCS of the lagging-leg switches, *F* should be selected to be slightly more than one. In the active-clamp step-up converter mode, *S2* and *S3* can achieve ZVS turn-on naturally from the asymmetricalPWM operation.

As shown in Fig.2, in the PSFB series-resonant converter mode, *Llk* performs as the output inductor and all energy stored in *Llk* is delivered to the load until the secondary current is zero. Then, only small magnetizing current flows on the primary side. In the active-clamp step-up converter, the proposed converter is operated by dual asymmetrical PWM control scheme. In the PWM scheme, there is no circulating current [22]. Thus, the proposed converter eliminates the conduction loss by the circulating current in the entire operation range.

IV. IMPLEMENTATION AND EXPERIMENTS

To evaluate a feasibility of the proposed converter, a 1kW prototype was built and tested. The operation range of the proposed converter is from 250V to 350V. The output voltage is designated as 200V and the normal input range is set up from 320V to 350V

A. Implementation of The Prototype

Considering power conversion efficiency under the normal input range, the proposed converter is designed. To obtain ZVS turn- on of the switches, the switching frequency *fs* should be higher than the resonant frequency *fr*. By the design rule proved in [15], the frequency ratio *F* (*fs/fr*) is selected to be slightly more than one. The quality factor *Q* is decided by Eqn. (17). If *Q* is too small, the proposed converter is operated with small *φ* under the normal input range. Thus, *Llk* is selected as 8.3μH. From the normal input range, the turn ratio *n* is decided by Eqn. (19) and Fig. 6.

TABLE I: PARAMETERS OF THE PROTOTYPE

Parameters	Symbols	Value
Input voltage	V_d	250-350V
Output voltage	V_o	200V
Switching frequency	f_s	50kHz
Primary winding turns	N_p	24turns
Secondary winding turns	N_s	8turns
Magnetizing inductance	L_m	695μH
Leakage inductance	L_{lk}	8.3μH
Clamp capacitor	C_c	11μF
Resonant capacitors	C_{r1},C_{r2}	680nF
Output capacitor	C_o	680μF
Switches	S_1, S_2, S_3, S_4	STW26NM60
Blocking diode	D_B	FFAF40U60DN
Output diodes	D_1, D_2	FFPF15U40S

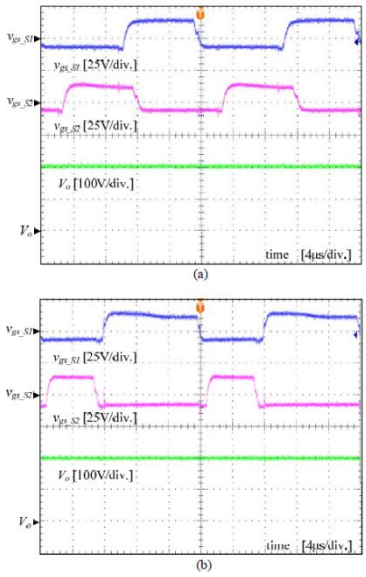

Fig. 7.Experimental waveforms for the gate signals and output voltage according to the operation mode. (a) PSFB series-resonant converter mode when Vd =350V. (b) Active-clamp step-up converter when Vd =250V

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

All switch stresses are determined by the input voltage in the PSFB series-resonant converter mode. On the other hand, in the active-clamp step-up converter mode, the voltage stress of the switches *S1* and *S2* are the same as the input voltage and those of *S*3 and *S*4 are determined by Eqn. (20). In both the operation modes, voltage stresses of the rectifier diodes are clamped at the output voltage *Vo*. The major experimental parameters are presented in Table I. The prototype is implemented using a single DSP chip, dsPIC33EP512GM604 (Microchip) which provides both phase-shift and asymmetrical PWM control.

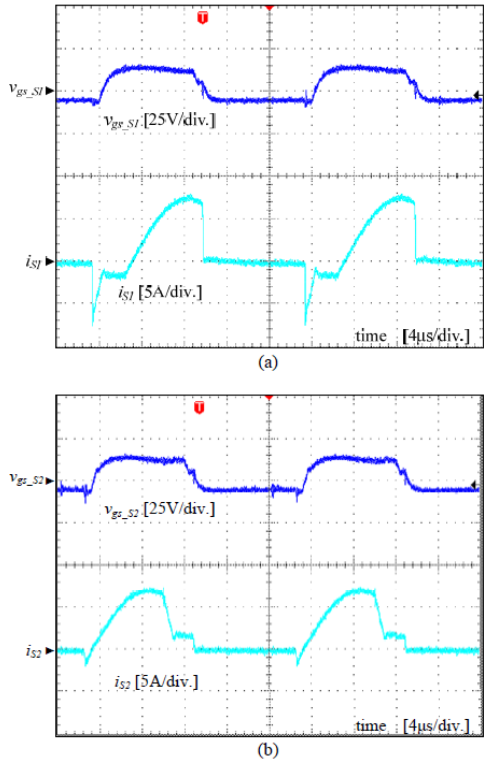

Fig. 8.Experimental waveforms for soft switching in the PSFB series-resonant converter mode. (a) ZVS turn-on of S1. (b) ZVS turn-on and ZCS turn-off of S2.

B. Experimental Results

Fig. 7 indicates waveforms for the door flags and yield voltage in the proposed converter as indicated by the operation mode. vgs_S1 and vgs_S2 are every door signal for S1 and S2, separately. At the point when the information voltage is 350V, the proposed converter is worked by stage shift control with the consistent obligation 0.5. Then again, when the info voltage is 250V, the proposed converter is worked by the unbalanced PWM control with the obligation 0.61. In both operation modes, the proposed converter controls vo. Fig. 8 (an) and (b) show waveforms for the entryway signs and streams of S1 and S2 at full load condition when Vd = 350V. At the point when the switches are turned on, the streams move through the body diode of every switch. Plainly all switches are turned on with zero-voltage. Besides, as appeared in Fig. 8 (b), S2 is killed with close to zero present as the hypothetical investigation. Fig. 9 show waveforms for the essential voltage vp and current ip of the ordinary PSFB arrangement thunderous converter and the proposed converter at full-stack condition under the typical information range. In the routine PSFB arrangement resounding converter, to ensure the assigned operation range, higher turn proportion n (=0.417) is required than the proposed converter. Different parameters are appeared in Table I. At the point when the info voltage Vd is 350V, the routine converter works with littleφ (=0.5).

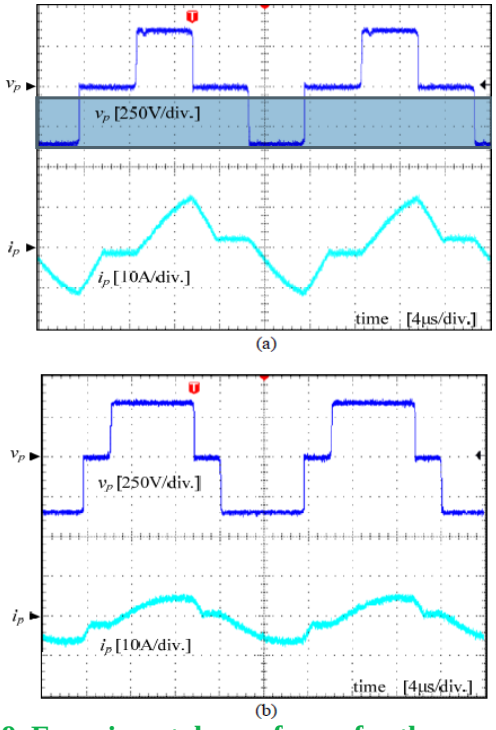

Fig. 9. Experimental waveforms for the current stress when Vd =350V. (a) Conventional PSFB series-resonant converter. (b) Proposed converter.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

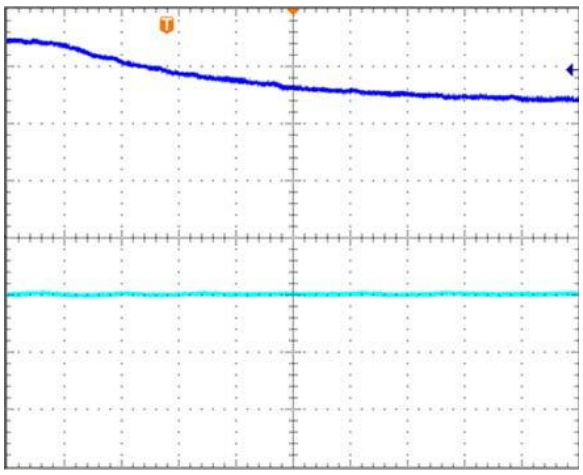

Fig. 10. Experimental waveforms for the input voltage Vd and output voltage Vo in the transition-state.

Then again, the proposed converter is worked with bigger φ (=0.75). As appeared in Fig. 9, the present anxiety in the proposed converter is much lower. What's more, the proposed converter dispenses with the coursing current. Fig. 10 demonstrates waveforms for the information and yield voltages in the transient-state. At the point when the information voltage Vd is decreased from 350V to 250V, the proposed converter manages the yield voltage with no hysteresis. Fig. 11 demonstrates measured efficiencies for the routine arrangement thunderous converter and the proposed converter when Vd =350V. It demonstrates that the proposed converter has higher productivity over all heap conditions. Fig. 12 demonstrates the variety of the yield voltage Vo at full-stack condition when the information voltage Vd diminishes from 250V to 200V.

As appeared in Fig. 12, in the underneath assigned operation scope of the ordinary converter, V o diminishes. In the proposed converter, Vo is kept up as 200V in spite of the fact that the info voltage diminishes underneath the assigned operation range. Fig. 13 demonstrates the similar plot of investigative and trial voltage addition of the proposed converter. At the point when the stage shift esteem φ is communicated utilizing the obligation D, φ/2 can be spoken to as D. The deliberate voltage addition is like the hypothetical examination in Eqns. (19) and (25). As appeared in the Fig. 13, the proposed converter has both the progression down and venture up capacities.

V. CONCLUSION

The novel crossover sort full-connect dc/dc converter with high productivity has been presented and confirmed by the investigation and exploratory results. By utilizing the half and half control plan with the straightforward circuit structure, the proposed converter has both the progression down and venture up capacities, which guarantee to cover the wide information range. Under the ordinary information run, the proposed converter accomplishes high productivity by giving delicate changing method to all the switches and rectifier diodes, and decreasing the present anxiety.

At the point when the information is lower than the ordinary information go, the proposed converter gives the progression up capacity by utilizing the dynamic clip circuit and voltage doubler, which augments the operation range. To affirm the legitimacy of the proposed converter, 1kW model was constructed and tried. Under the ordinary information extend, the transformation effectiveness is more than 96% at full-stack condition, and the information range from 250V to 350V is ensured. Along these lines, the proposed converter has numerous favorable circumstances, for example, high effectiveness and wide information range.

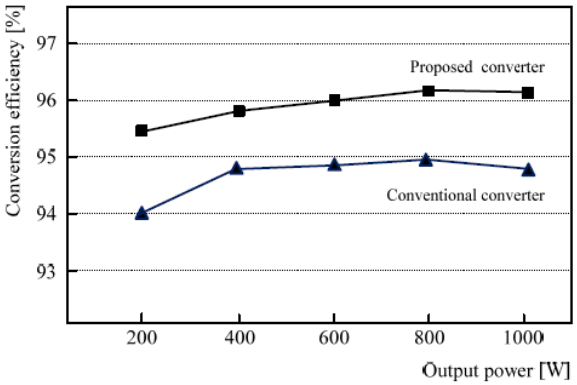

Fig. 11. Measured efficiencies under the normal input range according to the output power

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

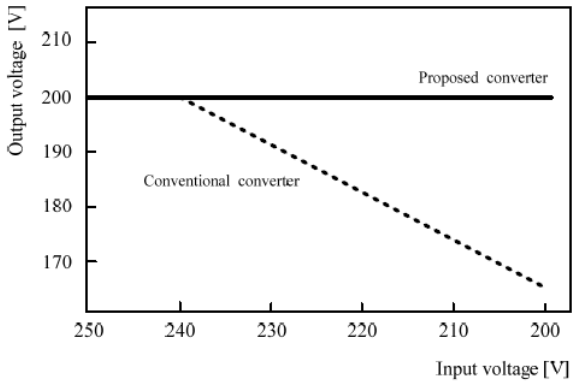

Fig. 12. Variation of output voltage in the below designated operation range

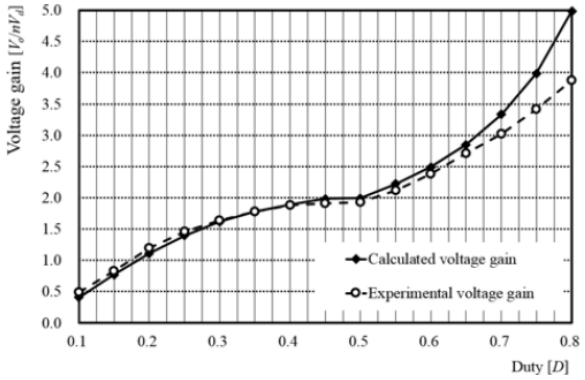

Fig. 13. Comparison between analytical and experimental voltage gain

REFERENCES

1.J. A. sabaté, V.Vlatkovic, R. B. Ridley, F. C. Lee, and B. H. Cho, "Design considerations for high–voltage high-power full-bridge zero-voltage- switching PWM converter," in Proc. Appl. Power Electron. Conf., 1990, pp. 275-284.

2.I. O. Lee and G. W. Moon, "Phase-shifted PWM converter with a wide ZVS range and reduced circulating current," IEEE Trans. PowerElectron., vol. 28, no .2, pp. 908-919.Feb. 2013

3.Y. S. Shin, S. S. Hong, D. J. Kim, D. S. Oh, and S. K. Han, "A new changeable full bridge dc/dc converter for wide input voltage range," in Proc. 8th Int. Conf. Power Electron.-ECCE Asia, May 2011, pp. 2328-2335.

4.P. K. Jain, W., Kang, H. Soin, Y., Xi, "Analysis and design considerations of a load and line independent zero voltage switching full bridge dc/dc converter topology," IEEE Trans. Power Electron., vol. 17, no .5, pp. 649-657.Sep. 2002

5.I. O. Lee and G. W. Moon, "Soft-switching DC/DC converter with a full ZVS range and reduced output filter for high-voltage application," IEEETrans. Power Electron., vol. 28, no .1, pp. 112-122.Jan. 2013

6.G. N. B. Yadav and N. L. Narasamma, "An active soft switched phase-shifted full-bridge dc-dc converter : analysis, modeling, design, and implementation," IEEE Trans. Power Electron., vol. 29 no. 9, pp. 4538-4550, Sep. 2014.

7.Y. Jang, M. M. Jovanović, and Y. –M. Chang, "A new ZVS-PWM full-bridge converter," IEEE Trans. Power Electron., vol. 18 no. 5, pp. 1122-1129, Sep. 2003.

8.T. T. Song and N. Huang, "A novel zero-voltage and zero-current-switching full-bridge PWM converter," IEEE Trans. Power Electron., vol. 20, no. 2, pp. 286-291, Mar. 2005.

9.R. Huang and S. K. Mazumder, "A soft-switching scheme for an isolated dc/dc converter with pulsating dc output for a three-phase high-frequency link PWM converter," IEEE Trans. Power Electron., vol. 24, no. 10, pp. 2276-2288, Oct. 2009.

10.K. W. Seok and B. H. Kwon, "An improved zero-voltage and zero-current-switching full-bridge PWM converter using a simple resonant circuit, " IEEE Trans. Ind. Electron., vol. 48 no. 6, pp. 1205-1209, Dec. 2001.

11.M. Pahlevaninezhad, P. Das, J. Drobnik, P. K. Jain, and A. Bakhshai, "A novel ZVZCS full-bridge dc/dc converter used for electric vehicles," IEEE Trans. Power Electron., vol. 27, no. 6, pp. 2752-2769, Jun. 2012.

12.J. Drobnik, M. Bodor, and M. Pastor, "Soft-switching full-bridge PWM dc-dc converter with controlled output rectifier and secondary energy recovery turn-off snubber," IEEE Trans. Power Electron., vol. 29, no. 8, pp. 4116-4125, Aug. 2014.

13.B., Gu, J.-S. Lai, N. Kees, C. Zheng, "Hybrid-switching full-bridge dc– dc converter with minimal voltage stress of bridge rectifier, reduced circulating losses, and filter requirement for electric vehicle battery chargers," IEEE Trans. Power Electron., vol.28, no.3, pp.1132-1144, Mar. 2013.

14.W. J. Lee, C. E. Kim, G. W. Moon, and S. K. Han, "A new phase-shifted full-bridge converter with voltage-doubler-type rectifier for high-efficiency PDP sustaining power module," IEEE Trans. Ind. Electron., vol. 55 no. 6, pp. 2450-2458, Jun. 2008.

15.E. H. Kim and B. H. Kwon, "Zero-voltage-and zero-current-switching full-bridge converter with secondary resonance," IEEE Trans. Ind. Electron., vol. 57 no. 3, pp. 1017-1025, Mar. 2010.

16.B. Yang, P. Xu, and F. C. Lee, "Range winding for wide input range front end dc/dc converter," in Proc. IEEE Appl. Power Electron. Conf., 2001, pp. 476-479.

17.X. Wang, F. Tian, and I. Batarseh, "High efficiency parallel post regulator for wide range input dc-dc converter," IEEE Trans. PowerElectron., vol. 23, no. 2, pp. 852-858, Mar. 2008.

18.R. Watson, F. C. Lee, and G. C. Hua, "Utilization of an active-clamp circuit to achieve soft switching in flyback converters," IEEE Trans. Power Electron., vol. 11, no. 1, pp. 162-169, Jan. 1996.

19.Q. Li, F. C. Lee, S. Buso, and M. M. Jovanovic, "Large-signal transient analysis of forward converter with active-clamp reset," IEEE Trans. Power Electron., vol. 17, no. 1, pp. 15-24, Jan. 2002.

20.W. Y. Choi, "High-efficiency DC-DC converter with fast dynamic response for low voltage photovoltaic sources," IEEE Trans. PowerElectron., vol. 28, no. 2, pp. 706-716, Feb. 2013.

21.G. Spiazzi, P. Mattavelli, and A. Costabeber, "High step-up ratio flyback converter with active clamp and voltage multiplier," IEEE Trans. PowerElectron., vol. 26, no. 11, pp. 3205-3214, Nov. 2011.

22.P. Imbertson and N. Mohan, "Asymmetrical duty cycle permits zero switching loss in PWM circuits with no conduction loss penalty," IEEETrans. Ind. Appl., vol. 29, no. 1, pp. 121-125, Jan. 1993