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Scan Test Bandwidth Management for System-on-Chip Using FPGA

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Abstract:
With the increase in chip size and complexity, the direct or bus interconnects in conventional SoC testcontrol models are rather restricted. In this paper, we propose a new distributed multihop wireless testcontrol network based on the recent development in "radio-on-chip" technology. The proposed architecture consists of three basic components, the test scheduler, the resource configurators, and the RF nodeswhich support the communication between the test scheduler and clusters of cores. Under the multileveltree structure, the resources (including not only the circuit blocks to perform testing, but also the on-chipradio-frequency nodes for intra-chip communication) are properly distributed and system optimizationis performed in terms of both test application time and test control cost.

Keywords:
Bandwidth management, embedded deterministic test (EDT), scan-based test, test access mechanism (TAM),test application time, test compression, test scheduling.

1. Introduction:

The integration of a complete system, which until recently consisted of multiple ICs on a PCB, onto one chip is termed as System-on-Chip (SoC) that uses embedded reusable cores. As the technology of microprocessor design and manufacture advances, more and more transistors can be placed on a silicon chip. This continuous increase in the design complexity poses a number of challenges to the system integrators while incorporating the test methodologies.

Since cores in an SoC are not directly accessible via chip inputs and outputs, special access mechanisms are required to test them at system level, also known as Test Access Mechanisms (TAMs). It is used to deliver the test stimuli from the test source to cores and also to deliver responses from cores to the sink. The efficiency of a TAM depends on to what extent it can reduce the testing time, that is, time to test all cores in the SoC. Optimized architectures are needed to test the System-on-Chip in a cost-effective manner. Apart from the testing of the cores, the interconnects between them also need to be tested. This essentially means some inputpattern to be applied at the origin of the interconnect and the value be checked at the other end. A number of interconnects can be tested in parallel, if the test resources are available.

Thus, to reduce the total testing time for the chip, it is necessary that we consider the core testing and interconnect testing in an integrated fashion. Another important issue during testing is the test power consumption. Though constrained scheduling to match the power budget has been proposed, another important component of power reduction is that of the scan chains. As a number of cores are put on a particular TAM, their test patterns will pass through the wrappers scan cells. This is particularly true for wrappers designed without any by-pass mechanism. Thus, the order in which the cores are placed on a TAM determines the switching and the associated power consumptions. The integrated wrapper/TAM co-optimization and test scheduling problem that we address in this paper is as follows.

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Determine (i) the number of TAMs for the SoC, (ii) a partition of the total TAM width among this number of TAMs, (iii) an assignment of cores to the TAMs of different widths, (iv) a wrapper design for each core such that the SoC testing time is minimized, and, (v) an order of cores assigned to a TAM bus such that switching activity on the bus during testing is minimized.

II.Literature survey:

This chapter deals with the theory behind the topics analyzed in this thesis. The firstsection of this chapter is a study of two DFT techniques that are widely used. The secondsection discusses why high test application time is a problem worth solving. The third sectionexplains the power considerations during test, which plays an important role in deciding thescan clock frequency.

Design For Testability (DFT) Techniques:

As discussed earlier, as the size of circuits increases, their test complexity also increases. The internal nodes in the circuits become harder to test. Circuits are therefore modified so that they can be tested better. This section describes some of the techniques used to improve the quality of test.

Scan Design:

A combinational circuit with n inputs has 2npossible input combinations. As n increases, the number of possible input vectors increases exponentially. It is therefore impossible to apply all possible input vectors to test the circuit. A subset is therefore chosen such that a sufficient percentage of the faults can be captured by the test. Sequential circuits are harder to test than combinational circuits. This is due to the presence of memory elements (shown in Figure 1) which create internal states during circuit operation. An exhaustive test would involve application of all possible input vectors at all possible states of the memory elements. This number becomes large even for small circuits.

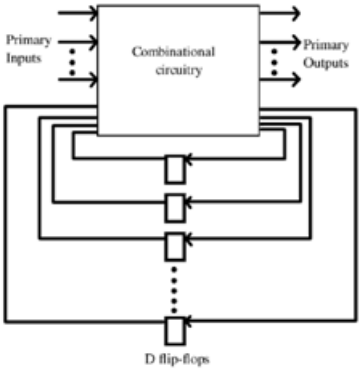

Figure 1: Sequential Circuit

In order to improve the testability of sequential circuits, they are enabled with a testmode. When the circuit is in the test mode, the flip-flops in the circuit are chained together to form one or more shift registers. Thus, the flip-flops can be sent to any state without depending on the values at the primary inputs. The flip-flops serve as points of controllability and observability and help in achieving better test coverages. There are two widely used types of scan designs - full scan and partial scan designs. Full scan designs utilize all flip-flops in the circuit to generate shift registers [11]. Partial scan designs [1] use a selective set of flip-flops to form shift registers. The flip-flops are chosen[18], [13] such that they minimize overhead without loss of coverage.

BIST:

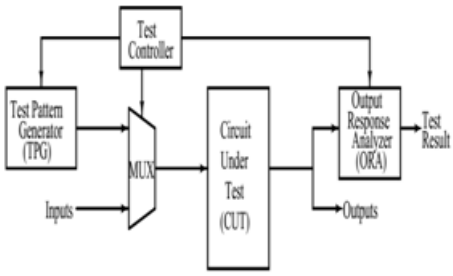

Figure 2: BIST Implementation

BIST is a DFT technique in which additional hardware is added to the circuit to betested so that it can test itself. BIST is widely used since it makes the chip easier and fasterto be tested.

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The basic circuitry required to implement BIST is shown in Figure 2.The patterns required for test are generated through a number of techniques [11]. One of them is to store the test patterns in a ROM on the chip. This method uses a lot of chip area and is hence not very widely used. Counters can be used to generate exhaustive test sequences. However, the number of exhaustive inputs is very high for any normal-sized circuit and hence the test time required is very high. A more commonly used technique is the use of a Linear Feedback Shift Register (LFSR) that generates pseudo-random pattern sets. A large number of test patterns are used in this method but the area overhead on-chipis very low. A large number of outputs are received from the circuit under test. Storing the correct values of all these bits would add a lot of extra hardware to the chip. The circuit responses are therefore reduced to a size that can be stored on the chip. This is done through a number of response compaction methods. A widely used method compacts responses with an LFSR [25]. Some other methods count number of transitions, or use parity information and so on.

III. Proposed System:

Control data delivery:

The approach summarized in Section II does not make any specific provisions for the way control data is delivered to SoC test logic in order to setup test configurations. It appears, however, that the number of test configurations, and hence the amount of control data one needs to employ and transfer between the ATE and DSR address registers, may visibly impact test scheduling and the resultant test time. Consequently, we begin this paper by analyzing three alternative schemes that can be used to upload control bits and show how they determine the final SoC test logic architecture. A. Using IJTAG. The IEEE 1687 is a proposed standard for accessing on-chip test and debug features via the IEEE 1149.1 test access port (TAP). The purpose of this internal Joint Test Action Group (IJTAG) standard is to automate the way one can manage on-chip instruments, and to describe a language for communicating with them via the IEEE 1149.1 test data registers (TDRs).

If there is an IJTAG network available on the SoC, and the total number of test configurations is relatively small, one can use it to deliver the control data, as shown in Fig. 3.The SoC design of Fig. 3 has a single TAP and three different blocks: 1) two cores (C1 and C2) under test and2) the DSR interfacing ATE withC1 and C2. TAP can beinstructed to enable a test path via the IEEE 1687 segment insertion bits (SIBs). Every SIB is used to either enable or disable the inclusion of an instrument into the path from a test data In to a test data output. The TDR in C1 orC2 can be either bypassed or loaded with data putting both cores into specific test modes. The TDR in DSR receives the control data indicating which core and which of its test channels are connected to which ATE channels.

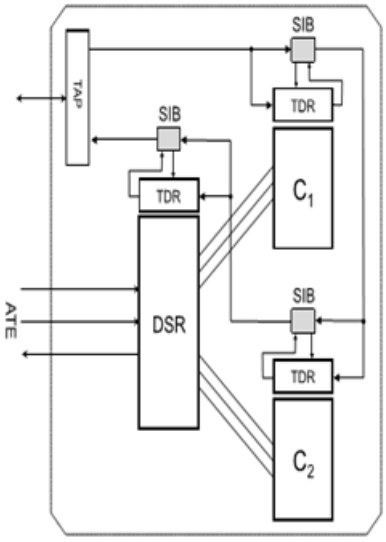

Fig. 3. Using IJTAG network to transfer control data

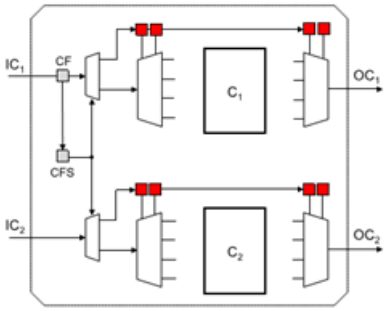

Fig. 4.Dedicated control chain-based architecture.

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The advantage of using the IJTAG network to deliver the DSR control data is a simple and easy way to implement flow as the network is frequently used to set the cores TDRs. However, such an approach can only support a limited number of configurations. This is because the IJTAG shift clock is typically 10 to 20 times slower than the scan shift clock. Delivering a large volume of control data can incur an unacceptable total test time overhead. Consequently, this architecture can be used for a relatively small number of test configurations. If the TDRs work with parallel update registers and many patterns use the same configuration, a low throughput IJTA Gcontrol can be mitigated. If one changes the control state rather seldom, the next configuration vector can be shifted in coincidently with application of test patterns, followed by updating TDR when ready to switch to the new configuration. It requires more DFT logic, though. Test Control Architectures. In this section, we first introduce the basic network components. Then we present three proposed test control architectures.

Network Components:

Three basic components are used in the proposed test control architectures: the test scheduler, the resource configurators and the RF (radio frequency) nodes dispersed on the SoC. The test scheduler is employed as a central controller, it (1) carries out the chip level test procedure, including the testing of the interconnects between the cores, the testing of the user-defined logics around the cores and the core testing, (2) communicates with the resource configurators and also with the chip external, such that no conflict arises during resource utilization and test application, (3) configures the routing of the test control path for each individual core, and (4) provides proper test control signals to carry out the test procedure of the selected core. The function of the resource configurator is to configure the test resources required for testing a particular core on command of the scheduler . A set of test resources (i.e., the circuit blocks required to perform testing) is distributed in the system for testing the cores.

At any particular control step, each resource is configured into its appropriate operating mode by the control signals. In case when more than one tests share common test resources, the resource configurators are activated such that no conflicts result in the use of resources. The RF node is a radio-frequency interface for (two-way) communication between the scheduler and IP cores. Particularly , one RF node is dedicated to the scheduler . The distribution of RF nodes chip-wide provides the coverage of the entire on-chip wireless communication. T o reduce the routing cost and area overhead, one RF node is shared by a cluster of cores which are hard-wired to it. For example, as shown in Figure 1,cores✂✁ , ☎✄ , ✝✆ and ✞✟ are organized into one cluster and are wired to the RF node. In addition, the IP coresin the system are organized into clusters and each has the IEEE P1500 wrapper interface to switch betweendifferent modes according to the control signals received.

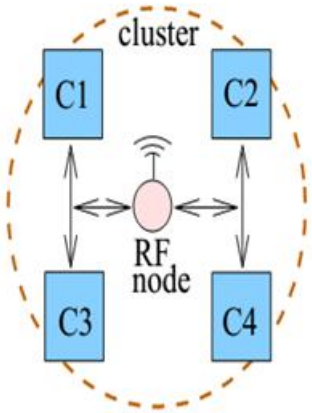

Figure 5:A RF node in a cluster of cores.

Miniature Wireless LAN Based Test Control Network:

Our first proposal is a miniature wireless LAN (local area network) that works as the intra-chip test control network for system-chips, where the scheduler broadcasts control signals through the attached RF node as shown in Figure 2. A single wireless channel is shared by all RF nodes in the chip and the control signals sent from the scheduler will be received by all RF nodes.

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Each RF node has a unique ID and each control signal is attached with an ID field to specify the intended recipient. Upon receiving a signal, a node checks the ID field through its local decoder. If the signal is intended for the receiving node, the node processes the control signal, otherwise, it is just ignored. By specifically assigning the ID (for example, reserving one bit to indicate multicasting while the remaining bits are to hold a group number), we can also support multicasting to a subset of RF nodes and consequently a subset of cores can be tested concurrently. When a core finishes testing, the related RF node needs to notify the scheduler its completion. Since the schedule of the tests is predetermined, each RF node is given exclusive access to the network in a predetermined order. Permission to transmit signals to the scheduler is passed from one RF node to another using a special message called a poll and the polling order is maintained by the scheduler according to the schedule result.

When the scheduler receives the completion signal from the RF node which holds the poll, it then forwards the poll to the next node in the polling sequence. This centralized polling schemeh as its unique features as compared to the conventional polling network, which divides time into alternating types of intervals: polling intervals, during which the poll is transferred between stations, and transmission intervals, during which the station with the poll transmits packets. Our scheme is quite simplified due to the fact that the scheduler knows in advance the completion time of each test and the transmission time is quite short. Thus it's not necessary to maintain the polling and transmission intervals. By using the polling scheme, no collision occurs even when multiple tests finish testing at the same time.

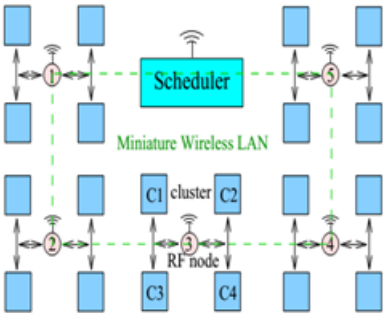

Figure 6: Miniature wireless LAN based architecture

Using Pipelines:

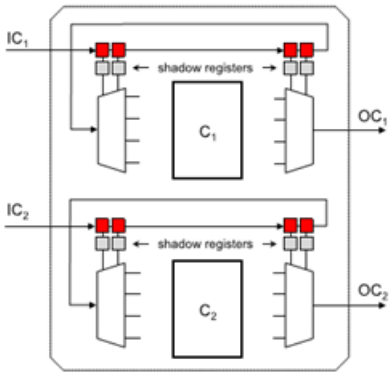

Fig. 7.Pipeline architecture.

One can also use the regular scan channels to deliver controls through pipelining stages, as shown in Fig. 7. For each channel, this approach concatenates+m control bits, where and mare the numbers of control bits used by the Indemultiplexers and output multiplexers, respectively. Moreover, each control bit is shadowed to avoid distorting test configurations in the middle of test data shifting. The shadow registers are updated at the end of each pattern upload. Thus, when a test pattern launches a new test configuration, the corresponding control data need to be loaded with its predecessor. Clearly, the first vector is exclusively a setup one. The architecture of Fig. 7 supports as many test configurations as required. However, the control data is always uploaded through the ATE channels as an integral part of a test vector. Hence, given a test configuration, the same control data is repeated for all test patterns.

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The amount of control data is small, though, as the number of control bits per channelis typically a tiny fraction of the test pattern shift cycles.

Simulation Results:

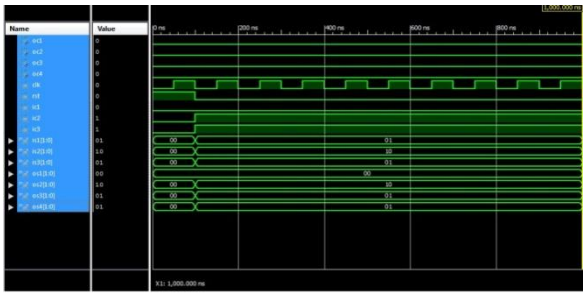

Fig.8: Existed System

Proposed System:

Fig.9: Block Diagram

Synthesis Results:

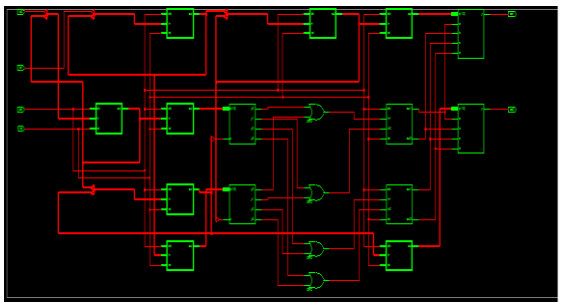

Fig.10: RTL Schematic

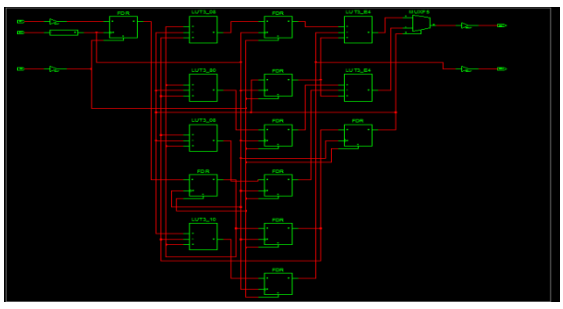

Fig.11: Technology Schematic

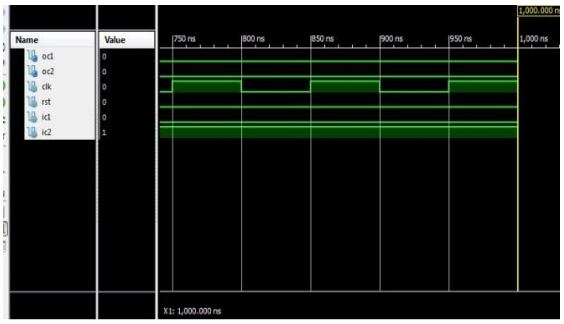

Fig.12: Simulation Result:

Design Summary:

TABLE 1: Design Summary Existed System

watrat Partition Summary
No partition information was found.

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	11	4656	0%
Number of Slice Flip Flops	7	9312	0%
Number of 4 input LUTs	20	9312	0%
Number of bonded IOBs	23	232	9%
Number of GCLKs	1	24	4%

TABLE 2: Design Summary Proposed System:

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	6	4656	0%
Number of Slice Flip Flops	9	9312	0%
Number of 4 input LUTs	6	9312	0%
Number of bonded IOBs	5	232	2%
Number of GCLKs	1	24	4%

Conclusion and Future Work:

In this paper, we have proposed a novel distributed wireless test control network using the “radio-on-chip” technology for future high density, high volume embedded system chips. Three types of control architectures, i.e., miniature WLAN, multihop scheme and distributed multihop scheme have been presented and the system optimization has been performed on control constrained test resource partitioning and distribution. Infuture research, several system

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optimization issues such as RF nodes placement, the optimal number of RF nodes and routing problems will be addressed in detail under the multilevel tree structure. Techniques need to be presented for the integration of test resource distribution and system optimization among T AM design, test scheduling (concurrent core testing as well as interconnect testing) under power and cost constraints. Simulations using randomly generated test sets and experiments with benchmarks will be performed for evaluation and verification of the proposed test optimization algorithms.

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