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Low Voltage and Power Efficient Double Tail Comparator with Reduced Delay Time

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Abstract:
One of the main building blocks in many appli-cations is the analogue-to-digital converter (ADC), which serves as an interface between the analogue world and the digital processing unit. In all these designs, the comparator of the ADC is one the building block. For power efficiency and to decrease the delay, ADC's make use of dynamic regenerative comparators. In this paper, the delay of the dynamic comparators is analysed and expressions are deri-ved. From the analytical expressions, the main fact-ors which are contributed to the comparator delay and tradeoffs in dynamic comparator design are explored. Based on the presented analysis, a new dynamic comparator is proposed, where the circuit of a conventional double tail comparator is modified for low-power and fast operation even in small supply voltages. Without complicating the design and by adding few transistors, the positive feedback during the regeneration is strengthened, which results in remarkably reduced delay time. Post-layout simulation results in a 0.18-µm CMOS techn-ology confirm the analysis results. It is shown that in the proposed dynamic comparator both the power consumption and delay time are significantly reduc-ed in the maximum clock frequency ranges of GHz with 0.8 V power supply.

Index Terms:
Double-tail comparator, dynamic clocked comparator, highspeed analog-to-digital converters (ADCs), low-power analog design.

1.INTRODUCTION:

One of the fundamental building block of most analog-to-digital converters (ADCs) is the COMPARATOR. Many high speed ADC's, such as flash ADC's require high-speed, low power comparators with small chip area. Especially, when we consider the threshold volt-ages of the devices have not been scaled at the same pace as the supply voltages of the modern CMOS processes [1], high speed comparators in ultra deep sub-micrometer (UDSM) CMOS suffer from low supply voltages. So, when the supply voltage is smaller, the task of designing of high speed comparators is a challenge. In other words, larger transistors are required to compensate the reduction of supply voltage at a given technology to achieve high speed. It also means that more die area and power is needed. Low-voltage operation results in limited common-mode input range, which is important in many high speed ADC architectures, such as the flash ADCs.

To meet the low volt-age design challenges, many techniques, such as supply boosting methods [2],[3], techniques employing body-driven transistors[4],[5], current-mode design[6], and those using dual-oxide processes, which can handle higher supply voltages have been developed. Based on augmenting the supply, reference, or clock voltage, Boosting and bootstrapping are two techniques to address input-range and switching problems. These are effective techniques, but they introduce reliability issu-es especially in the technologies of UDSM CMOS. Body driven technique adopted by Blalock[4] removes the threshold voltage requirement so that body driven MOSFET operates as a depletion type device. A 1-bit quantizer for sub-1V modulators is proposed based on this approach[5].

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But, the bodydriven transistor suffers from the smaller transconductance (equal to gmb of the transistor) compared to its gate-driven counterpart. While special fabrication process, such as deep n-well is required to have both nMOS and pMOS transistors operate in the body driven configuration. Developing new circuit structures which avoid stacking too many transistors between the supply rails is preferable for low voltage operation, apart from technological modify-cations, especially if they do not increase the circuit complexity. Additional circuitry[7]-[9] is added to the conventional dynamic comparator to enhance the comp-arator speed in low supply voltages. The proposed comparator works down to a supply voltage of 0.5 V with a maximum clock frequency of 600 MHz and consumes 18 μW. Despite the effectiveness of this approach, the effect of component mismatch in the additional circuitry on the performance of the comp-arator should be considered.

The structure of double tail dynamic comparator[10] first proposed is based on designing a separate input and cross coupled stage. This separation enables fast operation over a wide common mode and supply voltage range. In this paper, a comprehensive analysis about the delay of dynamic comparators has been presented for various archite-ctures. Furthermore, a new dynamic comparator is pres-ented, which does not require boosted voltage or stacking of too many transistors. Merely, by adding a few minimum size transistors to the conventional double tail dynamic comparator, latch delay time is profoundly reduced. This modification also results in considerable power savings when compared to the conventional dynamic comparator and double tail comparator.

2. CLOCKED REGENERATIVE COMPARATORS

Clocked regenerative comparators make fast decisions due to the strong positive feedback in the regenerative latch, so they found wide applications in many high speed ADC's. These comparators are used to investi-gate in different aspects noise [11], offset [12], [13], [14] random decision errors[15], and kickback noise [16]. But in this paper only delay analysis of conv-entional dynamic and conventional double tail comp-arator is analysed and based on that proposed comp-arator is presented.

2.1 Conventional dynamic Comparators:

The schematic diagram of the conventional dynamic comparator is shown in figure 2.1

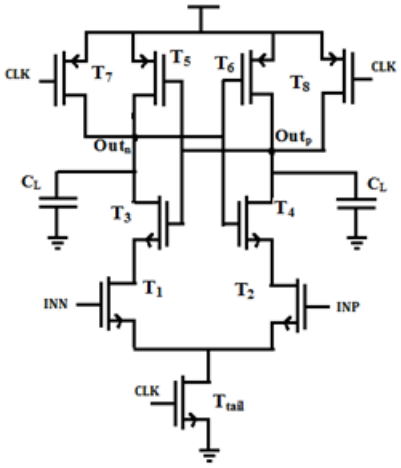

Figure 2.1.1 : Schematic diagram of conventional dynamic Comparator

They are widely used in A/D converters. They have high input impedance, rail-to-rail output swing and no static power consumption. The operation of convention-nal dynamic comparator is as follows:

It has 3 phases of operation, that are reset phase, comparison phase, latch regeneration phase. During the reset phase, when the CLK is low(=0), the tail transistor (T_{tail}) is OFF and reset transistors (T_7 –T_8) pull both output nodes Outn and Outp to V_{DD} to have a valid logical level to define a start condition during the reset phase. In the comparison phase, when CLK=V_{DD}, T_{tail} is on, transistors T_7 and T_8 are OFF. Depending on the applied input voltages at INN and IPP, the Output nodes (Outn and Outp) which had been precharged to $V_{DD,}$ start to discharge. If voltage at INP (V_{INP}) is greater than the voltage at INN (V_{INN}) i.e (V_{INP} > V_{INN}), Outp discharges faster than Outn . when Outp (discharged by drain current of transistor T_2), falls down to V_{DD}-V_{tp} before Outn (discharged by drain current of transistor T_1) and the corresponding pMOS

ISSN No: 2348-4845
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transistor (T_5) will turn on initiating the latch regeneration caused by back-to-back inverters (T_3,T_5 and T_4,T_6). Thus Outp discharges to ground and Outn pulls to V_{DD}. If ($V_{INP} < V_{INN}$), the circuit works vice versa.

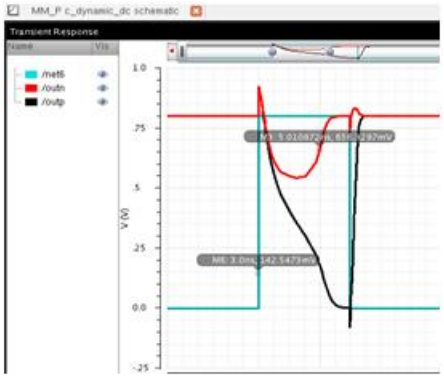

Figure 2.1.2: Transcient simulations of Conventional dynamic Comparator with Δv_{in} = 5mv, V_{cm} = 0.7V, V_{DD} = 0.8V

This comparator has 2 time delays, t_o and t_{latch}. The delay t_0 represents the capacitive charging of the load capacitance C_L (at the latch stage output nodes, Outn and Outp) until the first n-channel transistor (T_9 / T_{10}) turns on.

$$t_o = \frac{C_L|V_{thp}|}{I_2} = 2\frac{C_L|V_{thp}|}{I_{tail}} \quad \ldots\ldots\ldots (1)$$

In (1), since $I_2 = I_{tail}/2 + \Delta I_{in} = I_{tail}/2 + g_{m1,2}\Delta V_{in}$, for sm-all differential input (ΔV_{in}), I_2 can be approximated to be constant and equal to the half of the tail current.

The delay t_{latch} is the latching delay of two cross coupled inverters. Assuming that the voltage swing of $\Delta V_{out} = V_{DD}/2$ has to be obtained from initial voltage difference ΔV_0 at the falling output (Outp or Outn). Half of the supply voltage is considered to be the threshold voltage of the comparator following inverter or SR latch. Hence latch time is given by

$$t_{latch} = \frac{C_L}{g_{m,eff}}.\ln\left(\frac{\Delta V_{out}}{\Delta V_0}\right) \quad \ldots\ldots\ldots (2)$$
$$= \frac{C_L}{g_{m,eff}}.\ln\left(\frac{V_{DD}/2}{\Delta V_0}\right)$$

The total delay of the comparator is approximated as

$$t_{delay} = t_o + t_{latch}$$

$$t_{delay} = 2\frac{C_L|V_{thp}|}{I_{tail}} + \frac{C_L}{g_{m,eff}}.\ln\left(\frac{V_{DD}/2}{\Delta V_0}\right) \ldots\ldots(3)$$

From equation (3) the total delay is directly proportion-al to the comparator load capacitance C_L and inversely proportional to the input difference voltage (ΔV_{in}) and depends indirectly on input common voltage(V_{cm}). By decreasing V_{cm} causes smaller bias current and delay t_0 of the first sensing phase increases. Smaller I_{tail} results in an increased initial voltage difference (ΔV_0) reducing t_{latch} that will finally lead to an increase in the total dela-y. In [17], it has been shown that an input common mo-de voltage of 70% of the supply voltage is optimal regarding speed and yield.

The advantages of this structure is high input impedan-ce , rail-to-rail output swing, no static power consumpt-ion and good robustness against noise and mismatch due to the parasitic capacitances of input transistors do not directly affect switching speed of the output nodes and it is possible to design large input transistors to mi-nimize the offset. On the other hand, the disadvantage is due to the several stacked transistors, a sufficiently high supply voltage is needed for a proper delay time. The other important drawback is that there is only one curr-ent path via tail transistor T_{tail} which defines the current for both the differential amplifier and the latch.

2.2. Conventional Double Tail Dynamic Comparators:

A conventional double tail comparator is as shown in figure 2.2.

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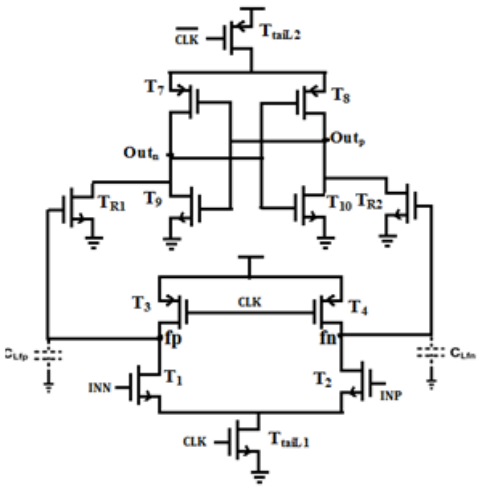

Figure 2.2.1 : Schematic diagram of Conventional double tail dynamic Comparator.

When compared to conventional dynamic comparator, this structure has less stacking so it can operates at lo-wer supply voltages. The double tail enables both a large current in the latching stage and wider T_{tail2}, for fast latching independent of the input common-mode voltage (Vcm), and a small current in the input stage (small T_{tail1}), for low offset.

The operation of this comparator is as follows:
During the reset phase CLK = 0 and $T_{tail1,}$ T_{tail2} are turn-ed off and transistors T_3 - T_4 precharge f_n and f_p nodes to V_{DD}, which causes transistors T_{R1} and T_{R2} to dischar-ge the output nodes to ground. During decision making phase CLK= V_{DD} and $T_{tail1,}$ and T_{tail2} turn on ,T_3 ,T_4 tra-nsistors turns off and at nodes f_n and f_p the previously charged voltage start to discharge. The transistors T_{R1} and T_{R2} passes input dependent differential voltage $\Delta Vf_{n(p)}$ to the cross coupled inverters due to this kick-back noise will going to reduce and good shielding between input and output will be provided.

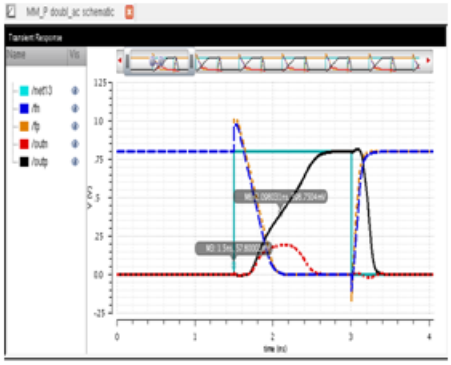

Figure 2.2.2: Transcient simulations of Conventional double tail dynamic Comparator with Δv_{in} = 5mv, V_{cm} = 0.7V, V_{DD} = 0.8V.

For this comparator, the total delay is the sum of t_0 and t_{latch}. The delay t_0 represents the capacitive charging of the load capacitance C_{Lout} until the first n channel trans-istor T_9/T_{10} turns on, after which the latch regeneration starts. So t_0 is

$$t_o = \frac{C_{Lout}|V_{thn}|}{I_{B1}} = 2\frac{C_{Lout}|V_{thn}|}{I_{tail\,2}}$$

Where Ib1 is the drain current of the transistor T_9(if we assume $V_{INP} > V_{INN}$) then Ib1 can be made half of Itail2. When the transistor T_9 of latch is in ON state,the output outn will be discharged to the ground potential which makes T_8 the p-Channel transistor to become ON state and charging the output outp to the voltage V_{DD}. The delay time t_{latch} dependents on ΔVo which is the di-fference between the node voltages at f_n and f_p of seco-nd stage.
Where

$$\Delta V_0 = 2V_{Thn}\frac{\Delta I_{latch}}{I_{tail\,2}} = 2V_{Thn}\frac{g_{TR1,2}\Delta V_{fn/\,fp}}{I_{tail\,2}}$$

Initial output differential voltage ΔVo is influenced by two main parameters transconductance $g_{TR1,2}$ and voltage difference $\Delta V_{fn/fp}$ at output nodes f_n and f_p.

$$t_{delay} = t_o + t_{latch}$$

$$t_{delay} = 2\frac{C_{Lout}|V_{thn}|}{I_{tail\,2}} + \frac{C_{Lout}}{g_{m,eff}}.\ln\left(\frac{V_{DD}/2}{\Delta V_0}\right)$$

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The important points can be concluded from the equations derived for the delay of the double tail comparator:

1. As $\Delta V_{fn/fp}$ increases the delay of the comparator is reduces.
2. In this Comparator the transconductance of interm-ediate transistors will improve only when intermediate stage transistor are cut off mode which makes both f_n and f_p nodes to discharge completely. Again in the reset phase, these nodes have to be charged from ground to supply voltage which leads to consumption of more power.
3. latch will be imbalanced due to the amplification of $\Delta V_{fn/fp}$ by intermediate stage transistors.

2.3 Proposed Comparators:

In low voltage applications, the proposed comparator is designed based on the double tail comparator due to the better performance. The main idea behi-nd the proposed comparator is to increase the diff-erential voltage $\Delta V_{fn/fp}$ inorder to increase the latch regeneration speed. For this purpose, two control transistor $T_{c1}$and T_{c2} are added to the double tail comparator in parallel to T_3/T_4 transisto-rs, but in cross coupled manner. The schematic of prop-osed comparator is as shown in the figure 2.3.

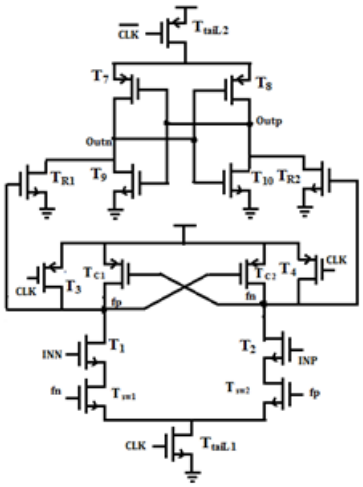

Fig 2.3.1: Schematic diagram of Proposed Comparator

Operation of proposed comparator:

The operation of proposed comparator is as follows:
When CLK=0, T_{tail1} ,T_{tail2} are turned off. This phase called reset phase. During this phase, T_3 and T_4 pulls both f_n and f_p nodes to $V_{DD,}$ hence transistor $T_{c1}$and $T_{c2}$are cut off and intermediate transistors reset both latch outputs to ground. When CLK= V_{DD} and $T_{tail1,}$ and T_{tail2} turn on, called decision making phase. During this phase, transistors T_3 and T_4 are turnoff. At the beginning of this phase, Since f_n and f_p nodes are about V_{DD} , the control transistors are still off. Thus, f_n and f_p nodes start to drop with different rates according to the applied input voltages. If ($V_{INP} > V_{INN}$), then f_n drops faster than f_p because more current is passed through T_2 than T_1.

As far as f_n continues falling, the corresponding pMOS control transistor T_{c1} starts to turn on, pulling f_p node to V_{DD}. So that T_{c2} remains off and allowing f_n to be discharged completely. For conventional dynamic double tail comparator $\Delta V_{fn/fp}$ is just a function of input transistor conductance and input voltage difference. But, in the proposed comparator, as quick as compa-rator detects node f_n discharges faster, a pMOS control transistor T_{c1} turns on puling the f_p node to V_{DD} so that the difference between f_n and fp($\Delta V_{fn/fp}$) increases in exponential manner leading to the reduction of latch regeneration time.

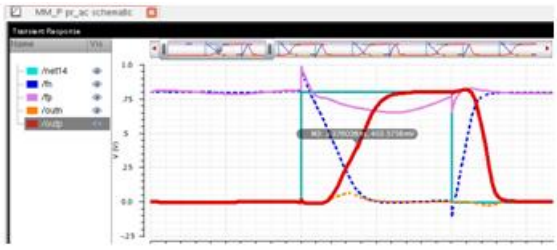

Figure 2.3.2: Transcient simulations of Conventional Comparator with Δv_{in} = 5mv, V_{cm} = 0.7V, V_{DD} = 0.8V

Delay analysis:

The proposed dynamic comparator enhances the speed of conventional dynamic double tail comparator by affecting two important factors:

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i)It increases the initial output voltage difference (ΔV_o). If ΔV_o increases, regeneration time is less.
ii) It enhances the effective transconductance.
By including both effects, the total delay of the propos-ed comparator is achieved from

$$t_{delay} = t_o + t_{latch}$$

$$t_{delay} = 2\frac{V_{Thn}C_{Lout}}{I_{tail2}} + \frac{C_{Lout}}{g_{m,eff} + g_{TR1,2}}.\ln\left(\frac{V_{DD}/2}{\Delta V_O}\right)$$

$$t_{delay} = 2\frac{V_{Thn}C_{Lout}}{I_{tail2}} + \frac{C_{Lout}}{g_{m,eff} + g_{TR1,2}} *$$

$$\ln\left(\frac{V_{DD}/2}{4V_{Thn}\left|V_{Thp}\right|\frac{g_{TR1,2}}{I_{tail2}}\frac{g_{m1,2}.\Delta V_{in}}{I_{tail1}}.\exp\left(\frac{G_{m,eff1}.t_o}{C_{L,fn(p)}}\right)}\right)$$

By comparing the expressions derived for the delay of the three structures, proposed comparator takes advan-tage of an inner positive feedback in double tail opera-tion, which strengthen the whole latch regeneration. Th-is speed improvement is even more obvious in lower supply voltages. This is due to the fact that for larger values of V_{th} /V_{DD}, the transconductance of the transis-tors decreases, thus the existence of an inner positive fe-edback in the architecture of the first stage will lead to the improved performance of the comparator. Simulati-on results confirm this matter.
iii) Reducing the energy per conversion:
It is not only the delay parameter which is improved, but the energy per conversion is reduced as well in the proposed comparator.

3. Comparison of Results:

Structure	Conventional Dynamic Comparator	Conventional Double tail Comparator	Proposed Comparator
Technology	180 nm	180nm	180nm
Power Supply	0.8 V	0.8 V	0.8 V
Delay	900ps	373ps	286ps
Area	16 µ × 16 µ	28 µ × 12 µ	28 µ × 14 µ

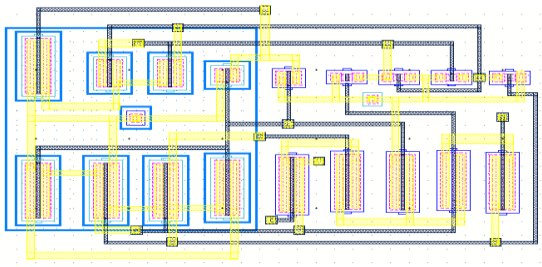

Figure 3: Layout of proposed comparator

4. Flash Type ADC:

In the real world, the signals are analog in nature. If we want to get digital signal, analog signal must be convert to digital form by using Analog –to- digital converter and if we need the analog signal back, digital-to-analog converter is used. There are many ADC architectures which are implemented oriented on power, size and speed. The first architecture is pipeline ADC operating in medium resolution and high speed but below flash type ADC. The second one is SAR type ADC which is operating in moderate speed and medium to high resolution applications. The third one is sigma delta ADC which is for high resolution and low speed applications.

The fourth is Flash type ADC which is for high speed and low resolution applications. Flash ADC is the fastest ADC in comparison with other ADC architectures. Flash ADC is the best type in applications of high speed low resolution applications. It is highly used in high da, high speed instrumentation, date rate links, radar, and optical communications and digital oscilloscopes. The maximum operating frequency in the range of gigahertz because flash ADC is operating in parallel conversion method. Here we use the proposed comparator to reduce the delay and power of ADC.

4.1 Flash Architecture:

The fastest ADC is the flash type ADC because its conversion speed is only one clock cycle. Flash type ADC is based on the principle of comparing analog voltage with a set of reference voltages. To convert the analog input voltage into a digital signal of n-bit output,(2n-1) comparators are required.

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The block diagram of 2-bit flash type ADC is as shown in figure:

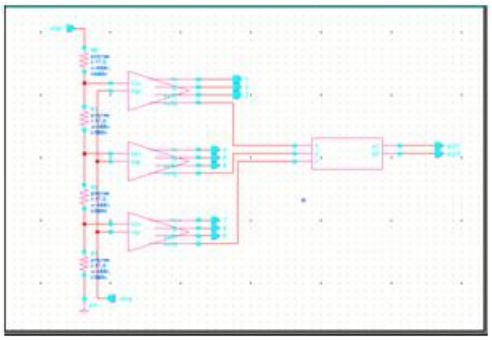

Figure 4.1.1 : Block diagram of Flash type ADC

It consists of 3 comparators and encoder block is shown in the figure

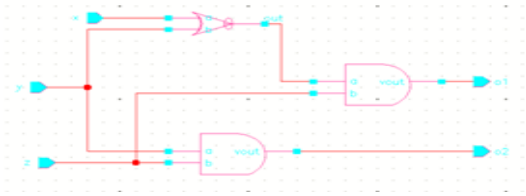

Figure 4.1.2 : Encoder block

The encoder block consists of one xnor gate and two and gates.

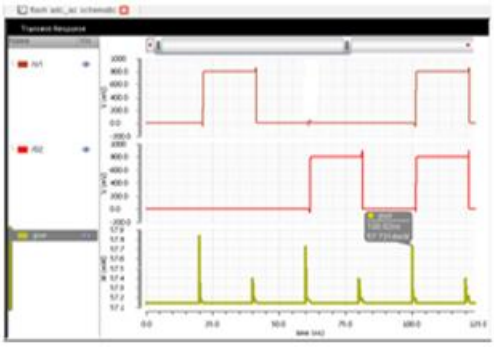

Figure 4.1.3 : Simulation result of 2 bit flash type ADC with PWR

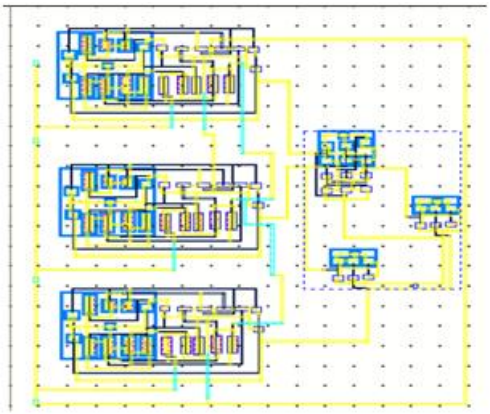

Figure 4.1.4 : Layout of Flash type ADC

Conclusion:

In this paper, a comprehensive delay analysis of two structures conventional dynamic and conventional double tail comparator were analyzed. In order to improve the performance of the comparator the new dynamic comparator with low voltage and low power capability is proposed. Post layout simulation in 180nm technology confirmed that the delay is reduced for the proposed comparator compared to the conventional dynamic and conventional double tail dynamic comparator. It is applied to 2 bit flash type ADC and its delay and power is greatly reduced.

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ISSN No: 2348-4845
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