ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

An Improved Tolerant Permanent Faults in FIFO Buffers of NOC Routers Using Bench Mark Circuits

Rachapudi Deevan Kumar
VLSI & ES,
Department of ECE,
Pace institute of Technology and Sciences,
NH-5, Near Valluramma Temple,
Ongole, Prakasam District, A. P.

Kasula Suresh Babu
Assistant Professor,
Department of ECE,
Pace institute of Technology and Sciences,
NH-5, Near Valluramma Temple,
Ongole, Prakasam District, A. P.

Abstract:
This router buffers during the operation in the field of short-encrypted hard faults NOC first in first out transparent testing technology in the development of the proposed on-line for this identity of faults. A model of the proposed algorithm to run the test periodically to prevent the accumulation of repetitive tests, the router technique involves be integrated into the channel interface and on-line testing has been performed with data traffic, such as synthetic self. The area has been studied by the hardware overhead synthesizing the test the performance of the test section of the circuit combines the NOC terms of investigated throughput. In addition, routing logic an on-line test technology for the transportation of samples to test, using the title proposed flits the data traffic movement.

Index Terms:
FIFO buffers, in-field tests No permanent fault transparent test.

INTRODUCTION:

Over the past decade, the network-on-chip (NOC), overcoming bandwidth difficulties related complex chip designs, compared with bus-based communication network, better communication infrastructure emerged, signal integrity and power dissipation [1] are like all the others, however, systems-on-a-chip (SoCs), NOC-based SoCs must tests were also defective. Testing of the components will be routers and FIFO buffers NoCinfra structure and routing logic, which is occupied by the NOC of the area occupied by the data transport medium is routers links. Significant the interrouter. Accordingly, the run-time errors or logic buffers and the likelihood of errors occurring are high compared to other parts of the NOC. Therefore, NOC infrastructure and routers routing logic testing process should start with the examination of the buffers. In addition, no error is deeply scaled CMOS-based memory test during the test accumulated. They are one of the major concerns of the occasional run-time functional faults must be performed periodically to ensure that it gets. And environmental susceptibility of these errors, the physical effects of aging, and low supply voltage, as a result, and hence are parts of the (nonpermanent device loss or malfunction indicating) in nature [2]. However, these intermittent faults generally exhibit relatively high occurrence rate and eventually become permanent [2].

Two samples can be tested based on the application of the test described in [1] - [3]. Switched to the test under the condition of non-functional operation, delays related to the detection of faults. One of the reasons for this is the following non-functional operation. When the state arbitrarily scan-state, the state transitions to a two-sample test, the circuit may not be functional at the time of the operation. As a result, the functional sensitivity of the operation is not possible at the time to slow down, [1] may result in failure of the circuit. In addition, the functional operation of the circuit to reduce the current demand is greater than the possible voltage drops that can cause it to fail, [2] [3]. In both cases, the circuit will operate correctly during functional operation.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Broadside functional tests [4] Scan-functional operation of the circuit, or in a position to enter the time to ensure that the state is a reachable. Broadside tests [5], the functional mode circuit for two clock cycles are carried out after an initial state of the scan. The use of this two-sample test results. Scan from the state is a reachable state, two-sample test at the time of the functional operation of the circuit will be guaranteed by the state transitions. Delay faults detected by the test can also affect the functional operation, and the current demand is likely to exceed that at the time of the functional operation. Reduces the tendency of the test described in [1] - [3]. In addition, tests are fast broadside functional clock cycles during a power dissipation during operation does not exceed that chance. Functional and pseudo-functional scan-based test generation for testing procedures are described in [4], [6] - [13]. The test procedures are applied to the offline product sets from the external tester. Scan-in and scan-based tests of functional states use only reachable states. Pseudo-functional scan-based tests to avoid the obstacles to reach the use of functional barriers.

The work on a chip (or built) generation of functional tests planned broadside. Reduce test data volume and speed the creation of on-chip test facilities to test the application. Methods of test for errors, such as on-chip delay [14] and [15] states described in them can be used to scan the states do not impose any obstacles. The experimental results can be used as a scan-state to an arbitrary state is a reachable [4] indicate that the state is unlikely to be. Production from the on-chip testing method [16] applies to the pseudo-functional scan-based tests. Such tests are not enough for scan-in states, avoiding unreachable states. This work is described in the on-chip test generation process guarantees will be used only reachable states. It is possible to delay fault coverage that can be achieved by using functional tests using a broadside to broadside the tests less than an arbitrary, in general, it should be noted that [14], [15] or [16] broadside tested in duplicate applications. [16] - this is due to a broadside functional tests [14] are allowed to be reached by the methods described is the fact that to avoid instates scan. However, these tests are necessary in order to achieve high fault coverage are the ones to be switched to the test. They can also dissipate more power than is possible during functional operation. Broadside only functional tests are considered in this work. The proposed on-chip test generation process, while applying the test circuit used for the production of reachable states. This is one of the leading states in offline mode or functional barriers need to count alleviates [4], [6] - [13] and [16]. The underlying research for off-line test generation, [4] as a means of Dharma, this is the following. A is a reachable state from an initial functional mode input range, if the opening is applied, across the bottom of all the states reachable states. Any of these states, the initial state for the use of the test can be used as a functional broadside. F | Needs to be gained in different states. Typically, this number is only a small part of the circuit, all reachable in many states. Therefore, the primary input sequence A state of all its reachable through the circuit does not need to take, but by the relative of a sufficiently large number of | F | In order to effectively target the detection of faults.

The hardware used in this paper is the basic input for the production of a sequence of linear feedback shift register (LFSR) on a random basis [17], and a small number of gates (almost every one of the six gates of the benchmark circuits that need to be considered). Repeat the sequence of gates gained the same or similar in order to avoid cases where states take to the circuit to be used for random order. The repeated synchronization [18] referred to as. In addition, on-chip test circuit is applied to the generation of the hardware is based on the tests used to determine a single gate. As a result, it is compatible with the following parameters given by the circuit is a simple and fixed hardware architecture is.

1) LFSR number of bits.
2) The length of the primary input sequence.
3) Changing the order of the specific gates used for the LFSR sequence.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

4) Based on a specific gate circuit is applied to the functional tests used for selecting a broadside.
5) Of the basic input sequences and many sub-tests in order to produce seeds for the LFSR.

One of the most important advantages of the built-in test generation, that is, without the need for an external source to deliver the tests, it tests the speed at which the faults will delay the application process [1] to locate the facilities [2], [3], [4], [5] [6] [7], [8]. Built-in test preparation, test data volume by a [9] reduces the need for circuit. Methods of test for low-power built-in power dissipation during test application functional operation [10] At the time of the power dissipation from beyond the possible, keep the [11] [12] [13] need to be able to solve. Power dissipation, as well as the delay in the examination of the faults to solve, in [14] described the production of functional test generation method is called a broadside in the tests. In general, where a functional broadside test delay faults detected during the functional operation of its functional clock cycles creates a broadside test conditions. Functional operation conditions at the time of the test, a functional clock cycles may occur during the operation, it seems that the transitions are also functional.

Under the assumption that the primary input sequences that are functional barriers during the operation, a functional test of a broadside scan-state is a reachable state, or is in a position to enter the circuit only requires functional operation. To simplify the discussion, this paper makes the same assumption. Unless the primary input constraints of the experimental results to create a high level of redundancy, that is, constrained and functional barriers to switching activity between broadside tests indicate that the differences are moderate. This paper considers the case of the design-under-test is divided into logic blocks, and there is a built-in option in relation to the placement of the blocks for the test generation logic [9]. Fig. 1 four logic blocks B0 B1, B2, B3, shows a design. Horizontal lines stand for the scan chains, and vertical lines stand for the primary inputs.

[14] from the built-in test production method, and only the values of the scan chains for the production of basic inputs. Scan chains circuit brings a reachable state, and the output is used in the beginning of the responses to the notice. After the start, the basic input sequences generated by the built-in test generation logic circuit will be gained through the States. Some of these states broadside functional tests can be used for the early states.

LITERATURE SURVEY:
BLOCK DIAGRAM OF LFSR RESEEDING SCHEME

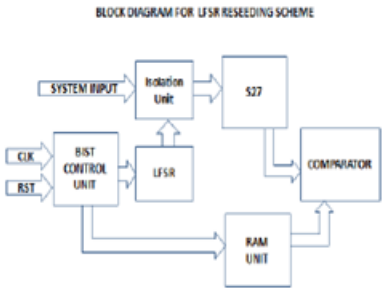

Fig: Simple BIST circuitry.

The linear feedback shift register (LSFR) whose input bit is a linear function of its previous state is a shift register. XOR is the only linear function of the bits, the bits of the input bit of a flap in the value of the shift register exclusive or (XOR) is driven by a shift register. The initial value of the LFSR is called the seed and deterministic operation register, enter the values produced by the flow of the current (or previous) will be determined by the state. Seed is used to generate the test sample and the test cube. LFSR length, r, where smax maximum number of bits specified in a test cube is at least smax +20. R- bit LFSR seed is initialized to the initial r- bit. The initial seed for the scan chains to fill the meter clock cycles LFSR (m scan length) by running the first test is used to create the cube.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

BROADSIDE TESTS IN PARTIAL-SCAN CIRCUITS:

A complete scan of the circuit, denoted by a broadside test referred to by the two primary input vectors and then starts by scanning a position to apply the functional mode. The final agreement by the end of the test is scanned out. The test can be divided into two models only work for one clock cycle, and the second functional clock cycle, apply, apply. Transitions will be under the clock signal in the circuit to settle to allow the application to slow down. Under the high-speed clock will be delayed in order to capture the signal-application transitions. In response to the faults of the initial and final state of the output vector that are detected by the scan. Circuit is a full scan, the scan-mentioned state of the state entirely. After scanning all of the state variables can be assigned to the known values of the circuit. In addition, at the end of the test all the values of the state variables can be observed during the scan-out operation.

For example, we suppose, is denoted by and are the two primary inputs are scanned and the scan an and un-five of the state variables, a circuit considered. A possible scan-in state x is a random (unknown) value today 000xx, is. A broadside test for this circuit, as well as to be partially specified state. For example, and we want to get 1x01x. We are two sample test000xx 00, 1x01x 11 Let's gain. Partially- mentioned models, some errors may not be activated. In addition, the effects of the second sample at the end of the campaign, or test the faults detected by the scan-out operation. Therefore, it is necessary to consider more than two tests of a broadside in the direction of the primary input. After the basic input vectors are applied to the functional mode. Nasal circuit such transitions in the signal-to settle down to allow the clock to be ongoing. Free circuit acts like a slow clock circuit fault.

PESUDO RANDOM TEST GENERATION:

There are three primary objectives:

(A) Random number generators and cryptographic pseudorandom number generators built using mud, but the randomness of the binary sequence to detect the development of a battery of statistical tests,
(B) The implementation of a software product documentation and the tests, and
(C) And to provide practical guidance on the application of these tests. Pseudorandom- appear to be random, but in fact the commitment (repeated) .Linear Feedback Shift Register (LFSR) weighted pseudo-random test generation, the models in the positive pseudo-random test generation

Algorithmic Test Generation:

Here are the basic inputs for controlling the location of a fault to be found in the list. Such an error can activate and sensitize the fault outputs are determined by the initial conditions determine the primary input.

Linear Feedback Shift Registers (LFSRs):

Efficient design for Test Pattern Generators & Output Response Analyzers (also used in CRC) FFs plus a few XOR gates better than counter

- Fewer gates
- Higher clock frequency
- Two types of LFSRs External Feedback, Internal Feedback
- Higher clock frequency

An LFSR generates periodic sequence must start in a non-zero state, The maximum length of an LFSR sequence is 2n -1 does not generate all 0s pattern (gets stuck in that state)The characteristic polynomial of an LFSR generating maximum length sequence is a primitive polynomial A maximum-length sequence is pseudo-random: number of 1s =number of 0s + 1 same number of runs of consecutive 0s and 1s 1/2 of the runs have length1 1/4 of the runs have length 2 (as long as fractions result in integral numbers of runs).

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

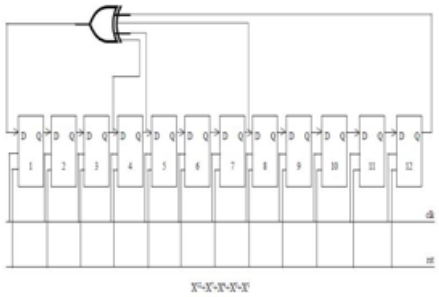

Figure 1.5 LFSR 12bit circuit

OUTPUT OF LFSR

u	LFSR(u)
0	101 011 100 100
1	010 101 110 010
2	001 010 111 001
3	100 101 011 100
4	010 010 101 110
5	001 001 010 111
6	100 100 101 011
7	110 010 010 101
8	111 001 001 010
9	011 100 100 101
10	101 110 010 010
11	010 111 001 010
12	001 011 100 101
13	100 101 110 010
14	010 010 111 001
15	101 001 011 100

RELATED WORK:

As was the fault tolerance, the importance of the research community in the NOC design, failure mechanisms, such as the number of pages, error modelling, diagnosis, and so on have been covered various aspects of fault tolerance. A comprehensive study of the documents summarizing the research work in [3] presented. Over the years, researchers NOC infrastructure for testing Design For-testability (DFT) as the number of processes (testing routers that interconnect as well as NOC) has been proposed [7] and is based on the NOC major test [8]. Built-in self-test (BIST) based methods, and [8] are used for interconnect testing routers, as well as the NOC. [9] In particular, the employment of NOC interconnects and DFT methods for testing routers and router test essence NOC recent paper. In addition to the novel test formats, fault-tolerant routing algorithms has been proposed [10]. NOC infrastructure and the large number of FIFO buffers expanded chip. Accordingly, the probability of faults router both online and offline testing methods have been proposed in other parts of the test, compared with the NOC FIFO buffers buffers is signifihigher. [11] FIFO buffers in the proposal proposes a shared BIST controller is an examination technique (preparation of the FIFO buffers suitable for fault detection) is. NOC routers to identify faults in the FIFO buffers online test methods [12] proposed. However, SRAM based FIFO cuddammarket models as a standard cell-based FIFO buffers planned. Therefore, this briefly considered faults [12] are different from those targeted. Best of our knowledge, no work within the NOC infrastructure, routers, SRAM based FIFO buffers are currently offered to the online test is reported in the literature. Thus, we usually test methods SRAM-based FIFOs online survey. The survey is based on SRAM FIFOs, to be tested by either of the following two approaches as proposed by BIST dedicated to a policy of Barbagallo said. [13] and the proposed distribution of or BistGrecu. [11]. However, the distribution of both dedicated and permanent faults, which can develop over time BIST offline testing methods fail to detect the presence of procedures.

PROPOSED TRANSPARENT TEST GENERATION:

If SRAMS or apply for drams, this briefly considered faults, can be determined using standard tests in March [6]. However, if the faults are considered for the same set of FIFOs SRAM- type, due to the March test [14] was kind of SRAM- FIFOs cannot be used to limit the address and so we were motivated to choose a single order address mats ++, test (SOA- mats ++,) [14] to

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

find this briefly considered faults. Wordoriented SOA-mats ++, test {(w) referred to; ↑ (RA, WB); ↓ (RB, W)}; (RA)} is a data background, b, where the data is to fill in the background. ↑ and ↓ addressing the growing decrease in the order of the memory. Means of addressing memory can increase or decrease. SOA-to FIFO memory into the use of mats ++, writing samples, and has been read back to them. As a result, the memory contents are destroyed. However, after examination of the online memory test methods necessary to the recovery of memory. Therefore, the researchers transparent Mar Test [15] and in March revised screening tests can be performed without the need for external data in the background, so that the memory contents can be restored after the test. FIFO buffers that way we can apply for online testing SOA-transparent mats ++ (TSOA- mats ++) test SOA- mats ++, have been transformed by the test. The test product is represented as transparent SOA- mats ++, {↑ (R X, wx, R X, wx upon, R X)}. The test operations performed at the time of the test, namely, the inverse phase, phase to restore the representation of three stages, and read phase. The first two set up a pair of read-write operations (RX, wx) the initial content test (lute) under the FIFO buffer locations (before the start of the test content) invert the phase where the representation is read and written back to the same location as its complement. After the restore operation in the phase inversion stage (RX, wx), the lute are reinverted to read the content. The test this time, the contents of the lute was flipped twice to get back to the original content. The final step, (RX) follow the lute without any write operation will be reading the content.

A. Test Algorithm:

Transparent mats SOA- ++, test interpretation algorithm is an algorithm is presented that FIFO memory 1. Transparent individual place mats SOA-++, step by step approach to perform the test in three stages. Acantly the number of FIFO memory locations where n 1, - testing the target location for the loop index i varies from 0 to N is given by.

Algorithm 1 Transparent SOA-MATS++ Test Algorithm

```
Require: N = number of rows of the FIFO memory
1: i ← 0;                          /* memory address pointer */
2: while (i ≤ N − 1) do
3:   j ← 0;                        /* test cycle counter */
4:   while (j ≤ 2) do
5:     temp ← read(i);
6:     if (j = 0) then
7:       original ← temp;
8:       write(i, !temp);
9:     else
10:      if (j = 1) then
11:        result ← compare(temp, original);
12:        write(i, !temp);
13:      end if
14:    else
15:      result ← compare(temp, original);
16:    end if
17:    j ← j + 1;
18:  end while
19:  i ← i + 1;
20: end while
```

In other words, I am referring to the address of the FIFO memory test for each of the three test runs under the hotel (i of the current value), the loop index to a specific FIFO memory location j for performed during three iterations, J. (address run1) of the first iteration of the FIFO invert the phase of either the location of the content, it will run. Invert the testing phase, backing up the original, it is a temporary variable, and then read the content of the temporary lute. Then, the inverse of a temporary rewrite the content lute. At this time, lute content original.In content inverted J (address run2) is the next iteration of, is carried out to restore the stage. Temporary lute content is read and compared to the original content. 1 must be the result of the comparison sample. However, the deviation from the pattern of 1 in a bit position indicates that the specific bit in the wrong place. Next, the inverse of a temporary rewrite the content lute. In this way, after the first iteration, the inverse of the lute content, will be restored after the second. The third iteration of j read the original elements of the temporary content compared lute lute, which will run only the read operation. At this stage of the test, as a result of the order of 0 to any bit pattern in place of the deviation of 0 means that a particular bit in the wrong place, the wrong refers to the free area.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Which remained undetected during two test runs before the read operation ensures the detection of faults. Three test runs (j again) at the end of the loop index i is incremented by one to mark the beginning of testing to the next location.

B. Fault Coverage of the Proposed Algorithm:

Transparent mats SOA- ++, intended for testing of the algorithm is difficult at fault, conversion disorder, and FIFO memories of the field at the time of the operation is to disrupt the development of the wrong tests. Fault coverage of the algorithm shown in Fig. 1. The two figures, the size of the word FIFO memory is assumed to be 4 bits. However, in accordance with the variables used in the algorithm 1 bold font text italic text against arrows, indicating the operation is performed. As shown in Fig. 1, 1010. The test cycles assume that the data word lute now invert the phase (0 value of the memory address pointer j) is read from the temporary location of the content to be addressed and then backed up at the time of the original will begin. SOA- mats ++, test data is written back. Lute is to fill the temporary content. Therefore, at the end of the cycle, the temporary current and 1010 actual data, lute 0101.Assume the most significant bit (MSB) in place of the word lute store is having a stuck-at-1 fault. Therefore, instead of the 0101, 1101, store, and as a result of the fact that shops, stuck-at-fault gets excited at MSB.

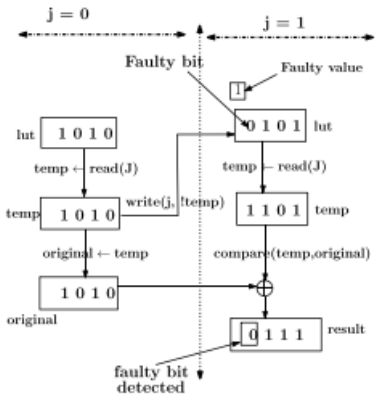

Fig. 1. Fault detection during invert phase and restore phase of the transparent

IMPLEMENTATION OF THE TEST ON FIFO BUFFERS OF NOC ROUTERS:

In this section, we proposed a mesh-type transparent NOC ++, testing SOA- mats used for implementing the present technique. Data packets flow control units (flits) and the pipeline is divided into fashion, [1] are transmitted. NOC infrastructure is considered to be the work of the mesh routers flit movement is considered to be in need of buffering input channels. Thus, the data from another core for the movement of traffic, online testing is the only way to lie input channel FIFO buffers, performed. Buffers two modes, normal mode and test mode to operate. A FIFO buffer operation mode and test mode will be synchronized with two different clocks. The purpose of the test (also known as the short test_clk) The clock is used in normal mode (Router Clock) to the clock is faster than the clock.

FIFO buffers before the time of their examination process, \ sufficient amount allowed for the normal operative mode. FIFO buffers to be transformed into a permanent faults, the delay in the initiation of the test development, run-time to provide enough time for intermittent faults. The process of testing a targeted FIFO buffer FIFO buffer normal mode and test mode switches to a counter, initiated by. FIFO buffer FIFO buffers, switching from test mode to normal mode, without caring about the current status occurs after a certain period of time.

It may be argued that the switching point, the buffer may not be complete, and the result of the test cycle for all locations are tested. However, following the initiation of the test problems later in the buffer gets full. First, to complete the necessary test may be able to delay the initiation of the process to wait for the buffer and allows you to get the accumulated faults.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

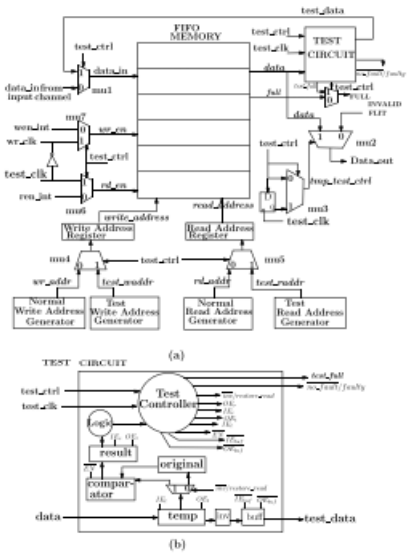

Fig. 2. (a) Hardware implementation of the test process for the FIFO buffers. (b) Implementation of test circuit.

Second, the buffer can be useful to prolong the time of the test and the test adversely affects the normal mode of operation. Burst test, a test series, read, write cycles. Read and write cycles of three to two, or three clock cycles, in other words, a FIFO buffer for faster testing SOA- transparent mats ++, perform the test in one location. It is time for a test burst, the FIFO buffer locations would be tested, or the position of the test may be interrupted. Both of these problems can be avoided by periodically testing FIFO buffers. Periodic testing of a FIFO buffer FIFO buffer for each test material to test a different set of bases. Every time there is a buffer test mode, the normal process gets interrupted. FIFO memory is being addressed in the normal manner in the context of switching, the test will be the location of the target. Leopard different instants of normal operation, the test is interrupted, so that there will be a variety of positions for each material tested. Therefore, in a FIFO buffer is a FIFO buffer, repeating several times the number of test explosions, as the small number of people in each location is covered by the test.

Moreover, the error accumulation buffer to prevent periodic examination

EXPERIMENTAL RESULTS:

A prototype implementation of the proposed test circuit has been integrated into the router-channel interface and online transparent SOA-MATS++ test is performed with synthetic self-similar data traffic. The router design considered in this brief has been taken from [16].

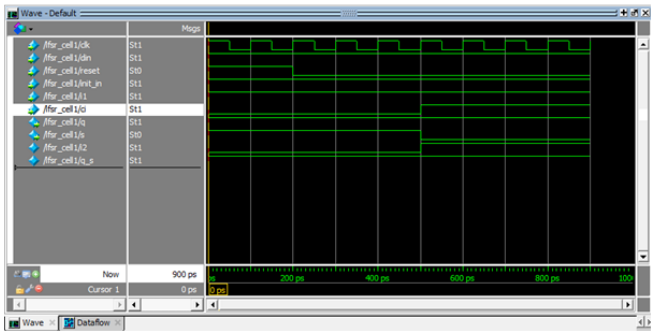

Fig: LFSR cell design

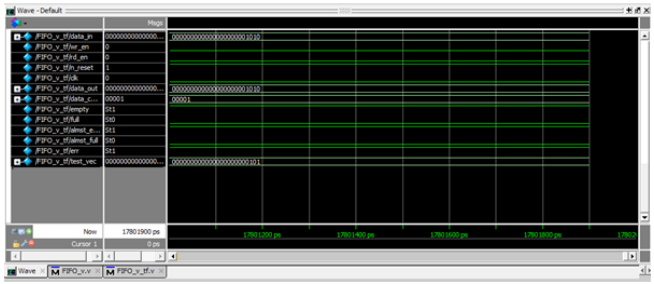

Fig: Waveform for FIFO without fault

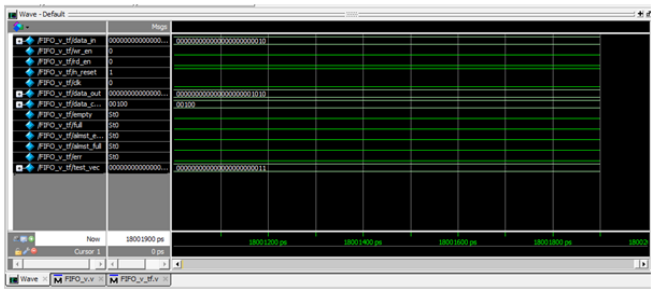

Fig: waveform for FIFO with faults

PROPOSAL FOR TEST OF ROUTING LOGIC:

The other part of the router, buffers, along with the possibility of permanent faults in the run-time routing logic.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

In this section, we will use for the test data packets and routing logic, thus overcoming the need for test access mechanism for the proposed offer an online test. The brief to be considered for the design of the router [16] and from the [16] used and the link to the width of two equal size to 32-bit flit. The title for the address bits (origin and destination) and the virtual channel allocation bits for the selection, are not used in some fields in the header flit, flit. Our proposal for the encoding of the test sample is to utilize the unused fields. Deterministic routing logic, automatic test pattern generation tool to generate the offline test samples. The test samples are available, once set, can be placed in each sample using the header flit. The size of the test pattern does not fit the size of the size of the field is available in the same article, the test pattern to adjust the header flits. In such a situation before it reaches the routing logic of the test sample, it requires two test cycles. NOC infrastructure for managing the routing logic at the time of normal operation of the test samples and the test mode at the time of applying for the test. Routing the logic test remains in test mode at the time of the suspension of the normal operation of the router simultaneously FIFO buffers examination.

CONCLUSION:

In this brief, we SRAM FIFO memories are based on the development of a transparent run-time permanent faults SOA- mats ++, test generation algorithm is proposed to detect. NOC proposed transparent test and periodic testing of the routers used to handle inside the FIFO memory. Periodic testing of the buffers and buffer to prevent the accumulation of faults to test each location. FIFO buffers the periodic examination of the results of the simulation tests of buffers, very often, except when the total throughput of the NOC does not have much effect on the show. We also performed the buffers simultaneously with the test, the test sample for the encoding of the data packets used in the fields of flits title would be the use of an online testing technology for the proposed routing logic. In the future work, we continued testing of incoming data packets to a router under test and would like to modify the proposed FIFO testing technology.

REFERENCES:

[1] W. J. Dally and B. Towels', "Route packets, not wires: On-chip interconnection networks," in Proc. 38th Annul. Design Atom. Conf., 2001, pp. 684–689.

[2] A. Bondavalli, S. Chiaradonna, F. Di Giandomenico, and F. Grandoni, "Threshold-based mechanisms to discriminate transient from intermittent faults," IEEE Trans. Comput., vol. 49, no. 3, pp. 230–245, Mar. 2000.

[3] M. Radetzki, C. Feng, X. Zhao, and A. Jantsch, "Methods for fault tolerance in networks-on-chip," ACM Comput. Surv., vol. 46, no. 1, pp. 1–38, Jul. 2013, Art. ID 8.

[4] S. Ghosh and K. Roy, "Parameter variation tolerance and error resiliency: New design paradigm for the nanoscale era," Proc. IEEE, vol. 98, no. 10, pp. 1718–1751, Oct. 2010.

[5] S. Borri, M. Hage-Hassan, L. Dilillo, P. Girard, S. Pravossoudovitch,and A. Virazel, "Analysis of dynamic faults in embedded-SRAMs: Implications for memory test," J. Electron. Test., vol. 21, no. 2,pp. 169–179, Apr. 2005.

[6] M. Bushnell and V. Agrawal, Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits (Frontiers in Electronic Testing). New York, NY, USA: Springer-Verlag, 2000.

[7] D. Xiang and Y. Zhang, "Cost-effective power-aware core testing in NoCs based on a new unicast-based multicast scheme," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 30, no. 1, pp. 135–147, Jan. 2011.

[8] K. Petersen and J. Oberg, "Toward a scalable test methodology for 2D-mesh network-on-chips," in Proc. Design, Autom., Test Eur. Conf. Exhibit., Apr. 2007, pp. 1–6.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

[9] D. Xiang, "A cost-effective scheme for network-on-chip router and interconnect testing," in Proc. 22nd Asian Test Symp. (ATS), Nov. 2013, pp. 207–212.

[10] M. Ebrahimi, M. Daneshtalab, J. Plosila, and H. Tenhunen,"Minimal-path fault-tolerant approach using connection-retaining structure in networks-on-chip," in Proc. 7th IEEE/ACM Int. Symp. NetwChip (NoCS), Apr. 2013, pp. 1–8.

[11] C. Grecu, P. Pande, B. Wang, A. Ivanov, and R. Saleh, "Methodologies and algorithms for testing switch-based NoC interconnects," in Proc. 20th IEEE Int. Symp. Defect Fault Tolerance VLSI Syst., Oct. 2005, pp. 238–246.