ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Modified Reverse Converter Design with Intervention of Efficacious Parallel Prefix Adders

S.Amirunnisa
PG Scholar
Department of ECE,
Alfa College of Engineering & Technology
Jntu Anantapuram, Allagadda,Kurnool (Dist)-518543.

Mr.M.Mahesh Kumar, M.Tech
Assistant Professor,
Department of ECE,
Alfa College of Engineering & Technology
Jntu Anantapuram, Allagadda,Kurnool (Dist)-518543.

ABSTRACT:

The residue number system (RNS) can play a vital role with the effects of its low-power features and immense performance. In the real time scenario the processes intervene the reverse conversion, i.e., residue to binary conversion, is a hard and time-consuming operation. In the implementation of residue number system reverse converters the anatomy of prefix adders and its hybrid structures scrutinizes in the modified architectures and they are intervened as sub modules. To solve the high power consumption problem, novel specific hybrid parallel- prefix based adder integrants that anticipate better tradeoff between delay and power consumption are here in presented to implement reverse converters. In the design implementations results show noteworthy improvements, which are the major reasons in the composite usage of the parallel-prefix adders to procure the high-speed reverse converter in now a day's system. Demonstrative approaches of top module structures with certain anatomies are also described to design reverse converters based on various kinds of efficacious prefix adders like BRENTKUNG and LANDER FISCHER adders. This approach helps the designer to adjust the performance in the proposed modifications of the reverse converter based on the target application and existing curtailments. However, its real usage requires forward and reverse converters to be integrated in the existing digital systems with the carry-free and fully parallel arithmetic operations for several applications. The RNS can operate mostly with the perplex nature of applications like as digital signal processing, parallel random access machine model of computing, algorithms for sorting integers and cryptography.

Keywords:
Digital Arithmetic, Parallel-Prefix Adder, Residue Number System (RNS), Reverse converter, BRENTKUNG and LANDER FISCHER adders

I.INITIATION:

A residue numeral system (RNS) manipulates a colossal integer with utilizing a stack of smaller integers, so that computation may be effectuate more efficiently. It relies on the Chinese remainder theorem of modular arithmetic for its operation, a mathematical idea from SUN TSU SUAN-CHING, a mathematician. Residue Number Systems (RNS) have significant advantages over conventional binary number systems with their impact attributes of inherent features, such as carry free operations, parallelism, modularity, and fault tolerance. The RNS can decompose in this process a large integer into a set of smaller integers, a large calculation can be performed as a series of smaller calculations that can be performed independently and in parallel for several applications. The reverse converters in the RNS are useful in the processing mode of digital design of filters which are used in frequently in the communication applications related devices. In the manufacture phenomena of power storage-based and compact devices, the residue number system (RNS) can play an emphasis role due to its low-power features and competitive delay. How- ever, its real time usage requires forward and reverse converters to be enact as an integrants in the proposed digital systems to fulfill the future requirements in the manufacture analysis of distinct scale of integrations.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Despite all these advantages, RNS have not found a widespread usage in general purpose processors since sign detection, magnitude comparison, overflow detection, and division are rather difficult to perform. However, several solutions for these problems, which rely heavily on RNS to binary conversion, have been proposed with certain modification to existing systems in the converters. This is one of the major reasons why the research is ongoing the efficacious RNS to Binary converters has become an emphasis role in adder based applications.

II. REVERSE CONVERSION ANALYSIS:

In the design of the traditional reverse converters the anatomies, i.e., which are supported with the residue to binary conversion in the real time research levels are complex in modern improved levels and also show minimal performances. Hence, these problems of designing high-performance reverse converters have motivated continuous research using two main perspectives to improve the performance of the converters:

a) Scrutinize the new algorithms and pre check with the novel arithmetic architectures with the preferable sub modules in the implementation of top module to achieve real time devices suitable results.

b) Insertion of new modules in the existing architectures and which can lead to more simple formulations and we will synthesize with the notable parameters in terms of various parameters area, performance and power consumption. In the existing conversion equations, the significant operations in the overall architecture are run by the well-known adder's architectures, such as carry-save adders (CSAs) and ripple-carry architectures, to implement carry-propagate adders (CPAs) and replaced and differentiated by the efficacious prefix adders in the real time analysis.

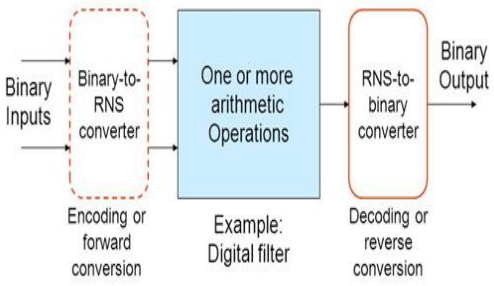


Fig.1.Top view of RNS converter operation

III. IMPLEMENTATION OF HYBRID PREFIX ADDERS

HMPE ADDER

Parallel-prefix adders can be used in the RNS reverse converters to bind the delay to logarithmic growth. However, in reverse converters, several parallel-prefix adders are usually required. Even when only one adder is used, the bit length of this adder is quite large. Consequently, this results in high power consumption notwithstanding its high speed. Primarily two approaches that extract advantage of the delay properties of the parallel prefix adders with competitive power consumption are introduced. Usually, one regular binary addition is required in reverse converter structures to achieve the final binary representation.

Usually, one regular binary addition is required in reverse converter structures to achieve the final binary representation. This final addition has an important effect in the total delay of the converter due to the large bit-length of the operands. A thorough assessment of this final regular addition in recent converter designs shows that one of the operands has some constant bits with value 1.The End Around Carry (EAC) for (2^n-1) addition is represented with two zero, but for the reverse converter design one zero representation is required. To correct these zero representation problem, a detector circuit was employed in the design but it incorporates additional delay.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

So, the Binary to excess one converter (BEC) is used to solve the double zero representation issue. An optimized approach is nothing but which utilizes an extra prefix level to summate the output carry. However, this method suffers from high fan-out, which can make it usable only for small width operands. The major reason for the high power consumption and area overhead of these adders is the recursive effect of generating and propagating signals at each prefix level. However, we could address this problem by eliminating the additional prefix level and using a modified excess-one unit instead. In contrast to the BEC, this modified unit is able to perform a conditional increment based on control signals. Eventually the hybrid modular parallel-prefix excess-one (HMPE) adder is depicted in the architecture.

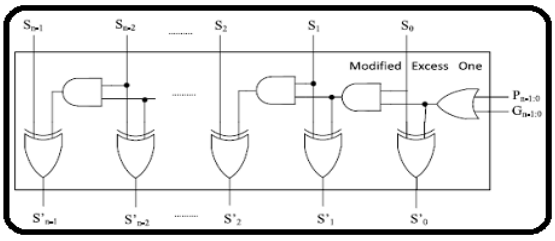


Fig.2. Modified Excess-one unit

With the stimuli (2n – 1) addition is an essential operation in the reverse conversion for most stimuli sets. The regular CPA with end around carry (EAC) is by default a stimuli 2n − 1 adder with double representation of zero, but in reverse converters a single representation of zero is required. So, a one detector circuit has to be used to evaluate the result, which imposes an additional delay. However, there is a binary-to-excess-one converter (BEC), which can be modified to fix the double-representation of zero issue. The HMPE consists of two parts:

1) A regular prefix adder and
2) A modified excess-one unit.

First, two operands are summated by using the prefix adder, and the result is conditionally incremented afterward based on control signals.

Those adders are generated by the prefix parallel operations so as to assure the single zero representation. The result generated by the prefix structure is conditionally incremented by this unit based on the control signal generated by the parallel prefix adder. Summarizing, the HMPE is highly flexible, since it can be used with every prefix networks.

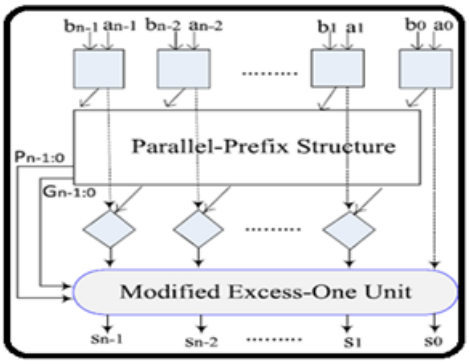


Fig.3. Internal architecture of HMPE adder

Hence, the circuit performance metrics such as area, delay, and power-consumption can be adjusted by selecting the desired prefix structure. On the other hand, the HRPX adder avoids the utilization of a large size parallel-prefix adder with high power consumption, and also does not have the penalty of using the long carry-propagation chain of a RCA.

HRPX ADDER:

The HRPX is depends on the basic operations of prefix adder. The production of the carriers the prefix adders can be designed in many different ways based on the different requirements.

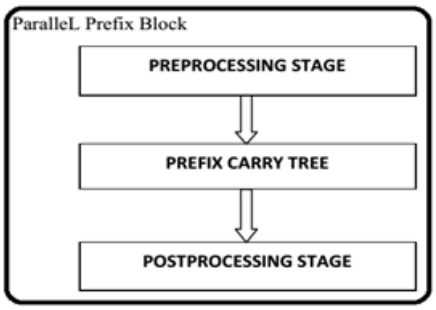


Fig.4. Prefix operation stages of HRPX adder

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

We use the prefix structure form to increase the speed of arithmetic operation. Parallel prefix adders are faster adders and these are faster adders and used for high performance arithmetic structures in industries. The parallel prefix addition is done in three steps.

1. Pre-processing stage
2. Carry generation network
3. Post processing stage

The parallel prefix adder employs the 3-stage structure of the CLA adder. The improvement is in the carry generation stage which is the most intensive one:
1. Pre-calculation of Pi, Gi terms

P = a xor b;

G= a and b;

2. Calculation of the carry part is parallelizable to reduce time. Prefix graphs can be used to describe the structure that performs this part.

Cg= G1 or (P1 and G0);

3. Simple adder to generate the sum.

S1=P1 and C0; [C0=G0];

The Brent Kung adder prefix structure is employed to achieve the higher speed with reduced power consumption. On comparing with the other parallel prefix adder structure the BK adder is chosen mainly for minimum fan-out and should be higher speed in operation than others. The regular parallel prefix adder is used to do the first part of addition and the simplified RCA logic is used to do the second part where the corresponding bits of the operand are fully variable. Full adder can be designed with XOR/OR gates because of the constant operand. In this reverse converter design the carry chain is not needed and can be ignored. For most modulo sets (2^n-1) addition is a necessary operation.

IV.EXISTING REVERSE CONVERTER DESIGN METHODOLOGY

In the existing methodology comprises of selection mode of operation different traditional adders are optioned with the certain conditions.

In this approach there are various adders are positioned according to their insertion of positions with distinct levels of classes. The first class consists of converters with a tree of CSAs with EAC followed by a two-operand modulo 2k− 1 CPA. A second class includes more complex reverse converters, which have several CSAs and CPAs with EACs followed by a final regular operator of subtraction with two operands of different size the implementation of this operator of subtraction using regular binary-adder results in one operand with some constant bits.

The third class covers the reverse converters that have been designed for moduli sets with stimuli's other than the popular 2n and 2n ± 1. The existing reverse converting process applies to the both HMPE and HRPX in the reverse converter. If it is just important to achieve the least power consumption and hardware cost without considering speed, no prefix adder is needed. On the other hand, if high speed is the designer goal, the CPAs with EAC and the regular CPAs should be replaced by traditional parallel prefix modulo 2n – 1 regular parallel-prefix adders, respectively.

However, for the VLSI designers, a suitable tradeoff between speed, power, and area is often more important. In this case, first, CPAs with the EAC can be replaced by the HMPEs. Then, if the converter contains a regular CPA where one of its operands has a string of constant bits with the value of one, it can be replaced with the HRPX. At the last it is relevant to decide about the required performance metrics based on the specified application.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

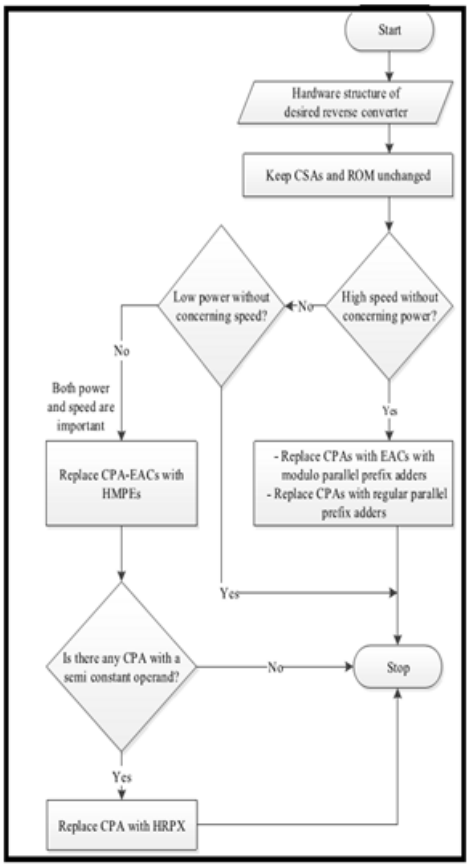


Fig.5. Existing Reverse Converter

Design Methodology

A. Brent-Kung Adder

The Brent-Kung adder is a parallel prefix adder. The Brent-Kung adder was developed by Brent and Kung which they published in 1982. Brent-Kung has maximum logic depth and minimum area. The number of cells are calculated by using 2(n-1) -Log2n. In those operations the Calculation of carries –Prefix Graphs held with the components usually seen in a prefix graphs are the following with the processing component.

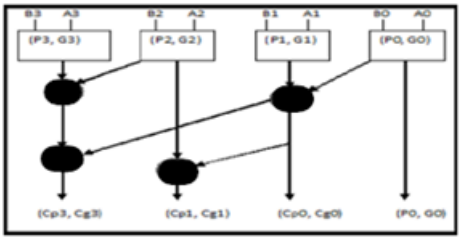


Fig .8.operation of 4-bit BRENT-KUNG adder

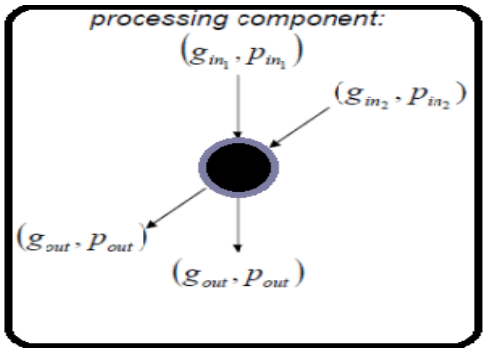


Fig .9.Prefix carry operation

The prefix adder which improves the speed and decreases the memory for the operation of 32-bit addition. The input bits A_i and B_i concentrates on generate and propagate by XOR and AND operations. These propagates and generates undergoes the operations of black cell and gray cell and gives the carry C_i. That carry is XORed with propagate of next bit, which gives sum.

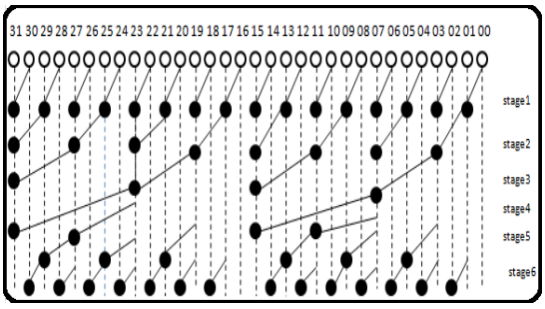


Fig.10. Algorithm of 32-bit BRENT-KUNG adder

The Brent-Kung adder is the extreme boundary case of:

- Maximum logic depth in PP adders (implies effective calculation time).
- Minimum number of nodes (implies minimum area).

V.FUNCTIONAL ANALYSIS OF PROPOSED REVERSER CONVERTER:

As compare with existing reverse converter the proposed reverse converter is more efficient and high speed analysis mode of architecture improvements with the regular stimuli's of different adders like HRPX adders, HMPE adders, Proposed Prefix adders in the analysis of modified reverse converter.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Mainly focus on the improvements in the functionality parameters like Performance, Power and Area with the reduction numbers in terms of Delay, Power Factors and LUTs in our project.

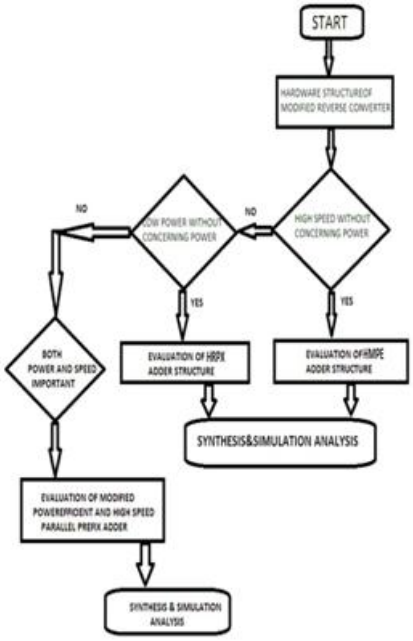


Fig.5. Proposed Modified Reverse Converter

Design Methodology:

The proposed reverse converter has improved the architecture conditions in the simple allocations of certain outputs by verify their input conditions based upon the desired operations like high speed without concerning power, low power without concerning speed and finally both speed and power are important. Within the architecture they undergone the verification analysis of sub-modules with the pre-check of different conditions in the algorithm of modified reverse converter .We obtain the synthesis outputs as per specifications of parameters features in the proposed system of reverse converter with the perfect simulation output. In the modified reverse converter as compare with the existing reverse converters which are used in Residue Number Systems (RNS) the synthesis functions of various parameters shows an effective result.

This reverse converters best novel components in the arithmetic features in future core sectors of chip designs in the performable digital structures those are so useful with the improved architectures as compare with traditional one. By comparing the both existing with 32-bit developed converters with the modified excess-one and the modified reverse converters with the proposed prefix adder structures in the synthesis mode of analysis the results shows of the project evaluation.

VI.REAL TIME SCENARIO OF REVERSE CONVERTER IN RNS

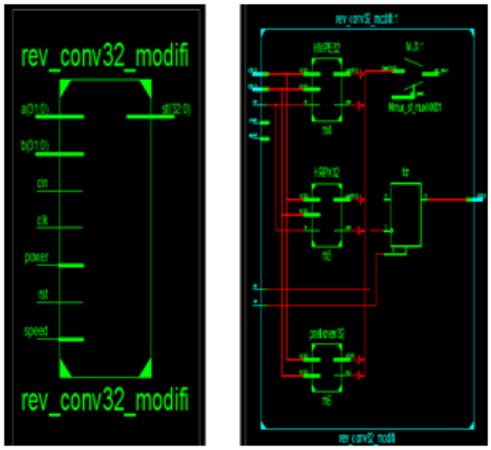
- These reverse converters in the parallel random access machine model of computing, prefix sums can be used to simulate parallel algorithms.
- Reverse converters assume the ability for multiple processors to access the same memory cell at the same time, on parallel machines that forbid simultaneous access.
- In the construction of Gray codes, sequences of binary values with the property that consecutive sequence values differ from each other in a single bit position, a number n can be converted into the Gray code value at position n of the sequence simply by taking the exclusive or of n and n/2 (the number formed by shifting n right by a single bit position).
- Reverse converter (using multiplication as the underlying associative operation) can also be used to build fast algorithms for parallel polynomial interpolation. In particular, it can be used to compute the divided difference coefficients of the Newton form of the interpolation polynomial.
- By those converters counting sort is an integer sorting algorithm that uses the prefix sum of a histogram of key frequencies to calculate the position of each key in the sorted output array.
- Converters runs in linear time for integer keys that are smaller than the number of items, and is frequently used as part of radix sort, a fast algorithm for sorting integers that are less restricted in magnitude.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

- In the performance of RNS/SD (Signed -Digit) the reverse converters are useful.
- The reverse converters in the RNS are useful in the processing mode of digital design of filters which are used in frequently in the communication applications related devices

VII.SYNTHESIS AND SIMULATION ANALYSIS

A.RTL SCHEMATIC VIEW OF TOPMODULE

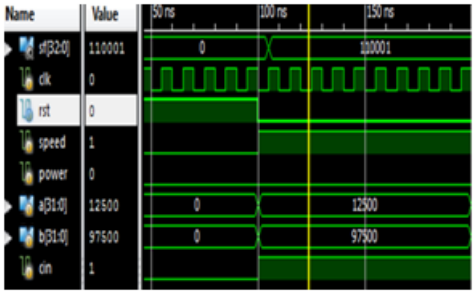


B. Modified reverse converter with extensions of architecture with proposed system

ADDER	NO.OF LUTS	DELAY (ns)	POWER (mw)
REVERSE CONVERTER_32	356	4.28	2.3
HMPE_32	232	19.1	1.6
HRPX_32	191	20.7	1.3
PREFIX_new_32	73	19.6	0.5

TAB.1.SYNTHESIS VALUES OF MODULES

C.SIMULATION RESULTS- PROPOSED REVERSE CONVERTER



VIII.CONCLUSION

In the modified proposed architectures these noteworthy results present a clear-cut of formulation under certain conditions with the efficacious prefix adders that can be applied to most of the current reverse converter architectures to enhance their performance and adjust the cost/performance to the application specifications. Furthermore, in order to provide the required tradeoffs between performance and cost, new parallel-prefix-based adder components were introduced. These components are specially designed for reverse converters. Implementation with effective reposition of prefix adders with the satisfactory levels of synthesis results in terms of various parameters analysis. It shows that the reverse converters based on the suggested components like hybrid prefix anatomies are considered to improve the speed and utilized in the low power applications when ever compared with the original converters.

A.FUTURE SCOPE:

In the research and development of innovative arithmetic architectures are enhanced and confined with these proposed methods of reverse converters in RNS formulation. And also we intervene the most perplex nature of prefix components merged with hybrid adders and propose new kind of structures in these project research in future. Finally with these conditional procure positions of adders elicit the eventual levels of area, power and performance in terms of synthesizable parameters with the implementation of scrutinizes architectures.

IX.REFERENCES:

[1] A. Omondi and B. Premkumar, Residue Number Systems: Theory and Implementations. London, U.K.: Imperial College Press, 2007.

[2] Andrew Beaumont-Smith' and Cheng-Chew Lim' "Parallel Prefix Adder Design"' Department of Electrical and Electronic Engineering' the University of Adelaide' 2001.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

[3] en.wikipedia.org/wiki/Residue_number_system

[4] C. H. Vun, A. B. Premkumar, and W. Zhang, "A new RNS based DA approach for inner product computation," IEEE Trans. Circuits Syst. I.Reg. Papers, vol. 60, no. 8, pp. 2139–2152, Aug. 2013.

[5] R. P. Brent and H. T. Kung, "A regular layout for parallel adders," IEEE Trans. Comput., vol. C-31, pp. 260-264, 1982.

[6] A. S. Molahosseini, S. Sorouri, and A. A. E. Zarandi, "Research challenges in next-generation residue number system architectures," in Proc. IEEE Int. Conf. Comput. Sci. Educ., Jul. 2012, pp. 1658–1661.

[7] D. Harris, "A Taxonomy of Parallel Prefix Networks", IEEE, 2003

[8] R. Brent and H. Kung, "A regular layout for parallel adders," IEEE Trans. Computers, vol.C-31, no. 3, pp. 260-264, March 1982.

[9] Giorgos Dimitrakopoulos and Dimitris Nikolos, "High Speed Parallel Prefix ...Ling adders," IEEE Transactions on Computers, vol.54, no.2, February 2005.

[10] S. Knowles," A family of adders".