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A New Gatefor Low Cost Design of All-Optical Reversible Combinational and Sequential Circuits

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Abstract:
The combinational circuit does not use any memory. Hence the previous state of input does not have any effect on the present state of the circuit. But sequential circuit has memory so output can vary based on input. This type of circuits uses previous input, clock, output and a memory element. Reversible computing offers a possible solution for high performance computing and low power consumption. Recently, in the literature, reversible logic gates and combinational circuits have been proposed using Mach Zehnder Interferometer (MZI) switches due to its advantages. Optical reversible designs have required high cost in terms of MZI switches, Beam splitters, and Beam combiners as well as optical delay. In this work, an optical reversible MNOT gate and all optical realization of combinational circuits and sequential counters using semiconductor optical amplifier (SOA) based MZI switches. All the designs are implemented using minimum number of MZI switches and garbage outputs. Finally, this design ensures improved optical costs in reversible realization of all the counter circuits and the theoretical model is simulated to verify the functionality of the circuits.

Keywords:
Reversible computing, Mach- Zehnder Interferometer, Optical cost, Optical delay, Garbage outputs.

I. INTRODUCTION:

There has been an incredible growth within the contribution and capacity of fiber optic communication networks over the past twenty-five years. To achieve high speed computation, high packing density in the logic circuits is required which results in more heat dissipation. The conventional computing is found unable to deal with low power.

R. Laundaur [1] stated that heat dissipation occurs due to energy loss in irreversible logics. C.H. Bannett [2] stated that reversible logic can overcome the heat dissipation problem of VLSI circuits because the bits of information are not erased in reversible computing. Like Boolean logic functions, reversible logic function is a special type of logic function and exists a bijective mapping between inputs and outputs i.e. number of input lines are equal to number of output lines. For a reversible function, it is always possible to extract original inputs from its outputs correctly, that means it shows no loss of information while retrieving original data. Fan out is not permitted in the reversible logic and constant inputs and garbage output lines can be added to the circuit to make reversible [3, 4]. Reversible logic seems to be hopeful due to its wide application in emerging technologies such as quantum computing, optical computing and power efficient Nano technologies. Recently, the researchers are aiming at the development of the optical digital computer system for processing binary data using optical computation. Optical computing is computation with photon as opposed to conventional electron based computation. This photonic particle provides unmatched speed with information as it has the speed of light. Unmatched high speed and high zero mass of photon have attracted the researches towards the optical realization of reversible logic gates using semiconductor optical amplifier (SOA) based Mach Zehnder Interferometer (MZI) switches. MZI switches which have significant advantages of the high speed, low power, fast switching time and ease of fabrication [5], [6], [7]. It is important to understand that all-optical signal processing is not necessarily a replacement for all electronics, but it can greatly increase the effectiveness and capacity scalability of the overall optoelectronic system.

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Mach Zehnder interferometers incorporating semiconductor optical amplifiers SOAs have recently been developed as very high speed all optical switching devices. The optical computing concept in design and synthesis of reversible logic circuit has first been introduced in [8]. Implementation of reversible logic gate like Feynman and toffoli gates [9] and CNOT [9] using optical technology has been reported. The optical implementation of functionally reversible Mach-Zehnder Interferometer based binary adder has been proposed in [8]. All optical reversible combinational circuits for 2x1 multiplexer [10], Binary Ripple Carry Adder [8], NOR gate [11] are proposed by the authors in the literature. The sequential circuit is one of the important components of the computer system and the efficient of the memory element is a primary concern inn this circuit. As the reversible circuit promises information lossless, fan-out, no heat generation property, an intensive research is going on design and implementation of sequential circuits using reversible logic circuit technology. The necessity for the sequential reversible logic circuits is discussed by toffoli [12] and frank, the first realization of sequential element is a JK flip flop using conservative logic has been proposed by Fredkin, Picton has presented a reversible RS latch in [13].

But Picton's model faces one problem that this model cannot avoid fan-out problem which is essential property of the reversibility. This fan-out problem of picton's model has been solved by Rice [14]. Some preliminary works on the reversible implementation of latches, flip flops, shift registers, counters using quantum technology have been reported by the authors in the literature. Our results have shown significant improvements in terms of MZI Switches, BS, BC and Optical delay. The rest of the paper is organized as follows: Section 2 describes basics of all optical reversible logic gates, in the section 3, proposed all optical reversible combinational gates are presented, The proposed technique with examples is discussed in section 4, in section 5, optical cost and delay of the circuits are discussed. Finally section 6, concludes the work.

II. BASICS OF ALL OPTICAL REVERSIBLE LOGIC GATES:

In this section, first, the fundamental of reversible logic and circuit is introduced. Next, the optical architecture of MZI switch and its working principle are explained. Design of basic reversible gates like Feynman gate, Toffoli gate and fredkin using all optical MZI switches are presented [9][11].

1. Concept of Reversibility:

Reversibility in computing implies that no information about the computational states can ever be lost, so we can recover any past stage by computing backwards. This is called as logical reversibility, low power design, high efficiency and fast processing. Reversible circuits conserve information and this improves the performance of the system. It also improves computational efficiency by minimizing power dissipation and increase portability of device, as it reduce the element size to atomic size. Although due to reversibility the hardware cost of the circuit increases as extra inputs and outputs are required to maintain reversibility but power cost and performance are dominant than hardware cost.

2. MZI Basics:

MZI is a device used to determine relative phase shift between two collimated beams from a coherent light source either by changing length of one of the arms or by placing a sample in path of one of the beams. MZI has two input ports and two output ports. A basic MZI[15] as shown in fig.1 is constructed. Using two couplers, one at the input acts as spitter and another at the output acts as combiner. The light is split in two arms of the interferometer by the output coupler. The optical path length of two arms is unequal making the phase shift corresponding to delay to be a function of wavelength of the input signal. This property is used to design a number of all optical devices used for signal processing in all optical domain.

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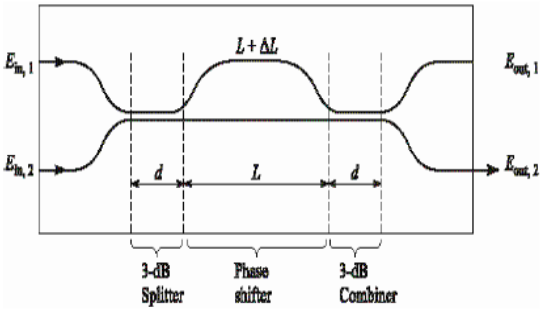

Figure 1. An MZI constructed by interconnecting two 3dB directional couplers

3. Reversible logic gates:

Any Boolean function is said to be reversible if it has one- to – one mapping and bijective. In other words, for every input vector, there must be a unique output vector, and vice versa, A reversible logic gate is the basic unit to design reversible logic circuits as it consists of a cascade of reversible gates, with several constraints. Specifically, the number of input and output ports must be equal, and there cannot be any fan-outs or feedback connections [16], [17]. In a reversible gate netlist, extra inputs known as constant input or ancilla input are often added to make a function reversible and the outputs that are not used in the circuit but required to maintain reversibility are known as garbage outputs.

2.3.1Feynman Gate:

Feynman gate is a 2 x 2 one through reversible gate as shown in figure 2. The input vector is I(A,B) and the output vector is O(P,Q). The outputs are defined by P=A, Q=A □ □ B. Quantum cost of a Feynman gate is 1. Feynman gate (FG) can be used as a copying gate. Since a fan-out is not allowed in reversible logic, this gate is useful for duplication of the required outputs.

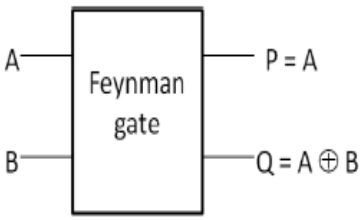

Figure2. Feynman gate

The Feynman gate can be realized using MZI switches (2), beam combiners (2) and beam splitters (3) in all optical domain.

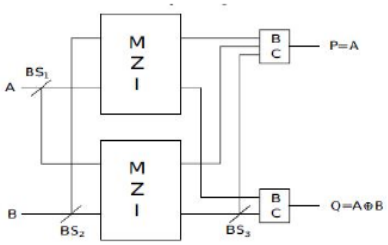

Figure3. Feynman gate using MZI switches

2.3.2 Toffoli Gate:

Figure 4 shows a 4 x 4Toffoli gate. The input vector is I(A,B,C,D) and the output vector is O(P,Q,R,S). The outputs are defined by P=A, Q=B, R=C, S=D⊕ABC

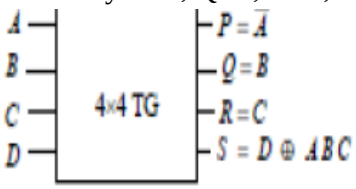

Figure 4.Toffoli Gate

This gate has been realized with MZI switches (4), beam splitters (5), beam combiner (1). The optical delay of this gate is considered as 3Δ.

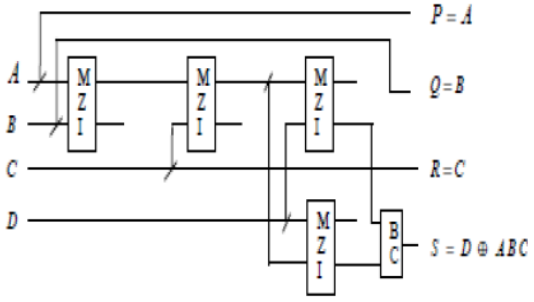

Figure5. Toffoli gate using MZI Switches

III. ALL OPTICAL REVERSIBLE COMBINATIONAL GATES USING PROPOSED MNOT GATE:

A new 2x2 all-optical reversible MNOT gate (1,A) to outputs (P,Q) has been proposed, where P=A, Q=~A. figure 6 shows the block diagram of MNOT gate. This gate generates logical NOT of the input logic A.

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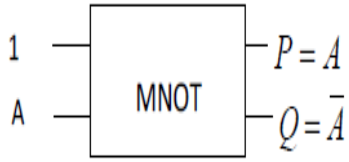

Figure6. 2x2 MNOT gate

The optical cost of MNOT gate is 1. No beam splitter or beam combiner is used in this gate. As only one MZI switch is used, so the delay is 1Δ.

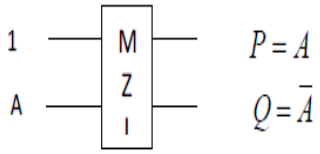

Figure7. 2 x 2 MNOT gate using MZI switch

3.1 All Optical Reversible 2x1 Multiplexer:

This section describes the design and realization of the reversible 2x1 multiplexer in all optical domain using the proposed MNOT gate and optical toffoli gate. It has two data inputs (D_0, D_1), a single output O and a select line to select one of the two input data lines. The output function of 2x1 multiplexer is given by $O = (\sim S_0)D_0 + S_0D_1$.

Input			Output
D_0	D_1	S_0	O
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

Table 1 Truth table of 2x1 multiplexer

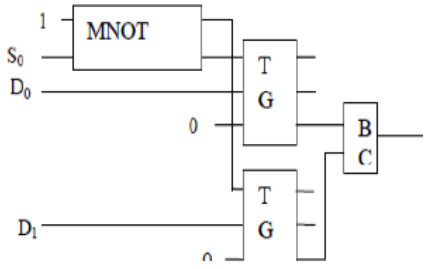

Figure 8. Optical realization of 2x1 Reversible multiplexer

Total optical cost of optical reversible 2x1 multiplexer is 7 MZI switches, 8 Beam splitters, 3 Beam combiners are used and delay of the multiplexer circuit is calculated as 3Δas the two TG are working in parallel.

3.2 Design of optical reversible 4x1 multiplexer:

The all optical reversible 4x1 multiplexer circuit has been realized with proposed optical reversible MNOT gate and optical 4x4 toffoligate. It has four data input lines (D_0 – D_3), two selection lines S_0 and S_1 to select one of the four inputs and a single output line O. The expression for the data output O is given as $O = D_0(\sim S_0)(\sim S_1) + D_1S_0(\sim S_1) + D_2(\sim S_0)S_1 + D_3S_0S_1$.

Input		Output
S_1	S_0	O
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

Table 2. Truth table of 4x1 multiplexer

The optical realization of 4x1 reversible multiplexer is shown in the figure 9. It is designed using two MNOT gates and four optical 4x4 TG gates. The 4x4 TG is realized with four MZI switches, 5 Beam splitters and 1 Beam combiner. The delay of this gate is considered as 3Δ. Thus, the optical cost of all optical 4x4 reversible multiplexer circuit comes out to be 18 MZI switches, 24 BS, 5BC. The delay is calculated 4Δas two MNOT gates as well as four 4x4 TG are working in parallel.

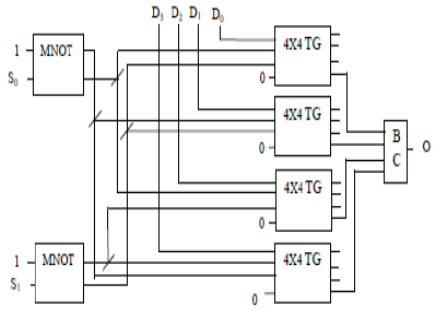

Figure 9.design of 4x1 optical reversible Multiplexer

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3.3Design of optical Reversible 1x4 De-Multiplexer:

The all optical reversible 4x1 de multiplexer circuit has been realized with MNOT gate and 4x4 TG. It has one input data line D, 2 select input lines (S_0 and S_1) and 4 output lines (O_0 – O_3). The expression for output lines are given as $O_0 = D\ (\sim S_1)(\sim S_0)$, $O_1 = DS_0(\sim S_1)$, $O_2 = D(\sim S_0)S_1$, $O_3 = DS_0S_1$.

Input		Output			
S_1	S_0	O_3	O_2	O_1	O_0
0	0	0	0	0	D
0	1	0	0	D	0
1	0	0	D	0	0
1	1	D	0	0	0

Table 3. Truth table of 1x4 multiplexer

The optical reversible 1x4 de- multiplexer is shown in the figure 10. It is designed using 2 MNOT gates and four 4x4 TG gates. This circuit is designed using 18 MZI switches, 27 Beam splitters, 4 Beam combiners. 2 MNOT gates as well as four 4x4 TG are connected in parallel. Thus, Delay is calculated as 4Δ.

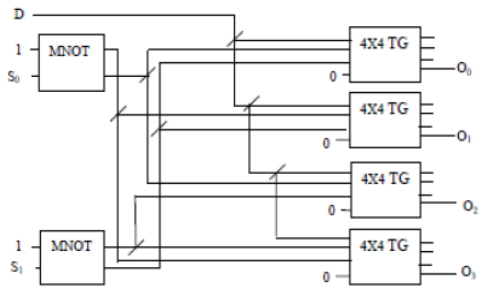

Figure 10. Optical realization of 1x4 De multiplexer

3.4 Design of optical reversible 3 to 8 Decoder:

A decoder circuit is similar to the De-multiplexer but there is no data input line. A 3 to 8 decoder has 3 input lines (P, Q, R) and eight output lines (O_0 – O_7). The output function of the 3 to 8 decoder is expressed as $O_0 = (\sim P)(\sim Q)(\sim R)$, $O_1 = (\sim P)(\sim Q)(R)$, $O_2 = (\sim P)(Q)(\sim R)$, $O_3 = (\sim P)(Q)(R)$, $O_4 = (P)(\sim Q)(\sim R)$, $O_5 = (P)(\sim Q)(R)$, $O_6 = (P)(Q)(\sim R)$, $O_7 = PQR$.

Input			Output							
P	Q	R	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

Table 4. Truth table of 3 to 8 Decoder

Optical reversible 3 to 8 decoder is designed using the proposed MNOT gate and optical 4x4 TG. To realize this circuit 3 MNOT gates and eight 4x4 TG gates are used. The circuit is designed with 35 MZI switches, 58 Beam splitters, 8 Beam combiners. Delay of this circuit is 4Δ.

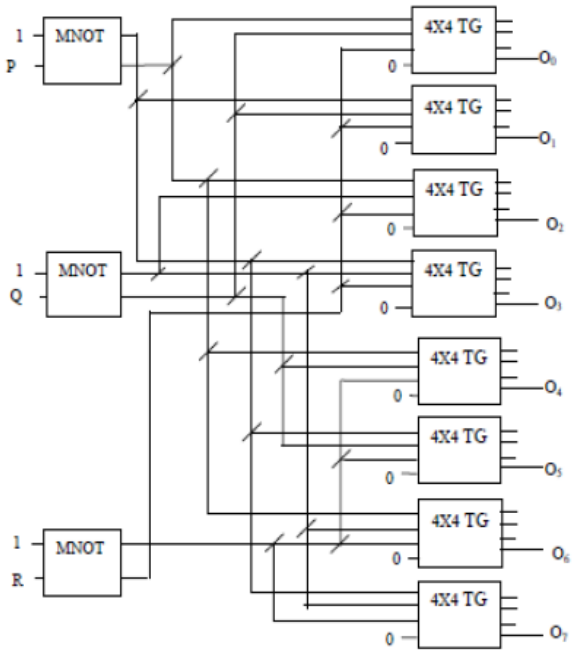

Figure 11. Optical realization of the reversible 3 to 8 Decoder

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Proposed Design	MZI Switch	BS	BC	Optical delay
4×1 multiplexer	18	24	5	4Δ
1×4 De-multiplexer	18	27	4	4Δ
3to8 Decoder	35	58	8	4Δ

Table5. Optical Cost and Delay of All optical Reversible Circuits

IV. PROPOSED ALL OPTICAL REVERSIBLE SEQUENTIAL CIRCUITS:

In this section, all optical implementation of counters with the property of functional reversibility. Semiconductor optical amplifier based MZI switches are used to design the sequential circuits. Primary objective inthis work is to achieve the reversible implementation of counters with minimum number of ancilla lines and MZI switches. All optical implementation of MZI based asynchronous and synchronous counter is presented. Finally, design complexities of all the counters are analyzed.

4.1 Asynchronous Counters:

Asynchronous counter is known as ripple counter. Design architecture and working principle of all optical functionally reversible asynchronous down counter is presented here.

4.1.1 Positive edge triggered down counter:

The schematic diagram of MZI based positive edge triggered down counter is shown in figure 12, which is constituted with two positive edge triggered D flip flops. Each of the positive edge triggered D flipflop consists of three MZI switches, 2 Beam combiners and 4 Beam splitters. A light from input port clock pulse directly incidents on MZI 1 of first flip-flop and acts as incoming signal. Similarly, another light from input port D_0 directly enters into MZI 1 of first flip-flop and acts as control signal of MZI 1. The light from bar port of MZI 1 (B1) and a part of light from cross port of MZI 3 (C3) is combined by BC 1 together to produce control signal of MZI 2.

The output lights from cross port of MZI 1 (C1) and MZI 2 (C2) are combined by BC 2 and acts as control signal of MZI 3. A constant light signal incidents on the beam splitter (BS 1) and splits into two parts. Where one part acts as incoming signal of MZI 3 and another part again incidents on another beam splitter (BS 2) and splits into two parts. One part appears to MZI 2 as incoming signal and another part that goes to next flip flop accts as a constant input light signal. The light from the cross port of MZI 3 (C3) is the final output Q_0 where as another light signal which emits from the cross port of MZI 2 (C2) goes back to port D_0 and acts as incoming signal. A part of light comes from BS 5 of first flipflop incident on MZI 1 of second flipflop. Again D_1 acts as the input value of first flipflop. We have obtained both the signals for second flipflop and the design architecture of second flipflop is same as first flip, we neglected the control flow description of second flipflop.

4.1.2 Operational principle of 2 bit positive edge triggered down counter:

The operational principle of all the optical asynchronous down counter as shown in figure12, is described below. Here, the presence of light is denoted as 1 state and absence of light is denoted as 0 state. State 1: Let $Q_0 = 0$ and $Q_1 = 0$. As D_0 is directly connected to Q_0, hence the value of D_0 is 1. Now, the value of clock pulse is 1 i.e., both the control signal and incoming signal are present in MZI -1. Hence, according to the working pri nciple of MZI, only bar port of MZI 1 of first flipflop emits light which incidents on BC 1 and as a result, an output light signal emits from BC 1. On the contrary, the cross light signal emits from BC 1 on the contrary, the cross port of MZI 1 emits no light which incidents on BC 2. Now, the output signal of BC 1 acts as the control signal of MZI 2 and the input signal of MZI 2 is also present.Therefore, the cross port of MZI 2emits no lights, as a result, no light incidents on BC 2. The output signal of BC 2 emits no light and as a consequence, the control signal of MZI 3 is absent. As the input signal of MZI 3 is present, the cross port of MZI 3 of first flipflop receives light which is the final output Q_0 i.e. $Q_0 = 1$.

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Now, this Q_0 acts as incoming signal of MZI 1 of first flipflop and D_1, which is directly connected to the Q_1 bar, acts as control signal of MZI 1. Therefore, both the incoming signal and control signal are present at MZI 1 as both the value of D_1 and Q_0 are 1. Hence the operation principle of flipflop 1 becomes similar to flrstflipflop and the cross port of MZI 3 of second flipflop emits light means $Q_1 = 1$. So the next stste becomes $Q_1 = 1$ and $Q_0 = 1$. State 2: Now, $Q_1 = Q_0 = 1$. Again the clock pulse is equal to 1 and D_0 acts as incoming signal and control signal of second flipflop MZI 1. Hence, only incoming signal is present at MZI 1. According to the working principle of MZI, the bar port of MZI 1 of first flipflop emits no light and cross port of MZI 1of first flipflop emits light which incidents on BC 2. So the output signal of BC 2 is present that acts as control signal of MZI 3. Again the input signal of MZI 3 is also present. So the cross port of MZI 3 receives no light that means the value of final output Q_0 =0. This output Q_0 acts as incoming signal of MZI 1 of first flipflop and D_1 is directly connected to Q_1bar. so the value of D_1 is directly connected to Q_1bar. So the value of D_1 is 0.

As both the incoming signal and control signal are absent at MZI 1 of second flipfflop, no operation is performed in second flipflop. Hence the final output value of second flipflop does not change and it is same as the previous state's output value of Q_1. Therefore, the final output of first flipflop is $Q_1 = 1$. So the next state becomes Q_1 =1, $Q_0 = 0$. State 3: Now, Q_1 =1, Q_0 =0. The value of D_0 is 1 and the value of clock pulse is 1 means both the control signal and incoming signal are present at MZI 1. So the situation becomes same as that of first flipflop at first stage. Hence, according to working principle of first flipflop is 1 means $Q_0 = 1$. As Q_0 acts as incoming signal of MZI 1 of second flipflop and D_1 is 0. Therefore only incoming signal is present at MZI 1 of second flipflop. This situation is same as first flipflop of second stage. Hence according to the working principle of first flipflop as described in second stage, the final output of second flipflop is 0 means $Q_1 = 0$. So the next state becomes $Q_1 = 0$ and $Q_0 = 1$. State 4: in this state, $Q_1 = 0$, $Q_0 = 1$ and the value of D_0 is 0.

As the value of clock pulse is 1, only incoming signal is present at MZI 1 of first flipflop. This situation is same as second stage of first flipflop. Hence according to working principle of first flipflop as described in second stage, the final output of first flipflop is 0 means $Q_0 = 0$. Now this Q_0 acts as the incoming signal of MZI 1 of second flipflop and D_1 is directly connected to complement of Q_1. So the value of D_1 is 1. As the incoming signal is absent at MZI 1 of second flipflop, no operation is performed in second flipflop. Therefore the final output value of second flipflop is not changed and it is same as previous state of Q_1.Finally, the output of second flipflop is $Q_1 = 0$. So the next state becomes $Q_1 = 0$ and $Q_0 = 0$.

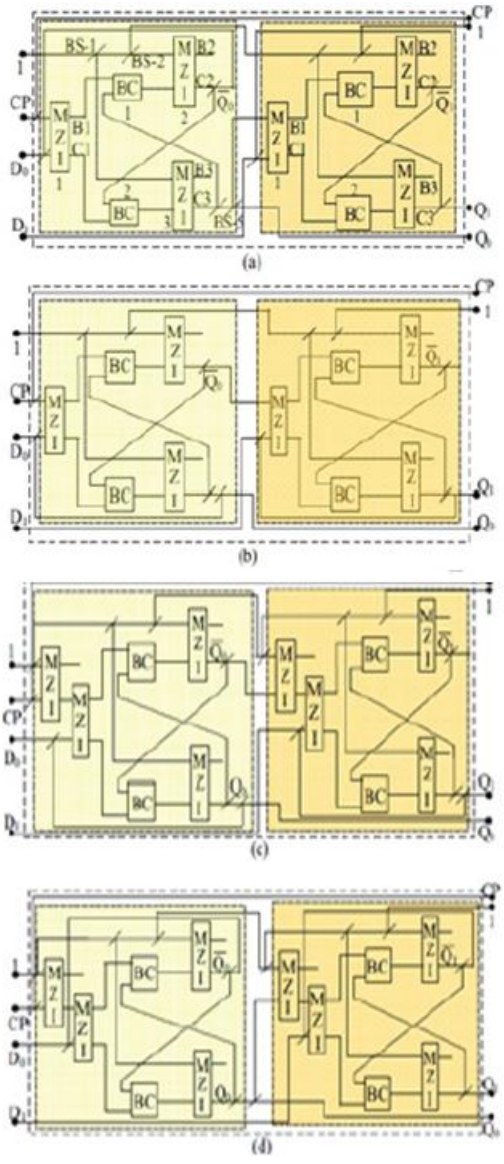

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Figure 12 Design of all optical reversible
a) asynchronous positive edge triggered down counter
b) asynchronous positive edge triggered up counter
c) asynchronous negative edge triggered down counter
d) asynchronous negative edge triggered up counter

Clock Pulse	FF-0				FF-1			
	CP_0	Q_0	D_0 $(\bar{Q}_0)$	Q_0^+	CP_1 (Q_0^+)	Q_1	D_1 $(\bar{Q}_1)$	Q_1^+
First	1	0	1	1	1	0	1	1
Second	1	1	0	0	0	0	1	1
Third	1	0	1	1	1	1	0	0
Fourth	1	1	0	0	0	0	1	0
Fifth	1	0	1	1	1	0	1	1

Table 6.Different states of positive edge triggered down counter

4.2 Synchronous Counter:

In the synchronous counter, all the flipflops are triggered simultaneously. As we have already explained the working principle of asynchronous counter. Here only the pictorial representation of all optical reversible architecture of MZI based synchronous negative edge triggered up counter and positive edge triggered down counter is shown in figure 13 a), b) respectively.

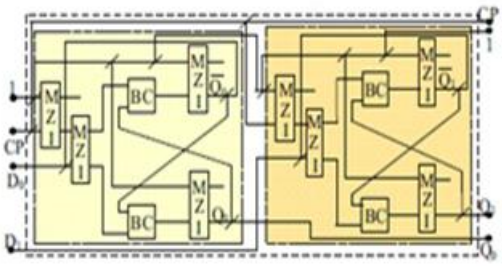


Figure 13 a) synchronous negative edge triggered up counter

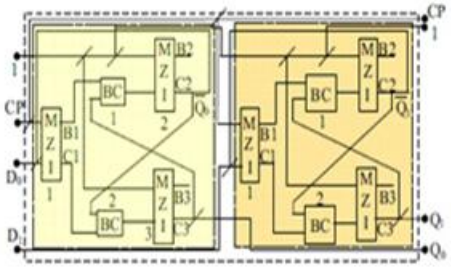
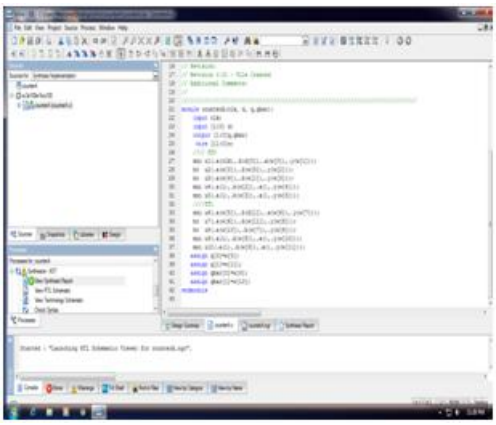


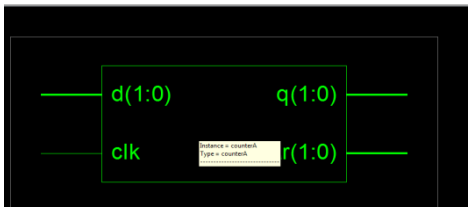
Figure 13 b) synchronous positive edge triggered down counter

V. SYNTHESIS AND SIMULATION RESULTS:

We have coded the reversible sequential counters in Verilog HDL using the proposed with MZI design. All the designs are synthesized with Xilinx synthesis tool and simulated using Xilinx ISE simulator. The simulation results are shown below for asynchronous positive edge triggered down counter.

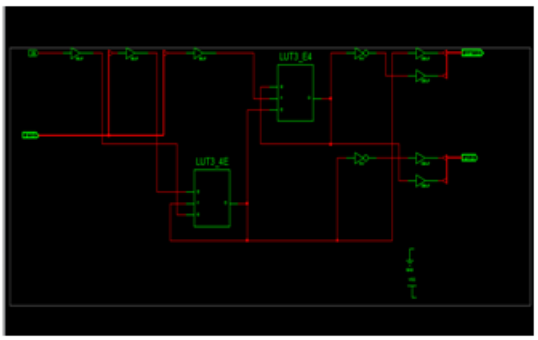


Program of asynchronous positive edge triggered down counter



RTL schematic

Technological schematic



Technological schematic

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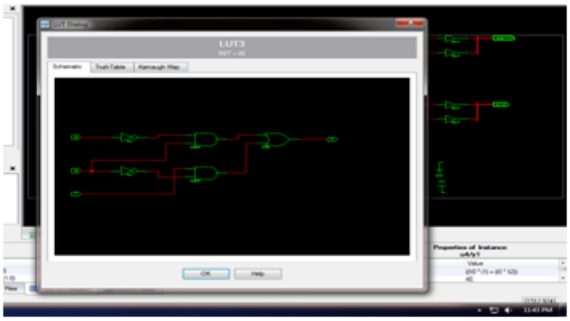
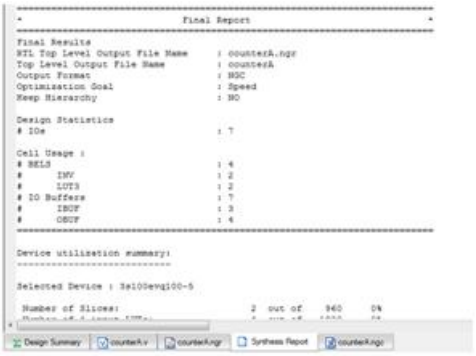
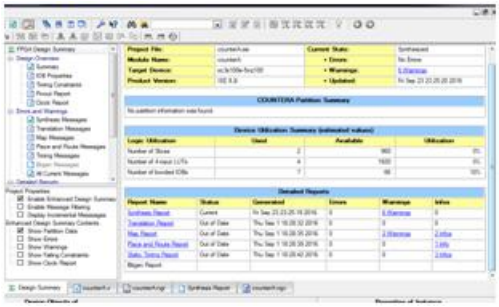


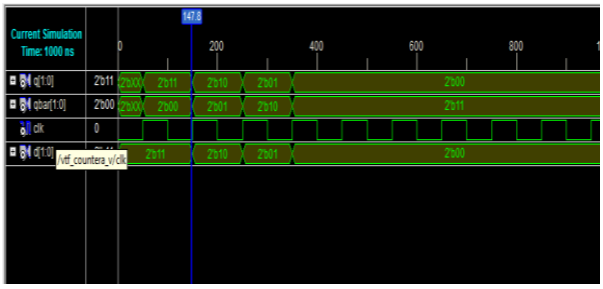
Internal block of look up table



Synthesis Report



Device utilization summary



Test Bench for asynchronous Positive edge triggered down counter

VI. CONCLUSION:

Optical computing is emerging as a feasible technology to implement reversible logic. We have proposed a new general design approach to realize all optical reversible logic circuits using SOA based MZI switches. An all optical MNOT gate has been proposed. Using MNOT gate 2x1 multiplexer, 4x1 multiplexer, 1x4 de-multiplexer, and 3 to 8 decoder are implemented. In this paper, various architectures of MZI based functionally reversible all optical counters have been proposed. Our proposed design can be generalized for n- bit counter also.

Different types of *n*-bit counters		No. of MZI (Optical Cost)	No. of Beam Combiner	No. of Beam splitter	Garbage Output
Asynchronous	down counter (positive edge-triggered)	3*n*	2*n*	6*n*	4
	up counter(negative edge-triggered)	4*n*	2*n*	7*n*	6
Synchronous	up counter(negative edge-triggered)	4*n*	2*n*	7*n*	6
	down counter (positive edge-triggered)	3*n*	2*n*	6*n*	4

Analysis on design complexities of all optical reversible counters

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