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Design and Study of a Low Power High Speed Full Adder Using GDI Multiplexer

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ABSTRACT:
The binary adder is the critical element in most digital circuit designs including digital signal processors (DSP) and microprocessor data path units. As such, extensive research continues to be focused on improving the power delay performance of the adder. This paper proposes a new method for implementing a low power full adder by means of a set of Gate Diffusion Input (GDI) cell based multiplexers. Full adder is a very common example of combinational circuits and is used widely in Application Specific Integrated Circuits (ASICs). It is always advantageous to have low power action for the sub components used in VLSI chips. The explored technique of realization achieves a low power high speed design for a widely used subcomponent- full adder. Simulated outcome using stateof-art simulation tool shows finer behavioral performance of the projected method over general CMOS based full adder. Power, speed and area comparison between conventional and proposed full adder is also presented.

Keywords:
Low power full adder, 2-Transistor GDI MUX, ASIC (Application Specific Integrated Circuit), 12-TFA, CMOS (Complementary Metal Oxide Semiconductor).

I. INTRODUCTION:
The binary addition is the basic arithmetic operation in digital circuits and it became essential in most of the digital systems including Arithmetic and Logic Unit (ALU), microprocessors and Digital Signal Processing (DSP). At present, the research continues on increasing the adder's delay performance.

In many practical applications like mobile and tale communications. With the tremendous progress of modern electronic system and the evolution of the nanotechnology, the low- power & high speed microelectronic devices has come to the forefront. Now a day, as growing applications (higher complexity), speed and portability are the major concerns of any smart device it demands small-size, low-power high throughput circuitry. So, sub circuits of any VLSI chip needs high speed operation along with low-power consumption. Now a day logic circuits are designed using pass transistor logic techniques. In PTL based VLSI chips MOS switches are used to propagate different logic values in various node points, as it reduces area and delay as compared to any other switches type [1].

It reduces the number of MOS transistors used in circuit, but it suffers with a major problem that output voltage levels is no longer same as the input voltage level. Each transistor in series has a lower voltage at its output than at its input [2]. In order to minimize sneak paths, charge sharing, and all the sub-circuit component has to be arranged obeying the VLSI design rules. Ensuring this simulation of circuit schematics provides a platform to verify circuit performance [3]. To get better speed and power consumption results lot of approaches have been recently proposed [4]-[7]. Among them, two have been established by Hitachi CPL [4] and DPL [6]. In 1993 Hitachi demonstrated a 1.5ns 32-bit ALU in 0.25µm CMOS technology [6] and 4.4ns 54X54 bit multiplier [7] using DPL technique.

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Like Pass Transistor Logic (PTL), Domino logic, NORA logic, Complementary Pass Logic (CPL), Differential Cascode Voltage Switch (DCVS), MOS Current Mode Logic (MCML), Clocked CMOS (C2MOS etc.[8][9] are also different approach for reducing the circuit power. In 2002, A. Morgenshtein, A. Fish, and Israel A. Wagner introduced a new method for low-power digital combinational circuit design known as Gate Diffusion Input (GDI) [10]. The main purpose of this work is to implement a low power GDI based full adder & to draw a detailed comparative study with a CMOS full adder. The purpose of implementing the low power full adder is to show that using fewer numbers of transistors in comparison to the conventional full adder, the propagation delay time & power consumption gets reduced. It also helps in reducing the layout area thereby decreasing the entire size of a device where this adder is used. Power consumption is becoming the major tailback in the design of VLSI chips in modern process technologies. These are evaluated from an industrial product development perspective.

II. EXISTING DESIGN:

The Full Adder circuit adds three one-bit binary numbers (a, b & c) and outputs two one-bit binary numbers, a sum (s) and a carry (co). The full adder is usually a component in cascade of adders, which add 4, 8, 16 etc. binary numbers. Implementation of full adder circuit using GDI technique which is a basic building block of arithmetic and logic unit has been shown in Fig. 1.

While taking account of full adder the sum and carry outputs are represented as the following two combinational Boolean functions of the three input variables a, b and c.

Sum =a xor b xor c ------- eqn.1
Carry = ab + ac + bc ------ eqn.2

Accordingly the functions can be represented by CMOS logic as follows in fig. 1,

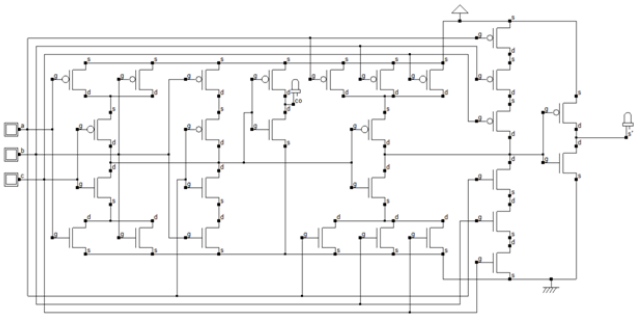

Fig. 1. Conventional 28-T CMOS 1 bit full adder

GDI technique based full adder have advantages over full adder using pass transistor logic or CMOS logic and is categorized by tremendous speed and low power. The technique has been described below.

III. GATE DIFFUSION INPUT (GDI):

Morgenshtein has proposed basic GDI cell shown in Fig.1 [8]. This is a new approach for designing low power digital combinational circuit. GDI technique is basically two transistor implementation of complex logic functions which provides in-cell swing restoration under certain operating condition. This approach leads to reduction in power consumption, propagation delay and area of digital circuits is obtained while having low complexity of logic design. An important feature of GDI cell is that the source of the PMOS in a GDI cell is not connected to VDD and the source of the NMOS is not connected to GND. Therefore GDI cell gives two extra input pins for use which makes the GDI design more flexible than CMOS design.

A. GDI Cell:

Technique the GDI technique offers realization of extensive variety of logic functions using simple two transistor based circuit arrangement. This scheme is appropriate for fast and low power circuit design, which reduces number of MOS transistors as compared to CMOS and other existing low power techniques, while the logic level swing and static power dissipation improves. It also allows easy top-down approach by means of small cell library [5]. The basic cell of GDI is shown in Fig. 2.

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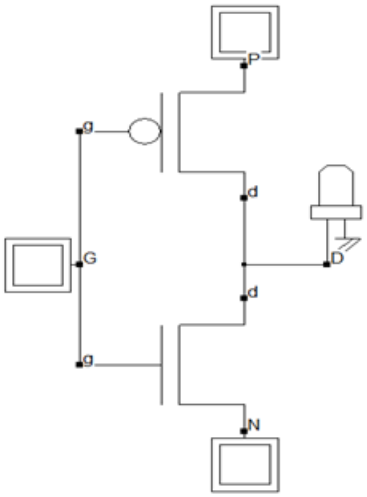

Fig 2 GDI basic cell consisting of PMOS and NMOS

1) The GDI cell consists of one nMOS and one pMOS. The structure looks like a CMOS inverter. Though in case of GDI both the sources and corresponding substrate terminals of transistors are not connected with supply and it can be randomly biased.

2) It has three input terminals: G (nMOS and pMOS shorted gate input), P (pMOS source input), and N (nMOS source input). The output is taken from D (nMOS and pMOS shorted drain terminal) [11].

GDI logic style approach consumes less silicon area compared to other logic styles as it consists of less transistor count. In view of the fact that, the area is less, the value of node capacitances will be less and for this reason GDI gates have faster operation which presents that GDI logic style is a power efficient method of design. We can realize different Boolean functions with GDI basic cell. Table I shows how different Boolean functions can be realized by using different input arrangements of the GDI cell.

Table I. GDI Cell Based Various Logic Functions Using Different Input Configurations and Corresponding Transistor Counts

N	P	G	OUTPUT	FUNCTION	TRANSISTOR COUNT
0	1	A	A'	Inverter	2
0	B	A	A'B	F1	2
B	1	A	A'+B	F2	2
1	B	A	A+B	OR	2
B	0	A	AB	AND	2
C	B	A	A'B+AC	MUX	2
B'	B	A	A'B+B'A	XOR	4
B	B'	A	AB+A'B'	XNOR	4

VI. ARCHITECTURE OF PROPOSED FULL ADDER

The basic architecture of the 2:1 MUX using GDI method is shown in fig. 3. In this configuration we have connected PMOS and NMOS gate along with a SEL line 'A', as in MUX. As we know that PMOS works on ACTIVE LOW and NMOS works on ACTIVE HIGH. So, when the SELECT input is low (0) then the PMOS get activated, and show the input 'B' in the output and due to low input (0) the NMOS stands idle, as it is activated in high input.

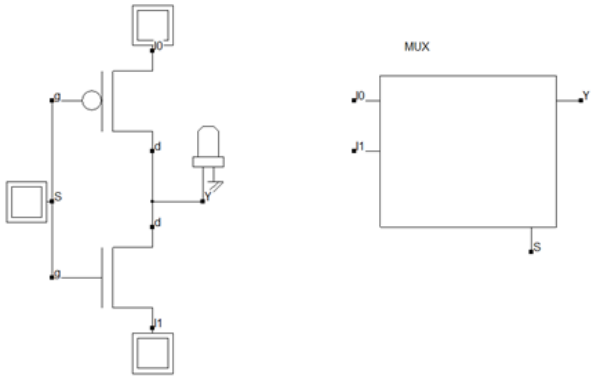

Fig.3 Basic view of 2T MUX using GDI technique

Same for the case, while the G input is high (1) then the NMOS get activated, and show the input 'C' at the output. Thus this circuitry behaves as a 2-input MUX using 'A' as SEL line, and shows the favorable output as 2:1MUX.

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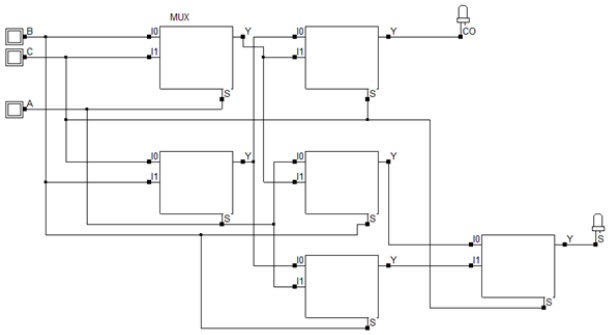

Fig.4 Block Diagram of Low Power Proposed Full Adder using 2T MUX

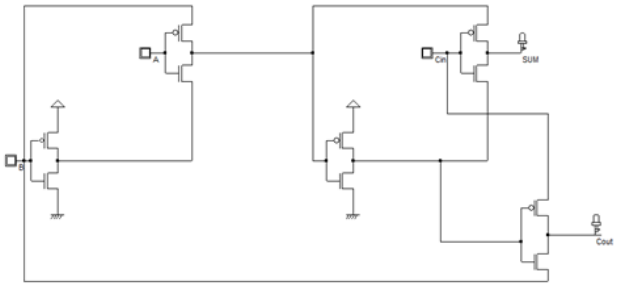

Fig.5 Block Diagram of Low Power Proposed Full Adder using 10T

Now we are implementing the low power full adder circuit with the help of 2T MUX, made by GDI technique. It require total 6 numbers of 2T MUX having same characteristics to design a 12T full adder and connected as above in fig.4 [5]. The truth table for the above circuit taking each MUX as consideration are shown table II, and from there it generates 6 various outputs of various MUX.

TABLE II. Truth Table Of Low Power Full Adder Using 2t MUX

A	B	Cin	MUX1	MUX2	MUX3	MUX4	MUX5	MUX6	SUM	Cout
0	0	0	0(B)	0(Cin)	0(Cin)	0(A)	0(Cin)	0(A)	0(A)	0(Cin)
0	0	1	0(B)	1(Cin)	0(B)	0(A)	1(Cin)	1(Cin)	1(Cin)	0(B)
0	1	0	1(B)	0(Cin)	0(Cin)	1(B)	0(A)	1(B)	1(B)	0(Cin)
0	1	1	1(B)	1(Cin)	1(B)	1(B)	0(A)	0(A)	0(A)	1(B)
1	0	0	0(Cin)	0(B)	0(B)	1(A)	0(B)	1(A)	1(A)	0(B)
1	0	1	1(Cin)	0(B)	1(Cin)	1(A)	0(B)	0(B)	0(B)	1(Cin)
1	1	0	0(Cin)	1(B)	1(B)	0(Cin)	1(A)	0(Cin)	0(Cin)	1(B)
1	1	1	1(Cin)	1(B)	1(Cin)	1(Cin)	1(A)	1(A)	1(A)	1(Cin)

LOGIC ANALYSIS:

The digital circuit shown in the fig. 4 can be analyzed logically with the help of simple Boolean algebra. The outputs of each MUX can be analyzed to get the sum & carry.

$$MUX1 = (B\bar{A}+CA)$$

$$MUX2 = (C\bar{A}+BA)$$

$$MUX3 = [(C\bar{A}+BA)\bar{C}+(B\bar{A}+CA)C]$$
$$= AB\bar{C}+\bar{A}BC+AC$$
$$= AB\bar{C}+\bar{A}BC+AC(B+\bar{B})$$
$$= AB\bar{C}+\bar{A}BC+ABC+A\bar{B}C$$
$$= AB\bar{C}+ABC+\bar{A}BC+ABC+A\bar{B}C+ABC$$
$$= AB(C+\bar{C})+BC(A+\bar{A})+AC(B+\bar{B})$$
$$= AB+BC+CA = Cout$$

$$MUX4 = \bar{A}\bar{B}+(\bar{A}B+AC)B$$

$$MUX5 = (C\bar{A}+BA)\bar{B}+AB$$

$$MUX6 = [\bar{A}\bar{B}+(\bar{A}B+AC)B]\bar{C}+[(C\bar{A}+BA)\bar{B}+AB]C$$
$$= A\bar{B}\bar{C}+\bar{A}B\bar{C}+\bar{A}\bar{B}C+ABC = A \oplus B \oplus C = Sum$$

Logic transition, short-circuit current and leakage current are the three main sources of power dissipation in CMOS VLSI circuits [6], [7]. During the transition of output from one logic level to other both the NMOS and PMOS transistors become active and provides a short circuit path directly between supply to ground which increases the power consumption of the circuit [2], [6]. As the proposed 12-T full adder is made of GDI based MUX , it does not provide direct connections between supply and ground, so the probability of a getting short circuit current during switching can be considerably reduced; i.e, the power consumption due to short circuit current is considerably small. Again, in the proposed 12T full adder, all the select line of the MUX i.e. the G nodes of the GDI cells are directly connected with the input signals, results a much faster transition (less delay) in its output signals. As a result, the power consumption of the final pad out stage is low and it can provide faster Sum and Cout outputs.

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V.SIMULATION RESULTS:

All the simulations are performed on Microwind and DSCH 3.5. The main focus of this work is to meet all challenges faces in designing of full adder circuit, The power and area in proposed mux based full adder is improved as compared to conventional full adder. The simulation results are shown below figures.

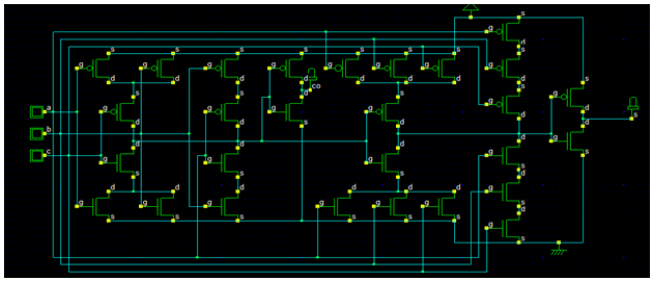

Fig 5: Schematic of 28T Full adder

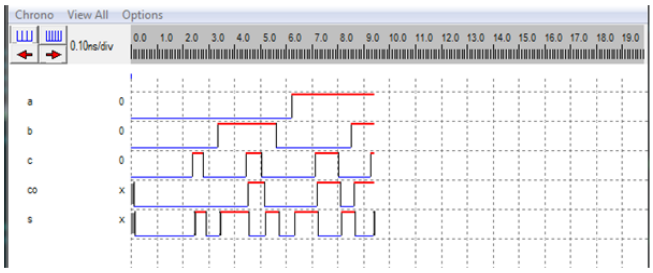

Fig 6: Timing Diagram of 28T Full adder

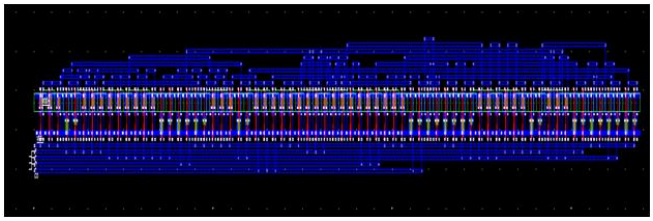

Fig 7: Layout of 28T Full adder

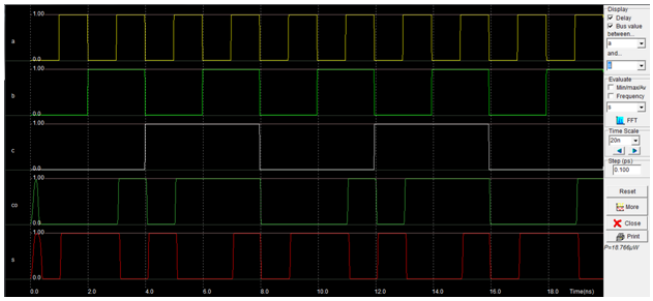

Fig 8: Simulation of Layout of 28T Full adder

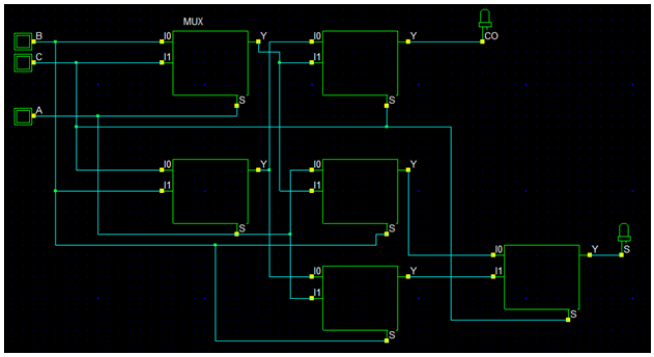

Fig 9: Schematic of 12T Full adder

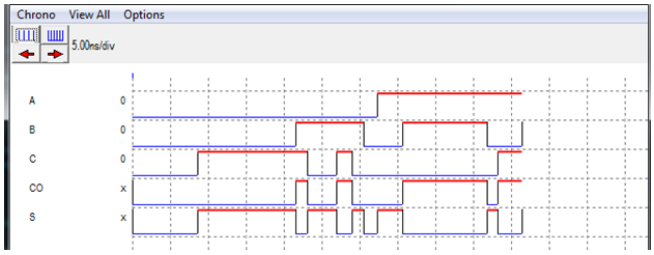

Fig 10: Timing Diagram of 12T Full adder

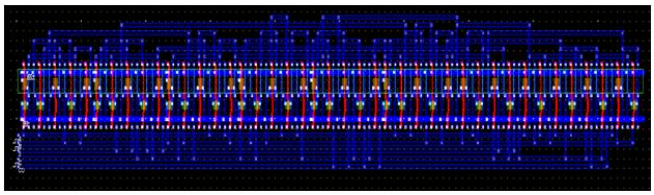

Fig 11: Layout of 12TFull adder

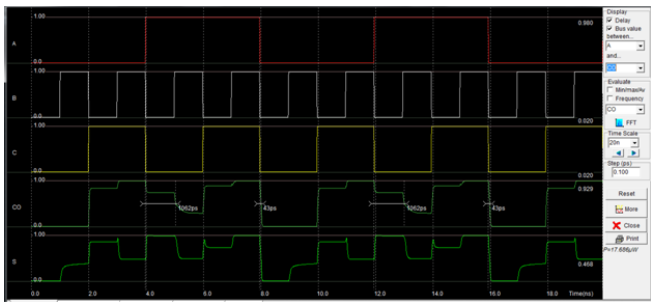

Fig 12: Simulation of Layout 12TFull adder

CONCLUSION:

From the above results it can be concluded that our proposed full adder has got better performance in delay, power and area consideration in comparison with conventional full adder.

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It shows that in contrast to other conventional techniques, this approach is better and it will be more appropriate for industrial practice in complex process technologies.

REFERENCES:

[1]Jaume Segura, Charles F. Hawkins CMOS electronics: how it works, how it fails, Wiley-IEEE, 2004, page 132.

[2]Clive Maxfield Bebop to the Boolean boogie: an unconventional guide to electronics Newnes, 2008, pp. 423-426.

[3]Albert Raj/Latha VLSI Design PHI Learning Pvt. Ltd. pp. 150-153.

[4]Yano, K, et al, "A 3.8 ns CMOS 16*16b multiplier using complementary pass transistor logic", IEEE J. Solid State Circuits, Vol 25, p388-395, April 1990.

[5]Yingtao Jiang, Abdulkarim Al-Sheraidah, Yuke Wang, Edwin Sha, and Jin-Gyun Chung, "A Novel Multiplexer-Based Low-Power Full Adder" IEEE Transaction on circuits and systems-II: Express Brief, Vol. 51, No. 7,p-345, July- 2004.

[6]Makoto Suzuki, et al, "A 1.5 ns 32 b CMOS ALU in double pass transistor logic", ISSCC Dig. Tech. Papers, pp 90-91, February 1993.

[7]N. Ohkubo, et al, "A 4.4 ns CMOS 54X54 b multiplier using pass transistor multiplexer", Proceedings of the IEEE 1994 Custom Integrated Circuit Conference, May 1-4 1994, p599-602, San Diego, California.

[8]Mohamed W. Allam, "New Methodologies for Low-Power High Performance Digital VLSI Design", PhD. Thesis, University of Waterloo, Ontario, Canada, 2000.

[9]A.Bazzazi and B. Eskafi, "Design and Implementation of Full Adder Cell with the GDI Technique Based on 0.18µm CMOS Technology", International MultiConference of Engineers and Computer Scientists (IMES) Vol II, March 17 - 19, 2010, Hong Kong.

[10]ArkadiyMorgenshtein, Alexander Fish, and Israel A. Wagner, "Gate Diffusion Input (GDI): A Power-Efficient Method for Digital Combinatorial Circuits", IEEE Transaction on VLSI Systems, Vol. 10.

[11]Dan Wang. "Novel low power full adder cells in 180nm CMOS technology", 2009 4th IEEE Conference on Industrial Electronics and Applications, 05/2009.

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