ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Performance Analysis of Low Power CSVCO for PLL Architecture

D.Rajiv Roy
Department of Electronics & Communication Engineering
Sanketika Vidya Parishad Engineering College,
Visakhapatnam - 530041, A.P, India.

Dr.Nihar Ranjan Panda
Department of Electronics & Communication Engineering
Sanketika Vidya Parishad Engineering College,
Visakhapatnam - 530041, A.P, India.

Manas Ranjan Biswal
Department of Electronics & Communication Engineering
Sanketika Vidya Parishad Engineering College,
Visakhapatnam - 530041, A.P, India.

Abstract

This paper describes the performance analysis of an ultra low power, low phase noise current starved CMOS VCOfor PLL architecture. This CSVCO is applicable for PLL application such as in, frequency control, frequency multipliers, tracking generators, clock generation and recovery etc. Transient response and phase noise analysis of CSVCO is performed and after simulation the phase noise at 1MHz is -104.0dBc/Hz with supply voltage of 1 V with a centre frequency of 2GHz. It is performed using cadence virtuoso gpdk045 nm CMOS technology.

*Keywords—**Current Starved Voltage Control Oscillator (CSVCO); Complementary Metal Oxide Semiconductor Field Effect Transistor (CMOS) ;low phase noise;ultra lowpower;phase locked loop (PLL).***

Introduction

Phase locked loop (PLL) is the heart of the many modern electronics as well as communication system. Recently plenty of the researches have conducted on the design of phase locked loop (PLL) [7] circuit and still research is going on this topic. Most of the researches have conducted to realize a higher lock range PLL with lesser lock time and have tolerable phase noise. The most versatile application of the phase locked loops (PLL) is for clock generation and clock recovery in microprocessor, networking, communication systems, and frequency synthesizers. Phase locked-loops (PLLs) are commonly used to generate well-timed on-chip clocks in high-performance digital systems. Modern wireless communication systems employ Phase Locked Loop (PLL) mainly for synchronization, clock synthesis, skew and jitter reduction. Phase locked loops find wide application in several modern applications mostly in advance communication and instrumentation systems. PLL being a mixed signal circuit involves design challenge at high frequency.

PHASE LOCKED LOOP ARCHITECTURE:

A phased locked loop is a feedback system that compares the output phase with the input phase voltage controlled oscillator (VCO) worked as the heart of phase locked loop. A novel IDEA based multi-objective fast design methodology is proposed. In order to reduce the power consumption the staking VCO and tripler with current reuse technique is used. Depending on the application, most of the cases the betterment of the power and size is very critical issue. A LC VCO has higher phase noise, less tuning range and consume larger area VCO plays a critical role in wireless applications it provide periodic signals required for timing in digital circuits. A PLL consists of a Phase Frequency Detector (PFD), Charge pump Low pass Filter (LPF), Current starved voltage controlled oscillator (VCO), and Divider circuits [1-5].

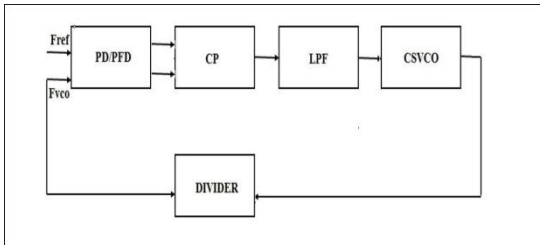


FIGURE: BLOCK DIAGRAM OF PLL

Cite this article as: D.Rajiv Roy, Dr.Nihar Ranjan Panda & Manas Ranjan Biswal, "Performance Analysis of Low Power CSVCO for PLL Architecture", International Journal & Magazine of Engineering, Technology, Management and Research, Volume 4 Issue 11, 2017, Page 248-256.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

The phase detector compares the phase of the output signal to the phase of the reference signal and it produces an output voltage which is proportional to the phase error of the two signals. And output of the phase detector passed through charge pump circuits which convert the logic states of the phase frequency detector into analog signals suitable to control the voltage-controlled oscillator (VCO) [2], then the signal feedback to the VCO which take the control voltage as an input and produces a output voltage. A divider circuit is used in feedback path of the circuit which is used provide the feedback path in the PLL. It takes the output of VCO as an input frequency Fin and produced an output signal of a frequency Fout.

COMPONENTS AND THEIR WORKING:

The PLL consists of phase frequency detector, charge pump, low pass filter and VCO. The following describes the brief explanation of each block.

PHASE FREQUENCY DETECTOR:

Phase frequency detector is a circuit which has two inputs, which can detect both the frequency and phase differences and its output is feedback to the charge pump. When the reference frequency (Fref) and VCO frequency (Fvco) inputs are unequal in frequency and/or phase, the differential UP (Up) and DOWN (Dn) outputs [3] will provide pulse streams. Its subtraction and integration provide an error voltage for control of a VCO.

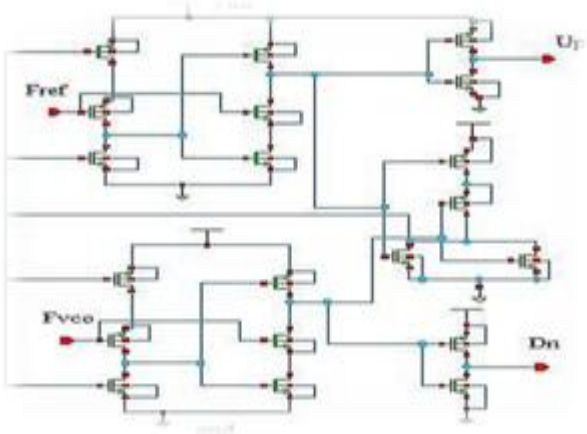


Fig.2 Phase frequency detector

CHARGE PUMP:

Charge pump is the next block to the phase frequency detector. The output signal is generated by the PFD is directly feedback to the charge pump. The main purpose of a charge pump is to convert the output signal of the phase frequency detector into analog signals suitable to control the voltage controlled oscillator (VCO). Basically, the charge pump consists with current sources and up & down signals. The output of the charge pump is connected to the VCO that integrates the charge pump output current to an equivalent VCO control voltage (Vctrl) [4]. Charge pump circuit converts the phase or frequency difference information into a voltage, used to tune the VCO.

When the reference signal clock edge leads the feedback clock edge, the UP signal of the PFD goes high. So to make both the clock have rising edge at the same time the VCO output signal frequency has to be increased. For this purpose an increase in control voltage is needed from the output of charge pump and loop filter circuit.

The simulation result which is shown in the Figure below gives an increase in the control voltage at the output of the loop filter circuit. From the Figure it's clear that the control voltage increases for a period during which the UP signal of the PFD remains high. In the other case a decrease in the control voltage is produced at the output of the filter circuit which is shown in the Figure. When the rising of feedback signal leads the reference signal rising edge the control voltage decreases for the period during which the DOWN signal of the PFD remains high [5].

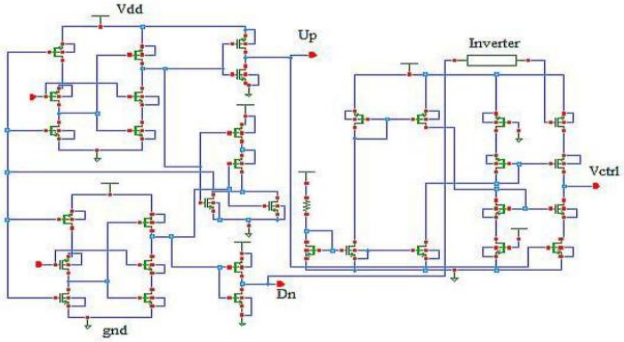


Fig.3 PFD with charge Pump Circuit

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

LOW PASS FILTER:

A low pass filter is next to the charge pump in the PLL circuits which work is to passes the low frequency signal but attenuates the frequency which is higher than cutoff frequency. LPF is used in PLL to get rid of the high frequency components in the output of the phase detector. It also removes high frequency noise. All these features make LPF a critical part in PLL and helps to control the dynamic characters of the whole circuit. The LPF helps in keeping the VCO from hunting. The filter supplies the control voltage to the VCO.

VOLTAGE CONTROLLED OSCILLATOR:

In the block of phase locked loop circuits VCO works as the heart of the circuits. The schematic diagram of Voltage Controlled Oscillator is shown in Fig. 11. The circuit associated with two parts, current starving circuits and the inverter stages. The design objective of this article is to minimize phase noise and power of the VCO with a desired frequency of oscillation, subject to the physical compulsion [6-8].

This circuit function is similar to ring oscillator, here five stage ring oscillator is used and a control voltage (Vctrl) is inputted with a supply voltage of 1 V applied in the circuits limit the current available to the inverter circuits. In other words, the inverter is starved for current. It can be made to oscillate from few hertz to hundreds of GHz. It can make in oscillating frequency in response to change in control voltages (Vctrl). The oscillation frequency of Voltage Controlled Oscillator for 'N' is represented as

$$f = \frac{1}{2N\Gamma}$$

Where f is frequency of oscillation of VCO and N is the number of stages

$$\Gamma = t_1 + t_2$$

To determine the total capacitance of VCO is represented as

$$C_{tot} = C_{out} + C_{in}$$

$$C_{tot} = C_{ox}(W_p L_p + W_n L_n) + \frac{3}{2} C_{ox}(W_p L_p + W_n L_n)$$

$$C_{total} = \frac{5.C_{ox}(W_p L_p + W_n L_n)}{2}$$

Where *Cox*is the oxide capacitance and *p W* &*n W* are the Width of PMOS and NMOS respectively, *p L* &*n L* are the length of PMOS and NMOS respectively.

The operation of Voltage Controlled Oscillator is similar to the ring oscillator. Middle PMOS M1 and NMOS M2 operate as inverter, while upper PMOS M13 and lower NMOS M14 operate as current sources. The current sources limit the current available to the inverter. In other words, the inverter is starved for current. The current in the first NMOS and PMOS are mirrored in each inverter/current source stage. PMOS M11 and NMOS M11 drain currents are the same and are set by the input control voltage. The operation of Voltage Controlled Oscillator is similar to the ring oscillator.

The purpose of VCO is to either speed up or slow down the feedback signal according to the error generated by the PFD. Added benefit of this VCO is to maintain a constant amplitude level and oscillation. This circuit has higher tuning range and low power consumption for various application domains [7-11].

Voltage Controlled Oscillator (VCO)

Voltage-controlled oscillator generates frequency controlled by input voltage.

The dc level output of a low-pass filter is applied as control signal to the voltage-controlled oscil-lator (VCO).

The VCO frequency is adjusted till it becomes equal to the frequency of the input signal.

During this adjustment, PLL goes through three stages-free running, capture and phase lock.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

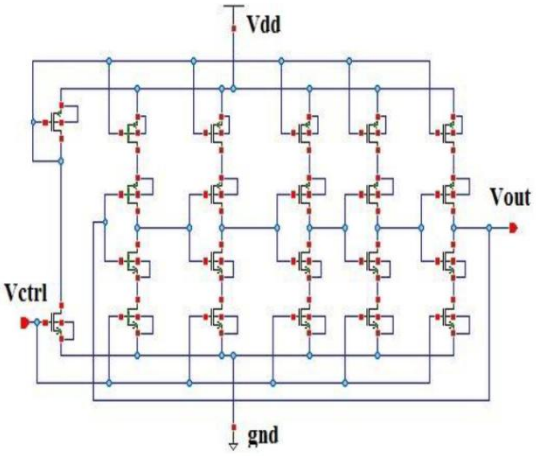


Fig.2.4 Schematic diagram of current starved VCO

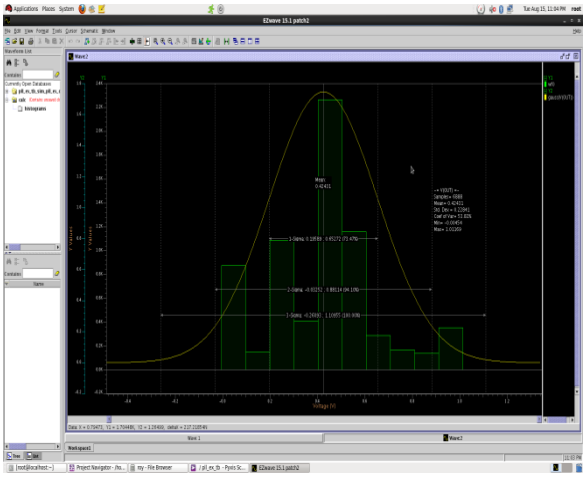


Fig: output waveforms of phase and magnitude

SIMULATION AND RESULTS

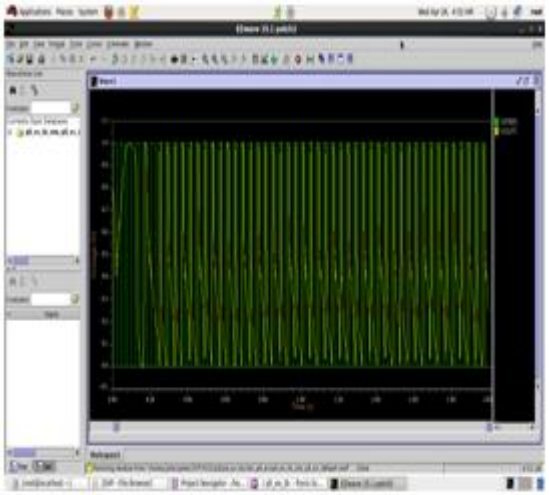


Fig: output waveforms of PLL

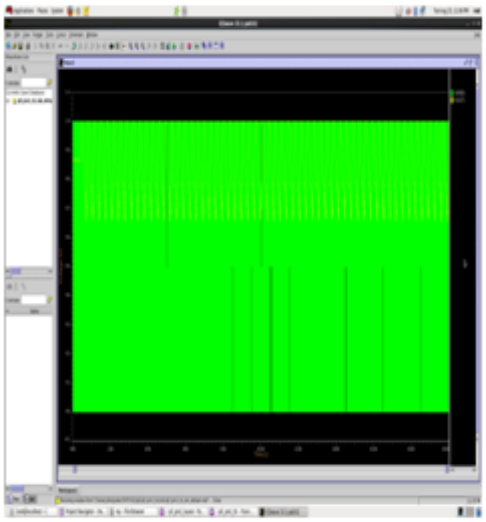


Fig: output waveforms of PLL

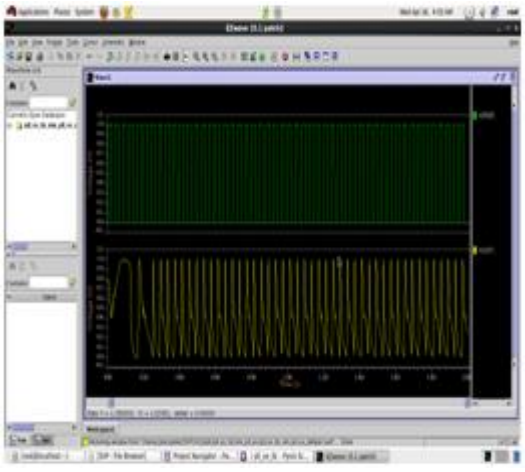


Fig: output waveforms of PLL

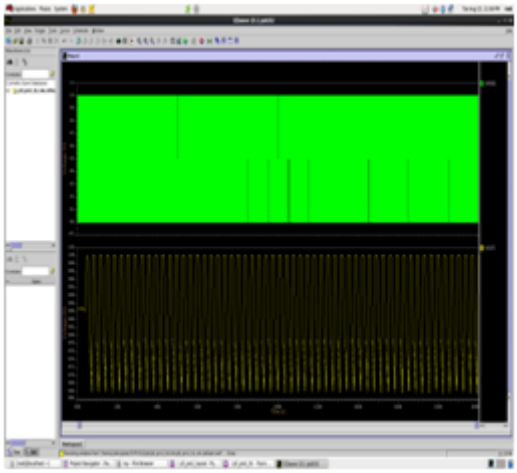


Fig: output waveforms of PLL

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

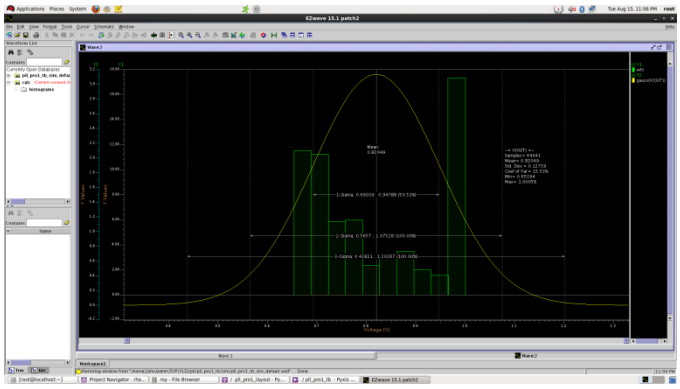


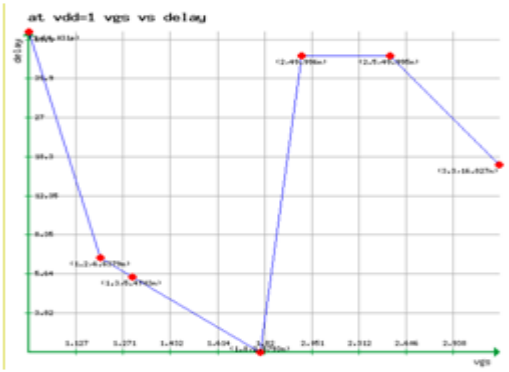
Fig: output waveforms of phase and magnitude

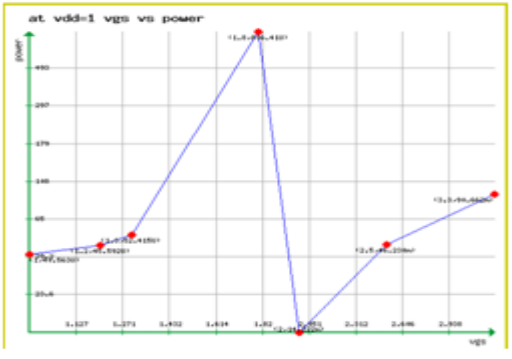
POWER ANALYSIS OF PLL :

TABLE NO 1: AT VDD=1 VGS VS POWER & VGS VS DELAY

VDD	VGS	POWER	DELAY
1	1	40.563UW	64.031PS
1	1.2	45.592UW	6.6379NS
1	1.3	52.415UW	5.4703NS
1	1.8	806.41UW	2.5793NS
1	2.0	14.222MW	49.996NS
1	2.5	46.230MW	49.995NS
1	3.3	90.662MW	16.827NS

AT VDD=1 VGS VS POWER

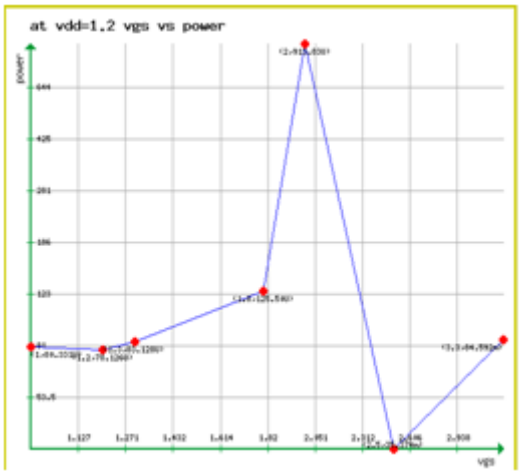




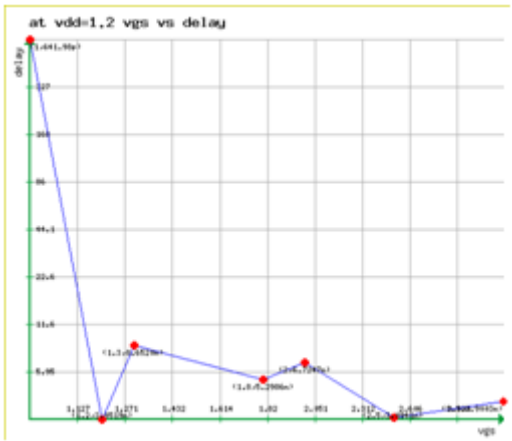
AT VDD=1 VGS VS DELAY

TABLE NO 2: AT VDD=1.2 VGS VS POWER & VGS VS DELAY

VDD	VGS	POWER	DELAY
1.2	1	80.331UW	641.98PS
1.2	1.2	78.126UW	3.0519NS
1.2	1.3	83.128UW	8.8520NS
1.2	1.8	125.50UW	5.2986NS
1.2	2.0	913.83UW	6.7247NS
1.2	2.5	35.374MW	3.0941NS
1.2	3.3	84.592MW	3.9003NS



AT VDD=1.2 VGS VS POWER

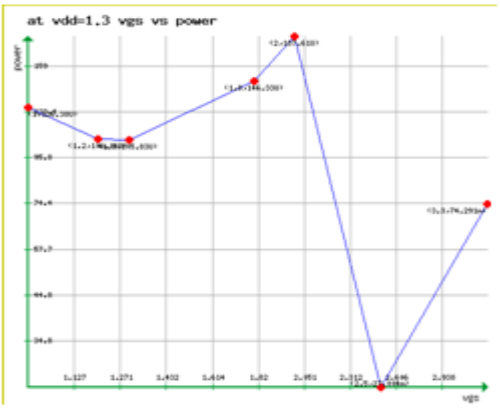


AT VDD=1.2 VGS VS DELAY

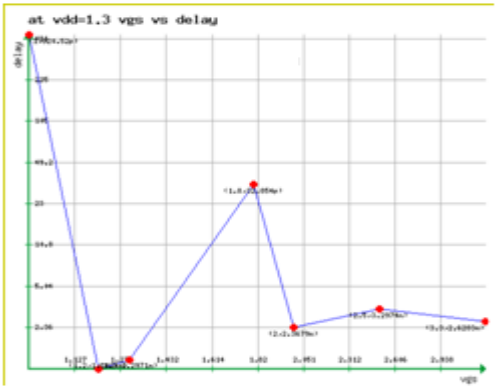
TABLE NO 3: AT VDD=1.3 VGS VS POWER & VGS VS DELAY

VDD	VGS	POWER	DELAY
1.3	1	126.38UW	520.52PS
1.3	1.2	106.06UW	1.1024NS
1.3	1.3	105.83UW	1.2971NS
1.3	1.8	146.33UW	32.854PS
1.3	2.0	187.61UW	2.3679NS
1.3	2.5	27.004MW	3.2974NS
1.3	3.3	74.291MW	2.6283NS

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal



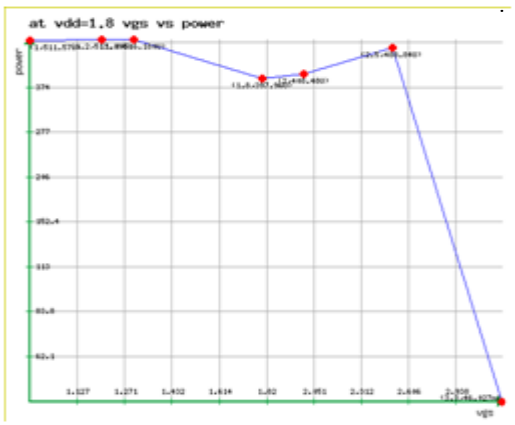
AT VDD=1.3 VGS VS POWER



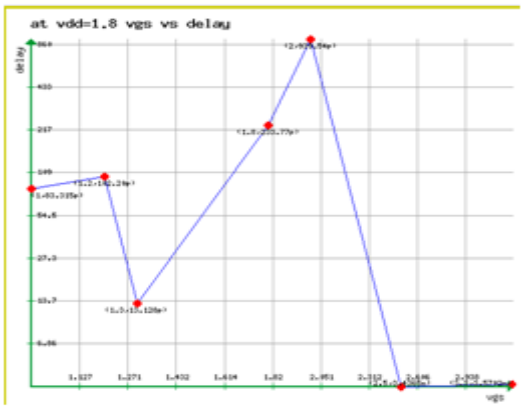
AT VDD=1.3 VGS VS DELAY

TABLE NO 4: AT VDD=1.8 VGS VS POWER & VGS S DELAY

TABLE NO 4: AT VDD=1.8 VGS VS POWER & VGS S DELAY			
VDD	VGS	POWER	DELAY
1.8	1	511.57UW	83.315PS
1.8	1.2	513.09UW	102.20PS
1.8	1.3	516.180UW	13.128PS
1.8	1.8	397.96UW	233.77PS
1.8	2.0	408.48UW	939.54PS
1.8	2.5	488.84UW	3.4365NS
1.8	3.3	46.027MW	3.5702NS



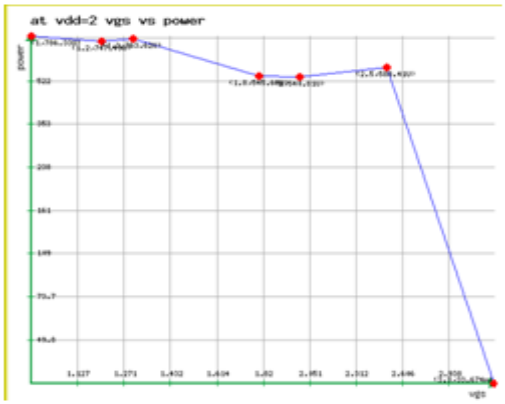
AT VDD=1.8 VGS VS POWER



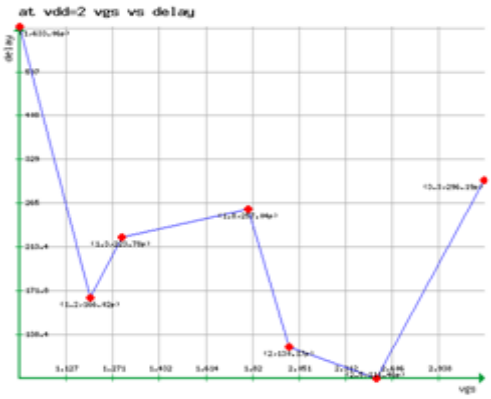
AT VDD=1.8 VGS VS DELAY

TABLE NO 5: AT VDD=2.0 VGS VS POWER &VGS VS DELAY

VDD	VGS	POWER	DELAY
2.0	1	786.33UW	633.06PS
2.0	1.2	747.49UW	166.02PS
2.0	1.3	763.62UW	223.78PS
2.0	1.8	545.69UW	257.04PS
2.0	2.0	540.81UW	130.17PS
2.0	2.5	588.41UW	111.46PS
2.0	3.3	33.674MW	296.19PS



AT VDD=2.0 VGS VS POWER

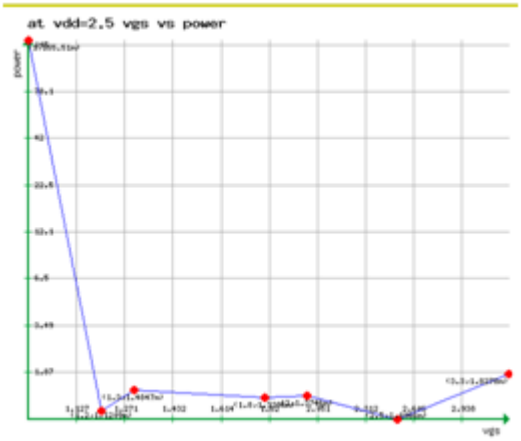


AT VDD=2.0 VGS VS DELAY

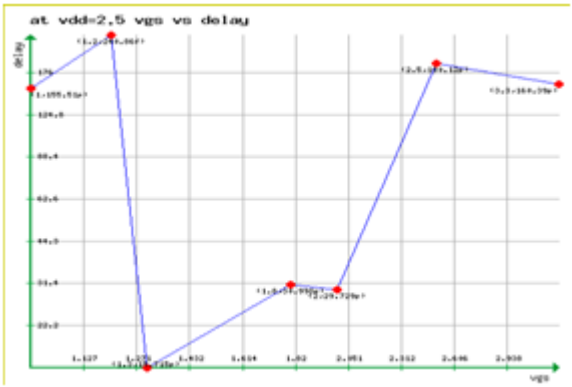
ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

TABLE NO 6: AT VDD=2.5 VGS VS POWER &VGS VS DELAY

VDD	VGS	POWER	DELAY
2.5	1	1.3020MW	155.51PS
2.5	1.2	1.1209MW	240.86FS
2.5	1.3	1.4847MW	15.715PS
2.5	1.8	1.3396MW	30.998PS
2.5	2.0	1.3746MW	29.729PS
2.5	2.5	1.0066MW	190.12PS
2.5	3.3	1.8278MW	160.39PS



AT VDD=2.5 VGS VS POWER

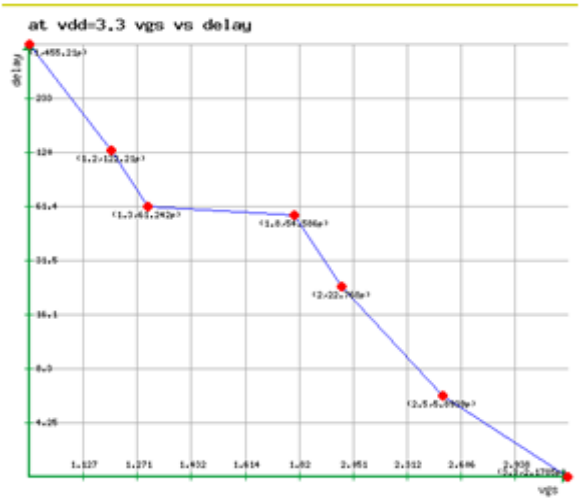


AT VDD=2.5 VGS VS DELAY

TABLE NO 7: AT VDD=3.3 VGS VS POWER & VGS VS DELAY

VDD	VGS	POWER	DELAY
3.3	1	2.5218MW	455.21PS
3.3	1.2	3.1654MW	122.21FS
3.3	1.3	3.5188MW	61.242PS
3.3	1.8	3.1604MW	54.586PS
3.3	2.0	2.6585MW	22.768PS
3.3	2.5	2.8965MW	5.8939PS
3.3	3.3	2.0840MW	2.1785PS

AT VDD=3.3 VGS VS POWER



AT VDD=3.3 VGS VS DELAY

CONCLUSION:

Phase-locked loops play a vital part in many modern-day circuits. They are used to demodulate amplitude and frequency modulated signals, synchronize clocks, recover small signals from noise, and they are used in devices such as dual-tone multiple frequency decoders and modems. Overall, designing a PLL gave us a great opportunity to go through the entire design process of VLSI technology. By researching, designing, and testing the PLL we were able to review and expand on many different topics that have been learned throughout our college career. Since PLL design requires knowledge of communications, this project served as a perfect means to exercise this knowledge in a “real world” application.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

FUTURE WORK:

1. The design can be upgraded to reduce area and power and to provide better stability.
2. In future direction, the data transfer may be up scaled to higher rates and high operating frequencies.
3. In the design of loop filter, capacitors and resistors were used. Instead, they can be replaced by MOS transistors, so that the designed circuit is more practical in nature
4. The lock time of the PLL mainly depends upon the type of PFD architecture used and the parameters of the charge pump and loop filter. So by properly choosing the PFD architecture and adjusting the charge pump current and the loop filter component values a better lock time can be achieved
5. The Centre frequency of oscillation of the VCO depends upon the sizing of the transistors. The frequency deviation from the desired value can be reduced by properly choosing the transistor sizes.

REFERENCES:

[1]. S. C. Gupta, "Phase-locked loops", Proc. IEEE, vol. 63, no. 2, pp. 291-306, Feb. 1975.

[2]. Yinqing et.al ,1991 Zhou Yinqing Li Jing wen Su Jie , Nonlinear analysis of phase lock loop in co-communication system , China 1991 International Conference on Circuits and Systems, June 1991, Shenzhen, China .

[3]. HC Yang, LK Lee, RS Co - IEEE Journal of Solid-State Circuits, 1997

[4]. Gonzalez et.al, 1997 Ricardo Gonzalez, Benjamin M. Gordon, and Mark A. Horowitz, ,ieee journal of solid-state circuits, vol. 32, no. 8, august 1997.

[5]. Moon et.al,2000 YeonKug Moon, Kwang Sub Yoon, Chang Ho Han, Design of a 3.3-V 1-GHz CMOS Phase Locked Loop with a Two-Stage Self-Feedback Ring Oscillator, Journal of the Korean Physical Society, Vol. 37, No. 6, December 2000, pp. 803_807.

[6]. R.E. Best, "Phase Locked Loops Design, Simulation and Applications," McGraw-Hill Publication, 5th edition 2003

[7]. Dan H. Wolver, "Phase Locked Loop Circuit Design," Prentice Hall Publication, 1991.

[8]. R.J.Baker, H.W.Li, and D.E.Boyce, "CMOS Circuit Design, Layout, and Simulation," IEEE Press series on Microelectronic Systems, 2002

[9]. S. M. Shahruz, "Novel phase-locked loops with enhanced locking capabilities," Journal of Sound and Vibration, Vol. 241, Issue 3, 29 March 2001, Pages 513-523.

[10]. B. Razavi, "Design of Analog CMOS Integrated Circuits," Tata McGraw Hill Edition,2002

[11]. M.Mansuri, D.Liu, and C.K.Yang, "Fast Frequency Acquisition Phase Frequency Detector for G Samples/s Phase Locked Loops," IEEE Journal of Solid State Circuit, Vol. 37,No.10, Oct., 2002.

Author Details

D.Rajiv Roy, Purusing Master's in VLSI Design from sanketikavidyaparishad college of engineering affiliated to Andhra University, Vishakapatnam Andhra Pradesh

Dr.Nihar Ranjan Panda is currently working as an Head of the Department of Electronics and

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

communication engineering in sanketikavidyaparishad college of engineering affiliated to Andhra University, Vishakapatnam,Andhra Pradesh. Master's in JRN University, Rajasthan, and Phd in KI University, Southkorea.

Mr.Manas Ranjan Biswal is currently working as an assistant professor in Department of Electronics and communication engineering in sanketikavidyaparishad college of engineering affiliated to Andhra University, Vishakapatnam,Andhra Pradesh. Master's in Communication Engineering from BijuPatnaik University Of Technology. Odissa.