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A Novel Method for Interconnection of Bipolar HVDC Networks Using Multilevel DC/DC Converter (DC-MMC)

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ABSTRACT

This project introduces a modular multilevel dc/dc converter, termed the DC-MMC that can be deployed to interconnect HVDC networks of different or similar voltage levels. Its key features include: 1) bidirectional power flow; 2) step-up and step-down operation; and 3) bidirectional fault blocking similar to a dc circuit breaker. The kernel of the DC-MMC is a new class of bidirectional single-stage dc/dc converters utilizing interleaved strings of cascaded sub modules. The DC-MMC operation is analyzed and an open loop voltage control strategy that ensures power balance of each sub module capacitor via circulating ac currents is proposed. Simulations performed in PLECS validate the DC-MMC's principle of operation and the proposed control strategy.

Index Terms—Converters, ANN, dc-dc power conversion, HVDC converters, multilevel systems.

INTRODUCTION

The dc/ac modular multilevel converter (MMC) has gained widespread popularity due to its many operational advantages for high voltage and high power applications. DC transmission is rapidly becoming a preferred choice for the large-scale integration of renewable energy sources. A new class of modular multilevel bidirectional dc/dc converters based on the MMC concept have recently been proposed. These converters, termed the DC-MMC, are able to achieve single-stage dc/dc conversion using series cascaded SMs. Most notably, its potential benefits for grid connection of offshore wind farms are widely recognized. Due to this changing electrical landscape, the development of dc grids for the collection and distribution of energy from renewable sources is gaining traction.

This paper proposes a modular multilevel dc/dc converter, termed the DC-MMC [1-4], that has the capability to interconnect HVDC networks [2] of either different or similar voltage levels while simultaneously offering the promise of bidirectional fault blocking. The DC-MMC uses multiple interleaved strings of cascaded SMs to perform single-stage bidirectional dc/dc conversion, and is capable of both step-down and step-up operation. Elimination of the traditional intermediate ac link is achieved by exploiting circulating ac currents to maintain power balance of each SM capacitor.

The use of two cascaded dc/ac stages is costly and hinders overall conversion efficiency while transformer less dc/dc converters are typically not fully modular and can suffer from uncontrolled propagation of fault currents [6] due to external dc faults. Due to its modular structure and many operational advantages, the well-known modular multilevel converter (MMC) has become a preferred solution for dc/ac conversion in various power system applications.

The MMC is particularly attractive for use in HVDC transmission where its scalable architecture enables large operating voltages to be realized by simply stacking the requisite number of sub modules (SMs) in cascade. However, the main drawback of MMC-based dc/dc topologies is that they require two cascaded dc/ac

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conversion stages. This is a relatively costly solution as each dc/ac stage must process the same input power, resulting in poor utilization of total installed SM rating. Moreover, the inherent need for an intermediate ac link and transformer rated for the full input power further adversely impacts the total cost as well as overall conversion efficiency [3].

The DC-MMC also offers advanced features such as buck/boost capability and dc circuit breaker capability. Although the prospect of HVDC-based grids offers many benefits, one of the principle challenges facing their widespread deployment is the interconnection of different dc networks and management of power flows between them. To accommodate both functions, bidirectional dc/dc converters can be dispatched (although other devices tailored for power flow control exist. By using dc/dc converters to adjust line voltages, or the voltage between different network segments, the power controllability within dc grids can be extended. This new energy conversion process employs a power transfer mechanism first introduced, which bears similarity to that recently described. A significant advantage of the DC-MMC is that a single converter structure can be utilized in place of two cascaded dc/ac converters. This offers a substantial improvement in utilization of total installed SM rating, as all SMs within the DC-MMC contribute to its overall dc power transfer capability. In addition, the flexibility to interconnect HVDC networks of similar voltages, as well as the capability for bidirectional fault blocking akin to a dc circuit breaker, make the proposed DC-MMC an attractive device for deployment in future dc grids [5].

MODELING OF PROPOSED THEORY II. PROPOSED DC-MMC FOR HVDC INTERCONNECTS

Three-String Architecture

The DC-MMC performs single-stage dc/dc conversion by utilizing interleaved strings of cascaded SMs. Fig. 1(a) shows the three-string architecture of the DC-MMC for deployment in bipolar HVDC networks. Each string is comprised of two pairs of arms; each pair of arms consisting of an inner arm and an outer arm, where an arm is defined as a set of cascaded SMs.

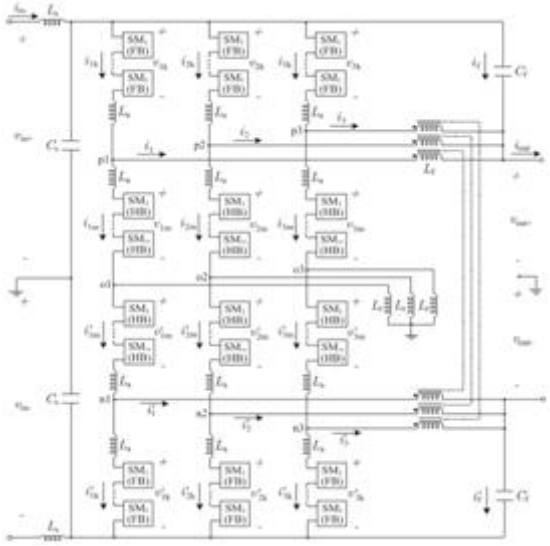

Fig. 1. Three-string DC-MMC architecture with input and output filtering: (a) circuit diagram

The arms of each string are series-stacked in symmetric relation about an associated midpoint, i.e., o1, o2, o3, with the inner arms flanked by the outer arms. Each inner arm and outer arm employs m half-bridge SMs (HB/SMs) and k full-bridge SMs (FB/SMs), respectively. Circuit configurations for the HB/SM and FB/SM switching cells are given in Fig. 1(b).

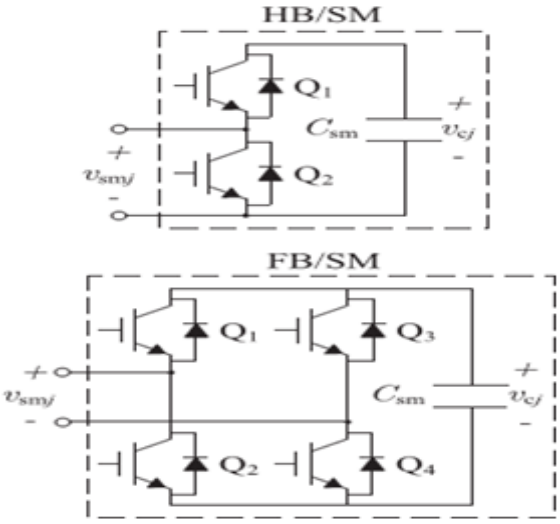

Fig. 1. Three-string DC-MMC architecture with input and output filtering: (b) switching cell configurations for j th half-bridge SM (HB/SM) and jth full-bridge SM (FB/SM).

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In comparison to the three-phase dc/ac MMC, the three-string architecture in Fig. 1 shares a similar modular structure. As will become more apparent in subsequent sections, the three-string implementation of the proposed DC-MMC may be viewed as the three-phase dc/ac MMC structure adapted for single-stage dc/dc conversion. Unlike the recently proposed dc/dc converter, which is formed by series-stacking two conventional three-phase dc/ac MMCs, the operation and control of Fig. 1 is fundamentally different from that of the dc/ac MMC [4]

Two-String Architecture

The DC-MMC in Fig. 1 utilizes three interleaved strings of cascaded SMs. By removing one of the strings, a two-string implementation is also possible as shown in Fig. 2.

This architecture is the simplest multistring implementation of the DC-MMC. In general, an arbitrary number of strings can be interleaved. Note the ability to install a coupled inductor set at each dc output pole has been exploited due to the even number of interleaved strings. Consequently, this reduces insulation requirements on the output filter inductances as compared to Fig. 1. The two-string and three-string architectures have the same fundamental principle of operation as each string employs an identical dc/dc conversion process. For equal string designs, the two-string has 2/3 the output power rating of the three-string.

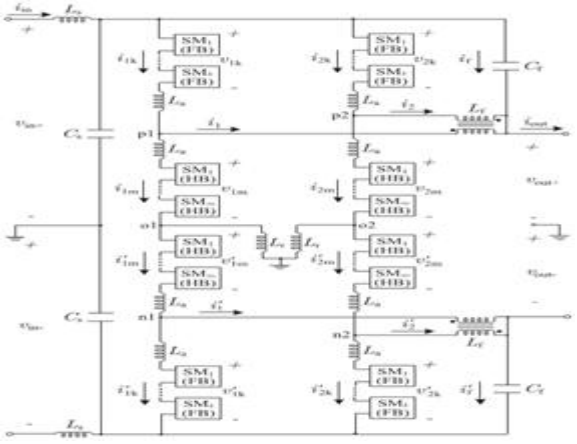

Fig. 2. Two-string DC-MMC architecture with input and output filtering.

Principle of Operation

In Figs. 1 and 2, the input network voltages vin+ and vin – can be unevenly split between the arms of each string. For example, arm voltages v1k (outer arm) and v1m (inner arm) can have unequal dc components that sum to vin+ . The same applies to v1m (inner arm) and v1k (outer arm) with vin −. Division of vin+ and vin − as described is achieved by controlling the number and polarity of SM capacitors inserted along each string via switching action, where possible switching states for the jth HB/SM and FB/SM are vsmj = {0, +vcj } and vsmj = {0, −vcj, +vcj }, respectively. The output network, represented by vout+ and vout −, is coupled across the inner arms of each string as shown. DC power transfer between networks can be reversed by changing polarity of iin. Bidirectional dc power transfer is easily accommodated as the SMs inherently permit bidirectional current flow. The arrangement of HB/SMs and FB/SMs [7] in Figs. 1 and 2 permits both step-up and step-down voltage level conversion for the DC-MMC. The voltage conversion ratio D and its complement D are defined as

$$D \triangleq \frac{v_{out+}}{v_{in+}} = \frac{v_{out-}}{v_{in-}} \quad (1)$$

$$D' \triangleq 1 - D \quad (2)$$

From (1) and (2) the operating modes of the DC- MMC are summarized:

1) Step-down operation: 0 < D < 1 and thus 0 < D < 1;

2) Step-up operation: D > 1 and thus D < 0.

For step-down operation where the voltages at nodes p1, p2,p3 (and n1, n2, n3) relative to ground always remain below vin+ (and above −vin −), By using circulating ac currents to ensure power balance for each SM capacitor the DC-MMC in Figs. 1 and 2 is able to perform single stage dc/dc conversion. The circulating currents are established by reactive elements and serve to exchange average ac power between each outer arm and the adjacent inner arm, in a near lossless manner. Average ac power exchange between arms (Pac) for SM capacitor charge balancing is indicated by the bold arrows. Link the string midpoints using capacitors; however, this is done at the expense of high- impedance grounding the

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DC-MMC structure. Based on the above discussion, the principle of operation of the two-string DC-MMC architecture is conceptualized in Fig. 3.

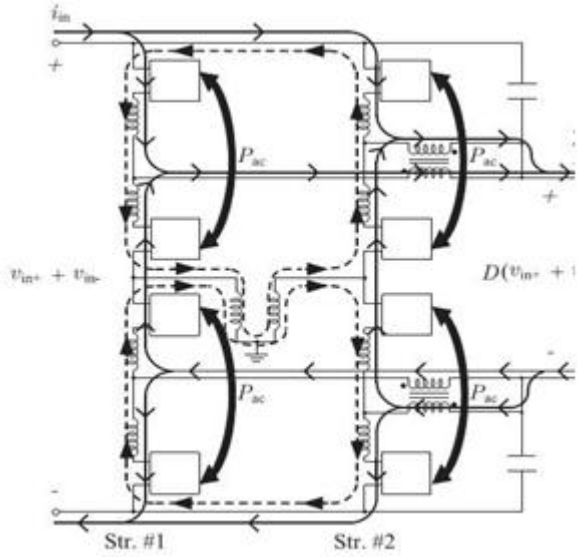

Fig. 3. Principle of operation for two-string DC- MMC architecture in Fig. 2: DC current (solid lines) and circulating ac current (dotted lines) paths are shown.

Although this balancing process will be analyzed later, a simple visual indicator of its necessity is that the dc current carried by each outer arm relative to the adjacent inner arm are of opposite directions. The requisite Pac is achieved through the interaction of the circulating ac currents and ac components of the arms voltages.

ANALYSIS OF DC-MMC OPERATION

Based on the analysis, a modulation scheme for the ac arms voltages that satisfies SM capacitor power balance for all possible operating modes is proposed. The DC-MMC operation in greater depth, by utilizing a simplified string model to study the ideal single-stage dc/dc conversion process. Unless otherwise indicated, the following assumptions are enforced: 1) each arm has a large number of SMs such that ideal sinusoidal ac voltages are synthesized;

2) ac voltages and currents are represented by their steady-state fundamental frequency components; 3) resistance terms are neglected; and 4) ac output filter currents are negligible.

Single-Stage DC/DC Conversion Process

This design flexibility is a salient feature of the DC-MMC. Depending on the specific application, a suitable modulating frequency would be selected based on a tradeoff between design constraints such as SM capacitor voltage ripple, total energy storage cost, and switching losses. To illustrate the ideal single-stage dc/dc conversion process, Fig. 4 provides a simplified model for string #1 of the DCMMC [8].

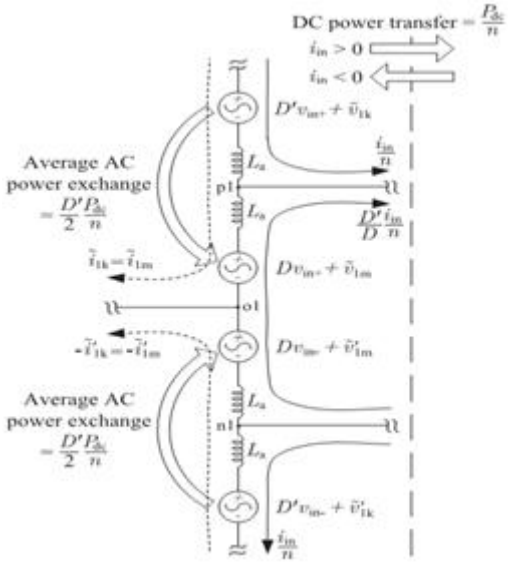

Fig. 4. Simplified model for string #1 of DC-MMC in Figs. 1 and 2, with ideal output filtering and ac filter currents neglected.

From Fig. 4, the dc current through the inner arms increases as D becomes smaller. For D < 0.5, the inner arms carry a dc current greater than |iin/n |. This operating region thus incites high conduction losses, and may necessitate additional inner arms installed in parallel. To eliminate individual chokes is possible, provided the basic requirement of an inductance in every voltage loop is not violated. To ensure steady-state power balance of each SM capacitor in string #1, the following average power constraints must be met:

$$V_{1k}.I_{1k} = -D'(v_{in+})\frac{i_{in}}{n} = -\frac{D'P_{dc}}{2n} \qquad (3)$$

$$V_{1m}.I_{1m} = D'(v_{in+})\frac{i_{in}}{n} = \frac{D'P_{dc}}{2n} \qquad (4)$$

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$$V'_{1m}.I'_{1m} = D'(v_{in-})\frac{i_{in}}{n} = \frac{D'P_{dc}}{2n} \quad (5)$$

$$V'_{1k}.I'_{1k} = -D'(v_{in-})\frac{i_{in}}{n} = -\frac{D'P_{dc}}{2n} \quad (6)$$

The direction of power exchange depends on the polarities of D (step-up/step-down) and Pdc (dc power transfer direction). For example, Fig. 4 shows the outer arms must deliver average ac power to the inner arms for: 1) D > 0, Pdc > 0; and 2) D < 0, Pdc < 0. To ensure a net ac voltage is not impressed across the input or output dc terminals, requirements are imposed on the synthesized arms voltages

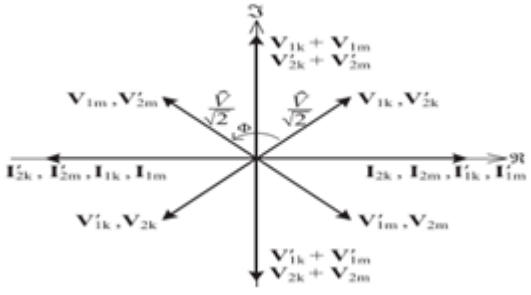
$$V_{1k} = -V'_{1k} \quad (7)$$

$$V_{1m} = -V'_{1m} \quad (8)$$

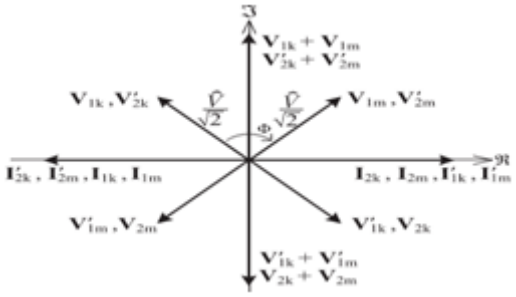
Based on the preceding discussion, the DC- MMCs in Figs. 1 and 2 internally circulate a total average ac power of |D Pdc |. Note interconnecting two HVDC networks of similar voltage levels requires only a small amount of ac power to be circulated.

Steady-State Power Balance of SM Capacitors

There are infinitely many combinations of ac arms voltages and resulting ac arms currents that can satisfy power balance constraints. The peak magnitude of the ac arms voltages is denoted by Vˆ . Φ is the phase shift between ac voltages of each outer arm and the adjacent inner arm, with positive values of Φ defined for the inner arm voltage leading the outer arm voltage. However, adopting such a strategy constrains each pair of arms to equally share the reactive power requirements of the composite load formed by Lr and La.



(a)



(b)

Fig.5.Fundamental frequency ac rms phasor diagrams that illustrate the power transfer mechanism used to achieve power balance of SM capacitors in Fig. 2, with ac output filter currents neglected, valid for: (a) D < 1, iin > 0 and D > 1, iin < 0; (b) D < 1, iin < 0 and D > 1, iin > 0.

Based on Figs. 4 and 6, the average power exchanged between each outer arm and the adjacent inner arm is

$$P_{k/m} = \frac{M\widehat{V^2}}{4X_r}\sin\phi \quad (9)$$

Where

$$X_r = \omega_m(L_r + L_a) \quad (10)$$

Positive values of Pk/m denote average ac power delivered from each outer arm to the adjacent inner arm of the same string. In general, Pk/m is adjusted by changing any combination ofM, Vˆor Φ.

Converters designed with smaller Xr offer reduced circuit var requirements and result in values of |Φ| approaching 180◦. A preferred strategy is to impose unity power factor on the outer arms while realizing near unity power factor operation for the inner arms as shown in Fig. 6. Here, M is the ratio of inner arm to outer arm ac voltage magnitudes, e.g., M= |V1m/V1k |. For a fixed V, this modulation scheme minimizes the circulating ac currents needed for the dc/dc conversion process when operating with larger values of D.

Moreover, it significantly reduces the circuit reactance required to establish the circulating ac currents [9].

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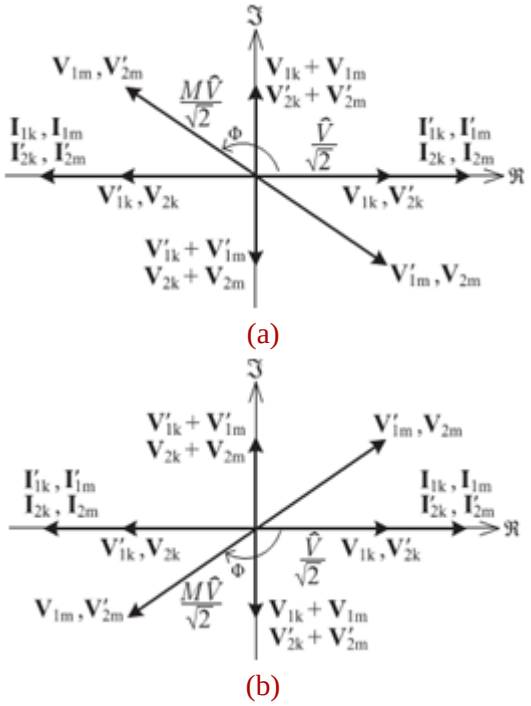

Fig. 6. Fundamental frequency ac rms phasor diagrams depicting modulation strategy to ensure power balance of SM capacitors in Fig. 2

while imposing unity power factor on outer arms and near unity power factor operation on inner arms, with ac output filter currents neglected, valid for: (a) D < 1, iin > 0 and D > 1, iin < 0; (b) D < 1, iin < 0 and D > 1, iin > 0.

Fig. 2 can be connected together and, possibly, or, if desired, solidly grounded. In this case, the arm chokes solely provide the reactance needed to setup the circulating ac currents. However, it must be stressed midpoint inductors Lr need only to carry ac currents while arm chokes La must carry both dc and ac currents. The simulations in Section V utilize a nonzero Lr. Equating (9) with the required average power exchange as dictated by (3) through (6) gives

$$\frac{M\widehat{V^2}}{4X_r}\sin\phi = \frac{D'P_{dc}}{2n} \qquad (11)$$

Power balance criteria is a primary design equation quantifying the amount of average ac power that must be exchanged between arms in steady state, as a function of the voltage conversion ratio and dc power transfer between HVDC networks. Furthermore, provides additional insight into DC-MMC operation as it relates ac and dc power transfer mechanisms. Substituting n = 2 reveals each pair of arms in Fig. 2 exchange |DPdc/4| of average ac power via circulating ac currents.

BIDIRECTIONAL DC FAULT BLOCKING CAPABILITY

In addition to enabling step-up operation and the interconnection of HVDC networks with similar voltage levels, the FB/SMs in Figs. 1 and 2 can provide bidirectional fault blocking. That is, the DC- MMC can interrupt fault currents initiated by dc faults in either the input or output side networks similar to a dc circuit breaker. This is accomplished by controlling the FB/SMs in Figs. 1 and 2 to impose the appropriate polarity of voltage [1].

OPEN LOOP VOLTAGE CONTROL AND SIMULATION RESULTS

Open loop control techniques for balancing of SM capacitor voltages within the dc/ac MMC have been discussed in several papers. One of the simplest forms of open loop control, direct modulation adopts fixed sinusoidal modulating signals for the MMC arms. Balancing of SM capacitor voltages is achieved by a sort and selection algorithm that arranges capacitors based on their voltage measurements, and inserts the appropriate one(s) at each switching instant based on arm current measurements.

Circulating AC Current Control

In general, the proposed control can be modified to split the vars generation between arms as desired. In Fig. 7, the ac component of the outer arms modulating signals are fixed for each string. In contrast, the ac component of the inner arms modulating signals are the outcome of closed-loop control action. Fig. 7 shows the proposed circulating ac current control scheme that enables open loop voltage control of the two-string DC-MMC [5]. The control structure is partitioned into four blocks for each string; inner and outer arm logic for the positive and negative poles.

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TABLE I
DC-MMC BIDIRECTIONAL FAULT BLOCKING CAPABILITY: OUTERARMSSM BLOCKING VOLTAGE REQUIREMENTS

Outer Arms SM Blocking Voltage Requirements (Normalized Relative to $v_{in+} + v_{in-}$)		
Fault Condition	**Step-Down Operation** ($D < 1$)	**Step-Up Operation** ($D > 1$)
Input Side Network Fault (Block Output Network Voltage)	D [p.u.] (FB/SMs) (Inject Negative Voltage)	D [p.u.] (FB/SMs) (Inject Negative Voltage)
Output Side Network Fault (Block Input Network Voltage)	1.0 [p.u.] (HB/SMs) (Inject Positive Voltage)	1.0 [p.u.] (HB/SMs) (Inject Positive Voltage)
Bidirectional Fault Blocking Capability	D [p.u.] (FB/SMs) + D' [p.u.] (HB/SMs) (Inject Pos./Neg. Voltages)	D [p.u.] (FB/SMs) (Inject Pos./Neg Voltages)
Example Scenario	**Step-Down Operation** ($D < 1$)	**Step-Up Operation** ($D > 1$)
$D = 0.5$	0.5 [p.u.] (FB/SMs) + 0.5 [p.u.] (HB/SMs) = 1.0 [p.u.]	——
$D = 0.8$	0.8 [p.u.] (FB/SMs) + 0.2 [p.u.] (HB/SMs) = 1.0 [p.u.]	——
$D = 1.1$	——	1.1 [p.u.] (FB/SMs)

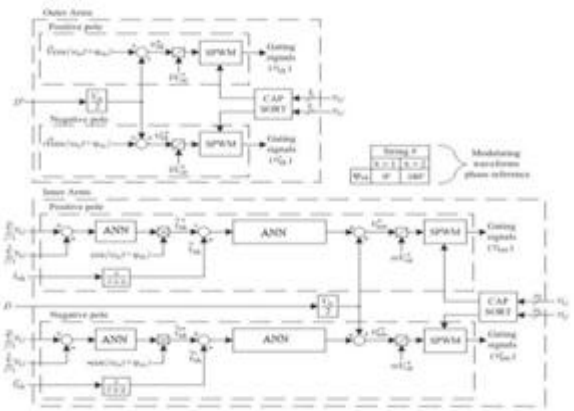

Fig. 7. Circulating ac current control for each string (i.e., x ∈ {1, 2 }) enabling open loop voltage control of the two-string DC-MMC.

Proportional-resonant compensators synthesize the inner arms ac voltages needed to drive the circulating ac currents in phase with the outer arms. AC current references for the outer arms are generated by proportional-integral (PI) compensators acting on the error between the sum of inner arm minus outer arm SM capacitor voltages. When this error deviates from zero, which signifies an imbalance in the ac power exchange between arms, the PI compensators adjust the magnitude of circulating ac currents to reestablish SM capacitor power balance. High-pass filters used in the feedback loop ensure the compensators to act only on the ac component of the outer arms.

Simulation Results

Two operating scenarios for the two-string DC-MMC are simulated in PLECS to validate the open-loop voltage control strategy proposed in Fig. 7.

TABLE II
PLECS SIMULATION PARAMETERS FOR FIG. 2 (k = m = 4)

Converter Parameters	**Value**
DC input network voltage, $v_{in+} + v_{in-}$	17.6 kV
Arm choke, L_a	2.5 mH
Midpoint string inductor, L_σ	0.5 mH
SM capacitor, C_{sm}	20 mF
Output filter rms winding voltage, $(V_t^{max})_{rms}$	2.47 kV
Output filter rms winding current, $(I_t^{max})_{rms}$	0.795 kA
Output filter magnetizing inductance, L_t	990 mH
Output filter capacitor, C_t	15 μF
Fundamental modulating frequency, f_m	50 Hz
Carrier frequency, f_c	2.5 kHz
Control Parameters	**Value**
Proportional gain, K_p^V	0.1 A/V
Proportional gain, K_p^I	2 V/A
Integral gain, K_i^V	8 A/Vs
Resonant gain, K_i^I	600 V/As
Resonant damping term, ζ	0.01
High-pass filter pole, a	15 rad/s

1) Step-Down Operation: Simulation results for D = 0.5 with dc power transfer from input to output are given in Fig. 8.

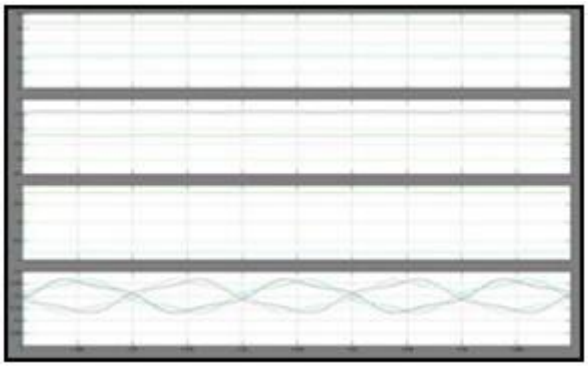

Fig. 8. Simulation results for two-string DC-MMC with D = 0.5 and iin > 0;˜V = 3.5 kV pk, Vcapn = 2.2 kV, Ls = 0 mH, Cs = 0 µF.

The second harmonic current ripple can be mitigated by increasing the energy storage capacity of the SMs (i.e., increasing Csm). For this case study, the SM capacitors are sized to achieve acceptable 100-Hz current ripple as well as tolerable capacitor voltage ripple.

2) Step-Up Operation:

Simulation results for D = 1.1 are provided in Fig. 9. The input voltage of ±8.8 kV is now stepped up to ±9.68 kV. This scenario is chosen to demonstrate the DC MMC's ability to interconnect dc networks of similar voltages by exploiting FB/SMs in the outer arms

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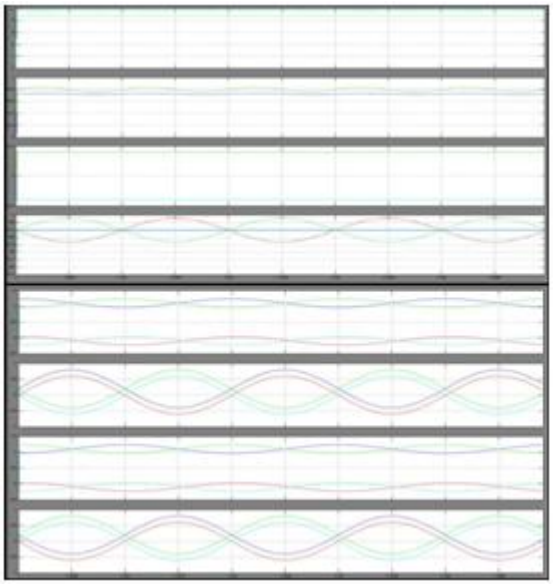

Fig. 9. Simulation results for two-string DC-MMC with D = 1.1 and iin > 0; ˆV = 1.2 kV pk, Vcapn = 2.9 kV, Ls = 0.5 mH, Cs = 40 µF.

TABLE III EXPERIMENTAL PARAMETERS FOR FIG. 10

Converter Parameters	Value
DC input network voltage, v_{in}	480 V
Arm choke, L_a	5 mH
Midpoint capacitor, $C_T/2$	5.3 mF
SM capacitor, C_{sm}	2.4 mF
Output filter rms winding voltage, $(V_f^{max})_{rms}$	66.5 V
Output filter rms winding current, $(I_f^{max})_{rms}$	16.7 A
Output filter magnetizing inductance, L_f	2210 mH
Output filter capacitor, C_f	10 μF
Fundamental modulating frequency, f_m	50 Hz
Switching frequency, f_{sw}	5 kHz
Control Parameters	**Value**
Proportional gain, K_p^v	0.2 A/V
Proportional gain, K_p^i	2 V/A
Integral gain, K_i^v	12 A/Vs
Resonant gain, K_i^i	600 V/As
Resonant damping term, ζ	0.01
High-pass filter pole, a	15 rad/s

For the step-down scenario, an input filter is not required. This is affirmed by very low switching ripple content in Fig. 8.The DC-MMC can provide bidirectional fault blocking as the outer arms have sufficient voltage to withstand the larger of the input or output dc terminal voltages.

Step-Down Operation

Fig. shows simulation results for step-down opera tion with vin = 478 V, vout = 240 V, and Pout= 4.0 kW.

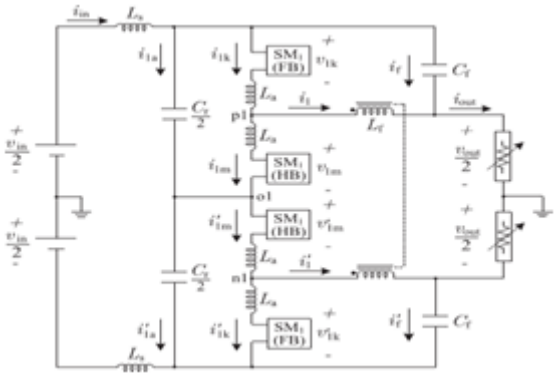

Fig. 10. Single-string implementation of DC-MMCs in Fig. 1 and Fig. 2 with k = m = 1 as basis for 4-kW: (a) circuit diagram

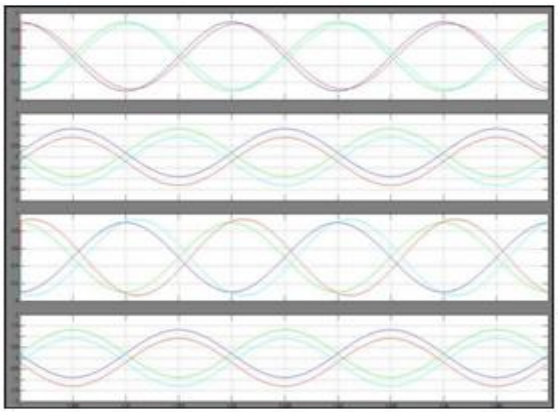

Fig. 11. Single-string architecture in Fig. 10 operating in step-down mode with vin = 478 V, vout= 240 V, Pout = 4.0 kW; waveforms recorded using Linux-based data acquisition software with fsample= 2fsw.

This shows ac currents used for SM capacitor power balancing can be confined to circulate within the converter structure despite typical load and parameter imbalances. Such validation is largely important to demonstrate the practical feasibility of the proposed energy conversion concept for the DC-MMC.

Step-Up Operation

Fig. 13 shows experimental results for step- up operation with vin = 478 V, vout = 500 V, and Pout = 4.2 kW. This simulation supplements the step- up scenario in Fig. 9, as both utilize voltage conversion ratios greater than unity. D is adjusted to achieve a voltage conversion ratio of 1.05 and nominal SM capacitor voltage of 325 V. The ac voltage Vˆ is set to achieve outer arms voltages of 35

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Vpk (uncompensated). Similar to Fig. 9, v˜1k∗ and˜i1k are in phase while v˜1m∗ lags ˜i1m by nearly 180^0.

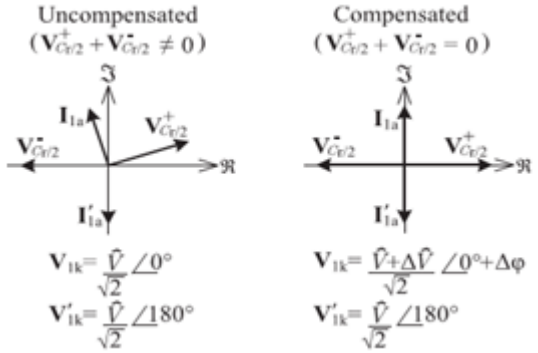

Fig. 12. Phasor diagrams illustrating adjustment to fundamental frequency component of v1k in Fig. 10 to eliminate undesired ripple in iin .

TABLE IV UNCOMPENSATED VERSUS COMPENSATED 50 HZ COMPONENT OF v1k IN FIG. 7 TO ELIMINATE 50 HZ iin RIPPLE

50 Hz component of v_{1k}		
Operating Mode	**Uncompensated**	**Compensated**
Step-down	$94.0\cos(w_m t)$	$91.4\cos(w_m t+5.3°)$
Step-up	$35.0\cos(w_m t)$	$36.3\cos(w_m t+5.5°)$

ARTIFICIAL NEURAL NETWORK

ANN is nonlinear model that is easy to use and understand compared to statistical methods. ANN is non-paramateric model while most of statistical methods are parametric model that need higher background of statistic. ANN with Back propagation (BP) learning algorithm is widely used in solving various classification and forecasting problems. Even though BP convergence is slow but it is guranteed. However, ANN is black box learning approach [7], cannot inteprete relationship between input and output and cannot deal with uncertainties. To overcome this several approches have been combined with ANN such as feature selection and etc.

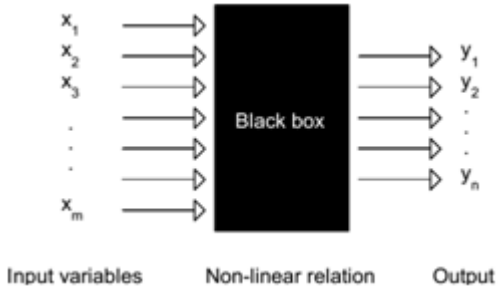

Fig13.Neural network as a black-box featuring the non-linear relationship between the multivariate input variables and multi-variate responses Neural networks (also referred to as connectionist systems) are a computational approach, which is based on a large collection of neural units (AKA artificial neurons), loosely modeling the way a biological brain solves problems with large clusters of biological neurons connected by axons. Each neural unit is connected with many others, and links can be enforcing or inhibitory in their effect on the activation state of connected neural units. Each individual neural unit may have a summation function which combines the values of all its inputs together.

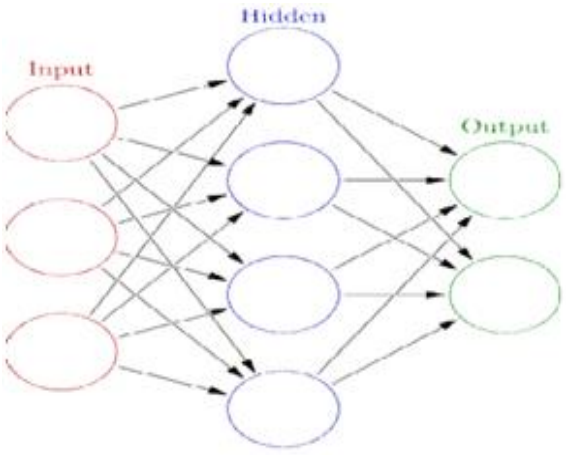

Fig 14.An artificial neural network is an interconnected group of nodes,

The goal of the neural network is to solve problems in the same way that the human brain would, although several neural networks are more abstract. Modern neural network projects typically work with a few thousand to a few million neural units and millions of connections, which is still several orders of magnitude less complex than the human brain and closer to the computing power of a worm

Applications

1. Multi level inverters are applied to transmission & distribution systems.
2. Multi level inverters are applied to STATCOM to improve stability.

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CONCLUSION

The DC-MMC is a new class of modular multilevel dc/dc converters well suited for HVDC system using ann is proposed in this paper . This paper presents the first dynamic model for the DC- MMC. The proposed state-space model is validated by comparing with simulation results for a comprehensive switched model. A new modular multilevel dc/dc converter, termed the DC MMC, is presented for the interconnection of bipolar HVDC networks. The main advantages of using Artificial Neural Networks (ANN) include: it can handle large amount of data sets; it has the ability to implicitly detect complex nonlinear relationships between dependent and independent variables; it has ability to detect all possible interactions between predictor variables; etc. The proposed state-space model is validated by comparing with simulation results for a comprehensive switched model. The DC-MMC features a new class of bidirectional single-stage dc/dc converters utilizing interleaved strings of cascaded SMs. By employing a unique arrangement of HB/SMs and FB/SMs for each string, the DC MMC can provide both step-up and step-down operations and interconnect HVDC networks of similar voltage levels. To ensure capacitor voltages are regulated to their nominal values the DC-MMC needs some form of regulation for the ac average power exchange between converter arms. This regulation is achieved via closed loop control of the internally circulating ac currents. A simplified model of the converter strings is presented and the ideal dc/dc conversion process is analyzed in this paper. An open loop voltage control scheme is proposed for the single string and two-string architectures that adopts closed-loop ac current control to maintain power balance of the SM capacitors. To ensure capacitor voltages are regulated to their nominal values the DC-MMC needs some form of regulation for the ac average power exchange between converter arms. To compensate for load and parameter imbalances the simulation results validate the proposed method. The proposed scheme has the benefits of minimizing the circulating ac currents needed for the dc/dc conversion process while significantly reducing the installed circuit reactances

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