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PNS-FCR: Flexible Charge Recycling Dynamic Circuit Technique for Low- Power Microprocessors

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Abstract

Due to the superior speed and area characteristics, dynamic circuits are widely applied in data paths and other time critical components in modern microprocessors. The high switching activity of dynamic circuits, however, consumes significant power. In this paper, a p-type/n-type dynamic circuit selection (PNS) algorithm and a flexible charge recycling (FCR) design methodology are proposed to achieve high power efficiency in data paths. The effects of technology scaling, data path width, design complexity, clock skew, and environmental conditions are discussed. Simulation results show that the power consumption of an arithmetic and logic unit (ALU) with the proposed PNS-FCR can be reduced by up to 60% as compared with a conventional ALU. An 8-bit ALU test circuit has also been manufactured based on a 0.35-μm Global Foundries technology, demonstrating the power and area efficiency of the proposed methodology.

Index Terms—Application conditions, charge recycling, low power, n-type dynamic circuit, p-type dynamic circuit, technology scaling.

INTRODUCTION

Over the past four decades, the number of transistors in a chip has grown continuously. With an increasing transistor density, the power consumption of microprocessors has become a major design issue for a wide range of applications, from ultralow power medical sensors to high performance microprocessors in leading servers.

As a fundamental part of modern microprocessors, data paths perform computing operations, typically along the critical path. The operating speed of the data paths usually determines the achievable operating frequency of the entire microprocessor.

At the same time, the data path is one of the most active components and consumes a significant share of the total power consumption. This situation is further exacerbated for those applications with an intensive computation, such as digital signal microprocessors and multimedia processors with multiple cores. Hence, it is vital to achieve low power data paths in modern microprocessors.

Due to the superior speed and area characteristics, dynamic circuits are widely applied in data paths and other time critical paths. For example, in the 32-nm Intel Itanium microprocessor, code named Poulson, and the 32-nm AMD microprocessor, code named Bulldozer, the on-chip memory and arithmetic and logic unit (ALU) adopt n-type dynamic circuits to minimize latency [1].

Existing Method:

Due to the superior speed and area characteristics, dynamic circuits are widely applied in data paths and other time critical paths. Intel Itanium microprocessor, code named Paulson, and the32-nm AMD

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microprocessor, code named Bulldozer, theon-chip memory and arithmetic and logic unit (ALU) adoptn-type dynamic circuits to minimize latency [2]. However, since the dynamic circuits are usually cascaded to form domino CMOS logic, each stage of dynamic logic requires astatic CMOS inverter to ensure that all inputs to each stageare maintained low during the precharge phase.

This property makes synthesizing dynamic circuits with Computer Aided Design (CAD) tools more difficult than synthesizing static CMOS circuits. In addition, the varying characteristics of different types of dynamic circuits (n-type and p-type)increase the design complexity of a data path. Unfortunately, the existing solutions are not sufficient to solve these issues.

Proposed Method:

In this paper, a novel p-type/n-type dynamic circuit selection (PNS) algorithm and a flexible charge recycling (FCR) design methodology are proposed, referred to here as PNS-FCR [3], which targets low power data paths in modern microprocessors. The primary contributions of this paper are as follows.

1) PNS algorithm is presented to provide charge recycling and explore power saving opportunities for specific applications.

2) A design flow to achieve power efficient data paths is presented.

3) An analysis of power efficiency of the PNS-FCR is provided and an analytical model is described for estimating the power savings of PNS-FCR.

4) A comprehensive suite of simulations is discussed, evaluating the effects of technology scaling, data path width, design complexity, clock skew and environmental conditions. These simulations demonstrate that PNS-FCR provides low design complexity, good design flexibility, and significant power savings, while achieving the targeted performance objectives of different applications.

DRC, LVS, PEX VERIFICATION

Physical Verification Of A Invertor Layout:

DRC

Once complete the full layout must conform to a complex set of design rules, in order to ensure a lower probability of fabrication defects. A tool built into the caliber called run DRC is used to detect any design rule violations during. If any errors is existing in the design deleted error markers and the corresponding rules is also displayed in a separate window. the designer must see the DRC and make sure that all layout errors are eventually removed from the mask layout before the final design is saved

The final DRC screen should look like this:

- Now verify the layout by running DRC we will run caliber interactive. In the pyxis layout window, select Tools_Calibre_Run DRC.
- Make sure the tabs named rules, inputs, outputs, run control should be green in color which ensures the paths specified are correct. Otherwise paths have to be changed.
- Select **Run DRC** in the caliber interactive window. The caliber RVE window will be pop up.

Fig 4.82: Run calibre DRC window

LVS

Once the layout complete all the DRC the next verification step follows the net list behind the layout view is extracted and compared to that of the schematic view, this is called layout Vs schematic(LVS) [4] check the extracted net list file and the parameters are subsequently used in layout verses schematic comparison and in detailed level simulation [1-3].

The tool LVS will compare the original network with one extracted from the mask layout and prove that two

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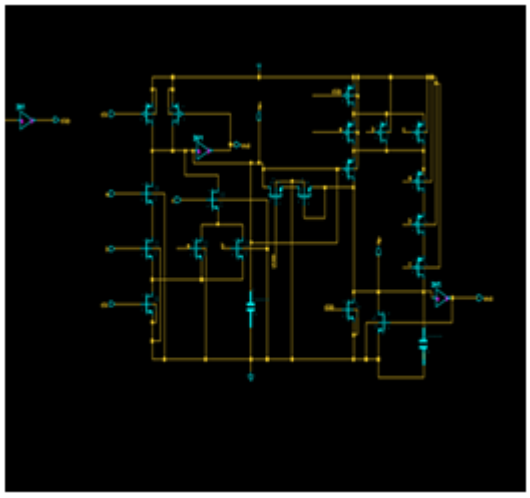
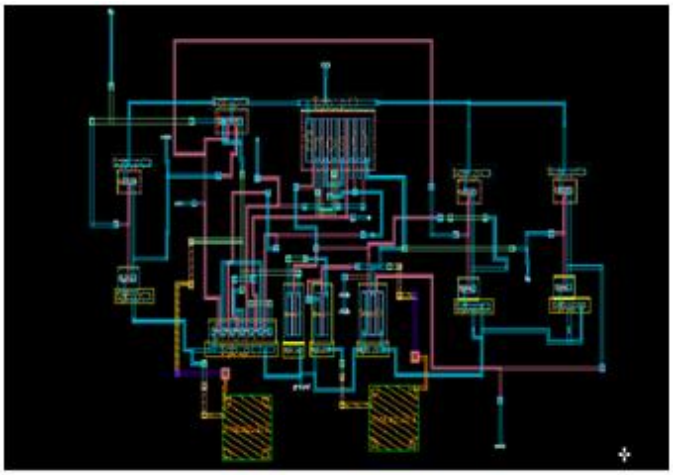
networks are indeed equivalent the LVS step provides an additional level of confidence the LVS step provides an additional level of confidence for the integrity of the design any error that may show up during LVS [4] should be corrected in the mask layout after a successful LVS we will have two main cell views for the same circuit they can be interchanged once performed these verification steps at highest hierarchical level our design is ready to be submitted to foundry [5].

RESULTS

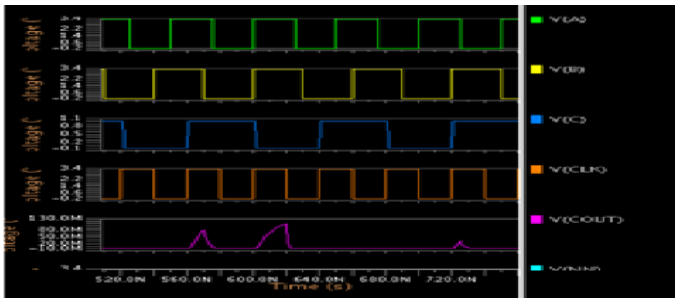
Adder Schematic: The figure illustrates the schematic of zipper dynamic adder circuit by using pull up and pull down circuit this adder circuit operates at sum and carry.



Adder schematic

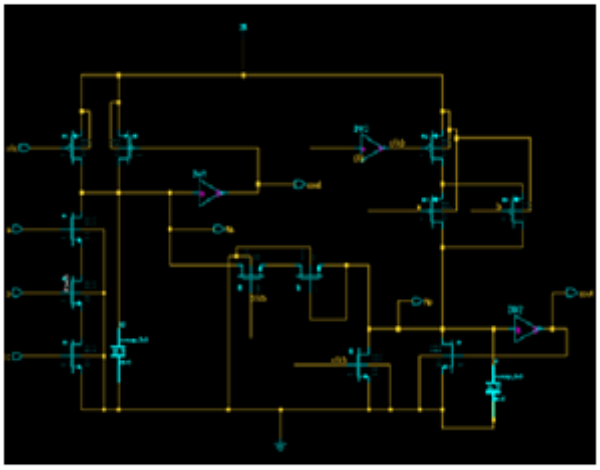


Adder Layout

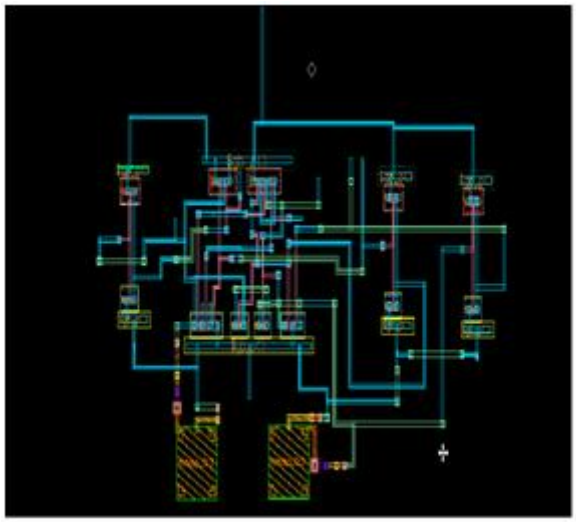


Adder Waveform

Nand Schematic : The figure illustrates the schematic of nand circuit using pull up and pull down circuits. This circuit states static behavior of circuit without clock.



Nand Schematic



Nand Layout

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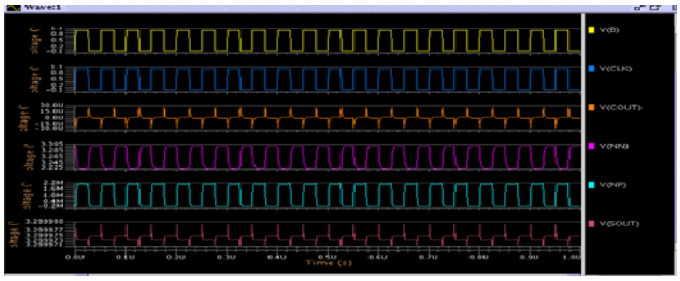

Nand Waveform

Multiplexer Schematic : This figure illustrates the schematic of multiplexer schematic which depicts multiple inputs enabling a single output .

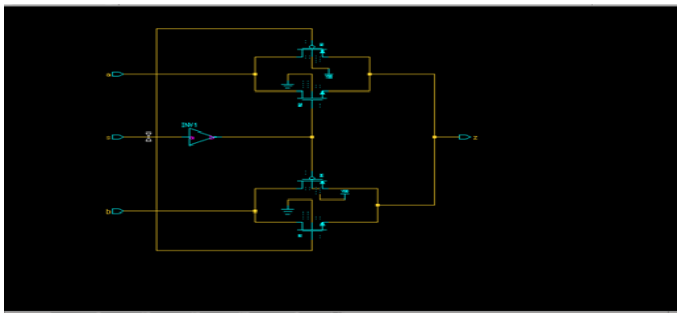

Fig.5.7. Multiplexer Schematic

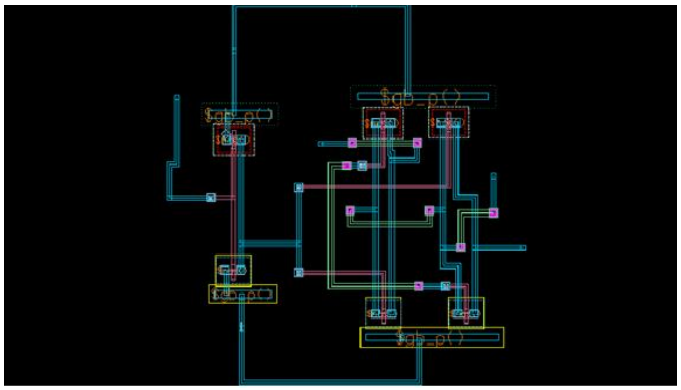

Fig.5.8.Multiplexer Layout

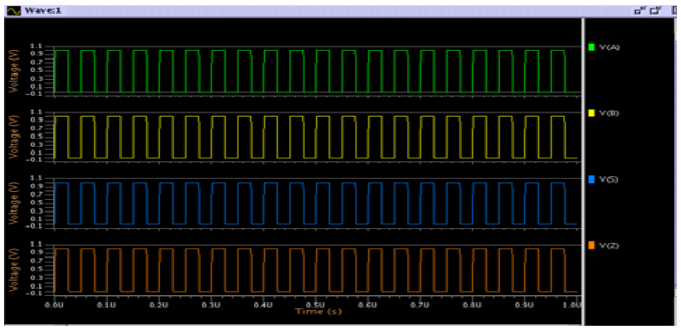

Fig.5.9.Multiplexer Waveform

5.4 Arithmetic Logic Unit : This figure illustrates the schematic of ALU using pull up and pull down circuits which performs all arithematic operations.

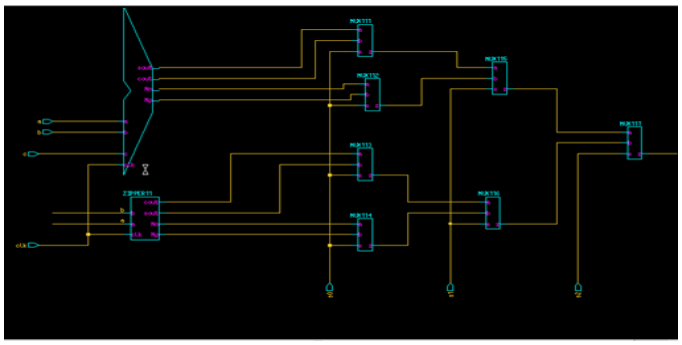

Fig.5.10. ALU Schematic

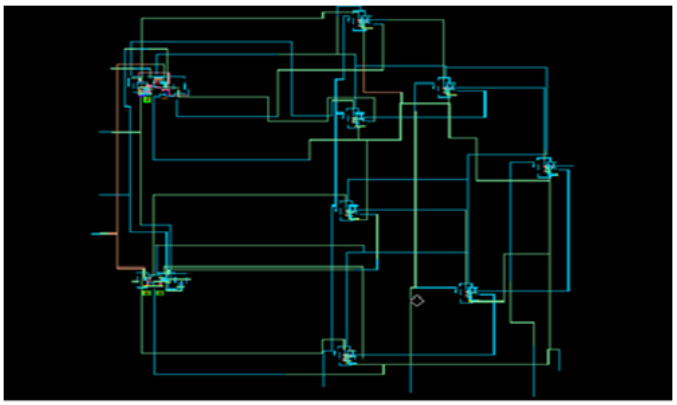

Fig.5.11. ALU Layout

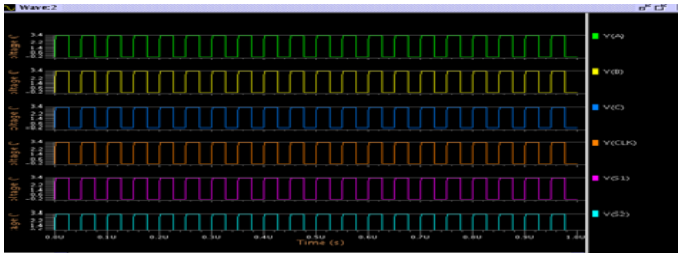

Fig.5.12.ALU Waveform1

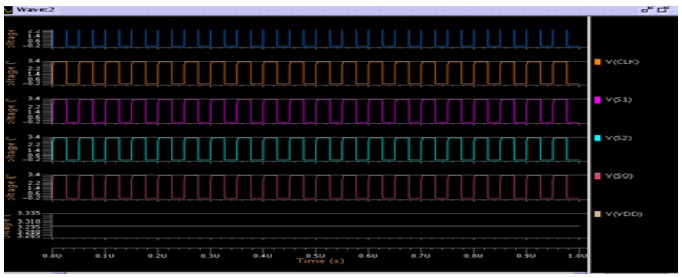

Fig.5.13.ALU Waveform2

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5.5 Voltage Analysis:

Vgs Vs Power

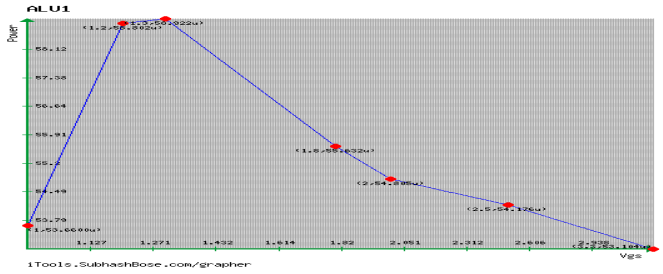

Fig.5.14.(Vdd=1)

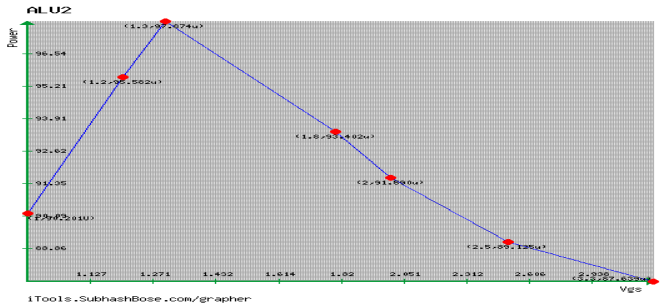

Fig.5.15.(Vdd=1.2)

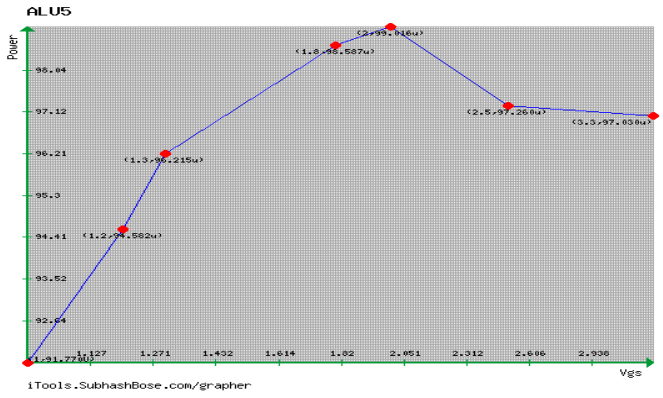

Fig.5.16.(vdd=2)

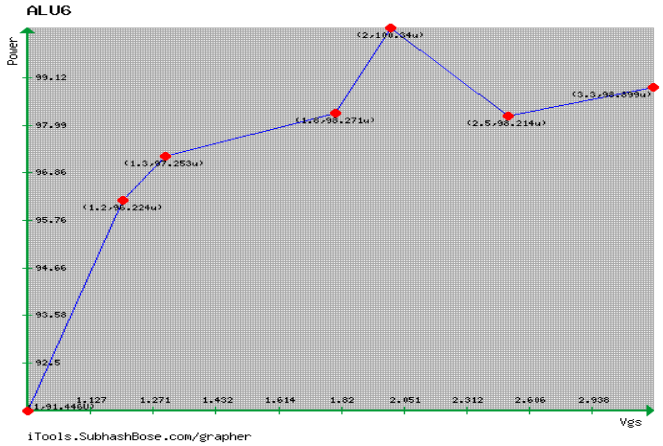

Fig.5.17.(Vdd=2.5)

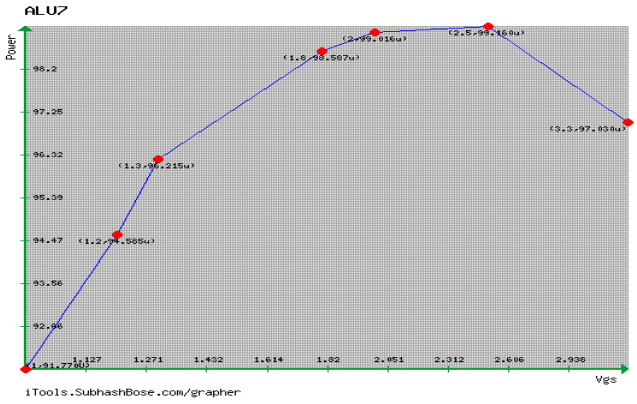

Fig.5.18.(Vdd=3.3)

Vgs Vs Delay :

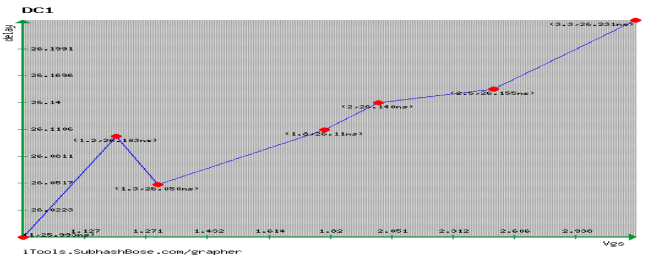

Fig.5.19.(Vdd=1)

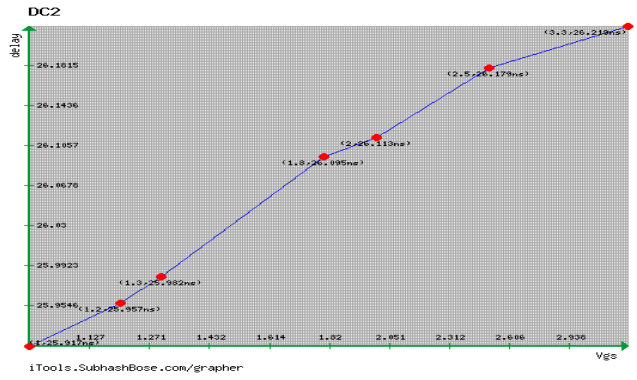

Fig.5.20.(vdd=1.2)

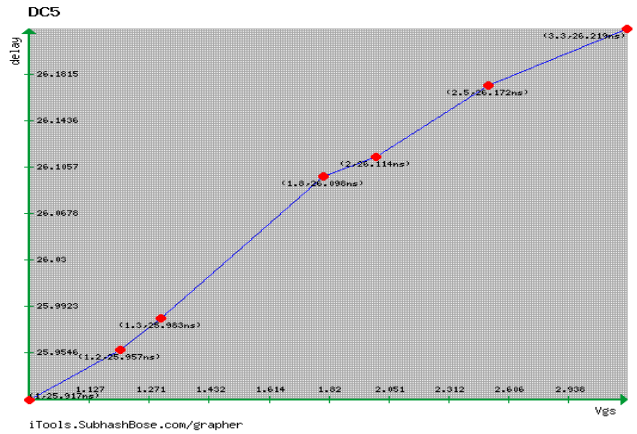

Fig.5.21.(vdd=2)

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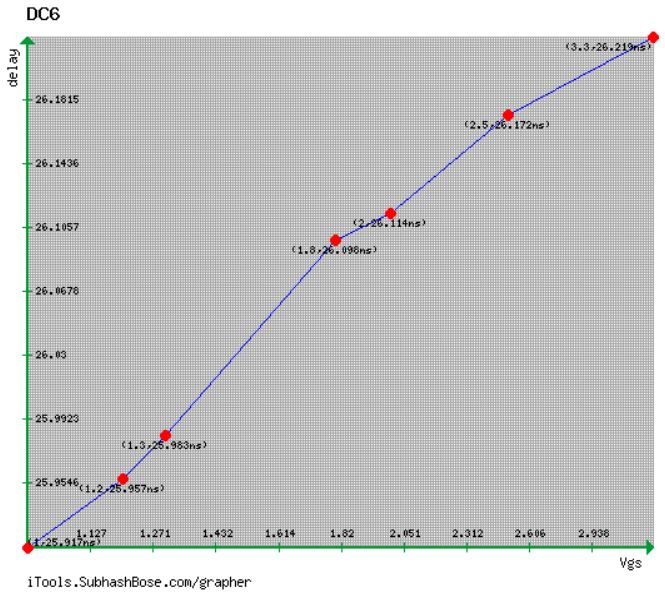

Fig.5.22.Vdd=2.5

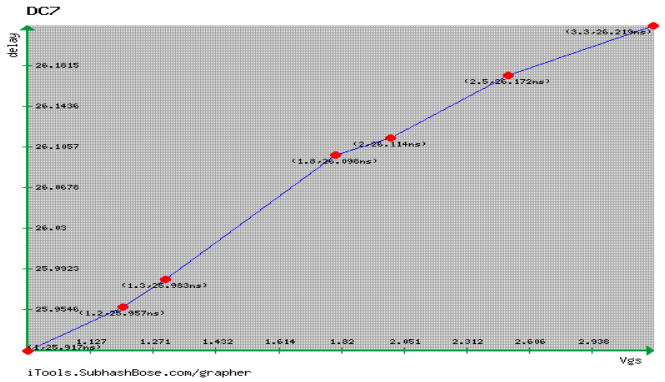

Fig.5.23.(Vdd=3.3)

CONCLUSION

A novel methodology is presented in this project for designing dynamic circuits in the functional units of modern processors. The proposed PNS-FCR methodology achieves high power efficiency, while satisfying specific timing constraints. We also have concluded from our project that PNS-FCR technique is more efficient than conventional transistors .It is also a flexible methodology to apply in wide areas and from the observed waveforms we also concluded that the power consumption of this circuit is much reduced than normal conventional transistors.So from this it can be finally concluded that it can be applied in many CMOS based logic gates ,microprocessors and microcontrollers.

FUTURE SCOPE

PNS_-FCR technique being observed as advantageous it can be applied in many large wide area electronic applications .We can also see many changes by applying this methodology as it is reliable and simple to implement as it contains minimum requirements such as adders and multiplexers which multiplies the efficiency of the object and reduces the power to maximum extent . Being flexible and affordable this implementation can be treated as greatest asset in the field of electronics as compared to conventional transistors which are complex and risky to handle .This PNS-FCR technique is mainly applied in the field of chip processing and microprocessors and microcontrollers which play a major part in our daily life aspects making the world more précised and compatible.

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