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FIFO Based Testing Using Bit Swapping

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ABSTRACT:

This technique involves repetition of tests periodically to prevent the accumulation of faults. NOC approach has emerged as a promising solution for on chip communications. This alternative way improves efficiency and in the case of detection of faults. The implementation of a prototype related to the proposed test algorithm has been integrated into the router channel interface and online test has been conducted with synthetic self similar data traffic. This on line transparent test technique is used for the detection of latent hard faults which are developed in the first input and first output buffers of routers during field operation of NoC and also proposed the fault tolerant solution by introducing shared buffer in router. Further this project can be enhanced by using scan chain reordering technique. The optimization of time is the main criteria in this enhancement.

Key Words: ***Network On Chip (NoC), Bit Swapping Linear Feed-back Shift Register (BSW LFSR), First in First Out (FIFO), Permanent fault***

INTRODUCTION:

In these recent years, network-on-chip (NoC) [1] has been emerged as a better communication network when compared to the bus-based communication network for the complex chip designs overcoming the difficulties such as bandwidth, power dissipation and signal integrity. However, just like all other system-on-a-chips(SoCs), NoC-based SoCs must also be tested for the defects. Testing the elements of the NoC infrastructure involves testing of interrouter links and routers. There is a significant amount of area of the NoC data transport medium which is occupied by the routers, which is predominantly occupied by routing logic and FIFO buffers. Accordingly, the occurrence of the probabilities of defects or run-time faults occurring in buffers and logic are significantly more when compared with the other components of the NoC. Hence, this testing process for the NoC infrastructure should begin with the routing logic of the routers and test of buffers.

Beside this, the test should be conducted periodically to ensure that no fault gets accumulated. The run-time functional faults which occur occasionally have been one of the major concerns during the testing of deeply scaled CMOS-based memories [3-5]. These are the faults which are resultant of physical effects such as aging, low supply voltage, environmental susceptibility, and these are intermittent in nature. However, the faults which are intermittent usually they exhibit a high occurrence rate relatively and finally they tend to become permanent.

Additionally, over work of these memories also cause occasional faults to become repeated enough to be classified as a permanent ones. So now, there is a need to perform online test techniques which can detect the faults occured during run-time and are irregular in nature but slowly become longlasting as the time pass on. The integration of chip has been reached a stage where a one complete system is fixed on a single chip.Primarily, this is used in the embedded systems.An SoC in a simple way can be explained as"An IC is designed by stiching together a number of independent VLSI designs [7] which helps in providing a full functionality for an

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application". When we state a complete system, it means all the required ingredients that covers a specialized type of application on a single silicon substrate. This integration is made possible only because of the rapid developments in the field of VLSI designs. An NoC is seen as a group of computational storage and I/O resources on -chip that are connected to each other by a network of routers or switches instead of connecting to point to point wires. These resources exchange information with each other using the data packets which are routed in the network in the same way as it is done in the usual networks. It is clear from the definition that we need to employ highly sophiticated and researched methodologies from traditional computer networks and implement them in the mono chips.Now, the motivating factors have to be found out which are compelling the researchers and designers to move towards the adoption of NoC architectures for the future of SoCs. The NoC area is still an inception and one of the thought why there exists several names for the same thing; some call it on chip networks, and some call networks on silicon, but the priority is given to the "Networks on Chips" (NoCs). Still, these terminologies are being used interchangeably in our tutorial.NOC means integrating several processors and on chip memories into a single chip [9].

The faults occuring in the NOC are:

- Permanent faults
- Transient faults

WORKING OF NETWORK-ON-CHIP MEMORY:

NoC Design has gained much importance in the research community as fault tolerance has been increased.The problem is because of the optimized testing time and testing power at reduced area over during the test of embedded memories in SoCs and it has being tackled separately by earlier approaches found in literature. Hence, there are no system-level solutions for these identical case of memories which are interconnected using NOC. So in this kind of aspect, the thesis focuses on providing a system level solution for testing of NOC based memory cores utilizing NoC as TAM and targeting optimization of testing time, test power and reduced DFT area overhead [10].

MBIST ARCHITECTURE:

In the proposed architecture system, based on distance and timing constraints the memory cores form into different groups.A distributed MBIST architecture has introduced for testing the different memory cores which are interconnected using NoC. The hybrid test technique and the distributed BIST architecture allows the testing of memory cores which are to be performed in very lesser time than it is required . The prospective of this architecture is an improvement on similar architectures found in literature as it allows testing of memory cores of any size while others had allowed only testing of similar memory cores. Every group has a BIST controller which is dedicated to perform parallel March test on all the given cores of a group. The groupsare is tested in a pipeline fashion. The NoC is re-used to act as TAM for delivering test instructions to the BIST controllers. So by using a distributed BIST architecture leads to the less area overhead than dedicated BIST for each core [2].

BASIC OPERATION OF SRAM:

The basic architecture of a static RAM is shown in the Figure.The location of a SRAM can be accessed randomly for reading/writing by inputting the address of the particular location. Every address is linked to a particular data input or data output pin. The architecture of the SRAM consists rectangular array of memory cells in rows that is word-lines and columns that is bit-lines and there are additional circuits arranged for decoding of addresses and to implement read and write operations. The memory location address comprises two parts. The first one is the row address (A0 to Ai1 lines,which selects one row/word- line). The second one is (Ai to An1 lines) the column address which selects one bit among all the bits of the word activated during the word-line selection. Since the addresses of row and column are not necessary at once, they can be multiplexed on the same address lines [4].A memory cell consists of four to six transistors which is a bistable flip-flop. The flip-flop

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has two states which are interpreted by the support circuitry to be a 1 or a 0. Every memory cell has a unique address or location that can be defined by the intersection of a column and row.The control logic controls the read/write operations.The chip select enable(CE#) is an additional input signal required to activate the chip [6].

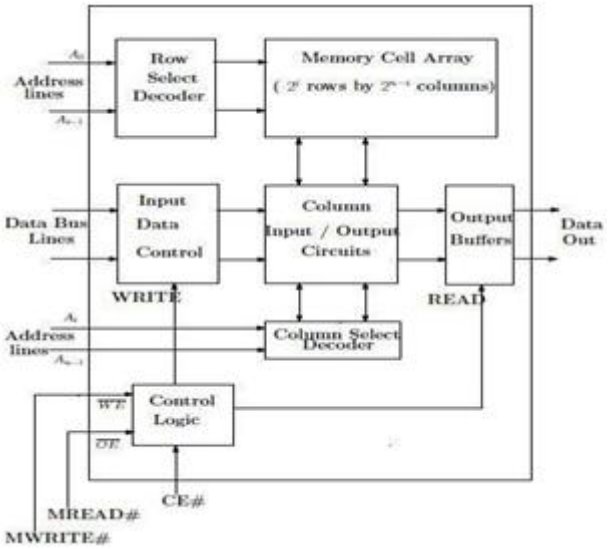

Figure 1 : Basic Architecture of SRAM

Two more control input pins are present on the chip, the WE#(write enable) and the OE#(output enable).

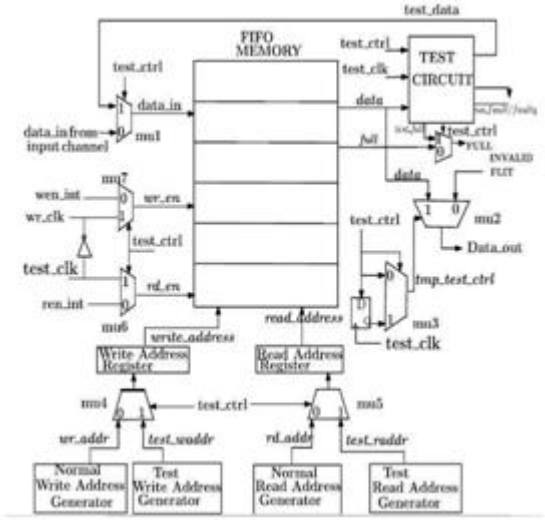

Figure 2: Testing process Process Implementation

TESTING USING FIFO BUFFER:

It is done by using the transparent test generation method. This involves the faults which are considered in brief, if they are applied to SRAMs or DRAMs, can be determined by using standard March tests. Thus, if the faults of same set are considered for SRAM type FIFOs, this March test cannot be used directly because of the restriction of address in SRAM type FIFOs mentioned and hence we are prompted to choose the address of single order MATS ++ test (SOA MATS ++) for the detection of faults which are considered in this brief. The word oriented SOA MATS ++ test is represented as {_ (wa) ; ↑ (ra,wb) ; ↓ (rb, wa) }; _ (ra) } here, a is the data background and b is the complement of the data background. ↑ and ↓ are increasing and decreasing addressing order of memory, respectively. _ means memory addressing can be increasing or decreasing.

Application of SOA MATS ++ test to the FIFO includes patterns of writing into the FIFO memory and reading them back. As a result, the contents of memory are destroyed [8]. Neverthless, online memory test techniques requires the restoration of the contents of the memory after testing. Therefore, researchers modified the March tests to transparent March test so that the tests can be performed without the requirement of any external data background and due to this the contents of memory can be restored after testing.Thus, we have transformed the SOA MATS ++ test to transparent SOA MAT S ++ (TSOA MATS ++) test that is applied for online test of FIFO buffers. The transparent SOA MATS ++ test performed is illustrated as {↑ (rx,w ¯ x, r ¯ x,wx, rx) } . The transparent SOA MATS ++ algorithm is engaged in the testing of stuck at fault, transient fault, and read stuck at fault, transition fault, and read disturb fault tests which were developed during the field operation of FIFO memories. The fault coverage of the algorithm is depicted in Fig. 2 . In the given figures, the word size of FIFO memory is assumed to be of 4 bits.

As represented in the figure let us consider the data word present in LUT be 1010.The test cycles begin with the invert phase (memory address pointer j with 0 value) during which the content of location addressed is read into temp and then backed up in the original . The data written back to SOA MATS ++ test. LUT is the

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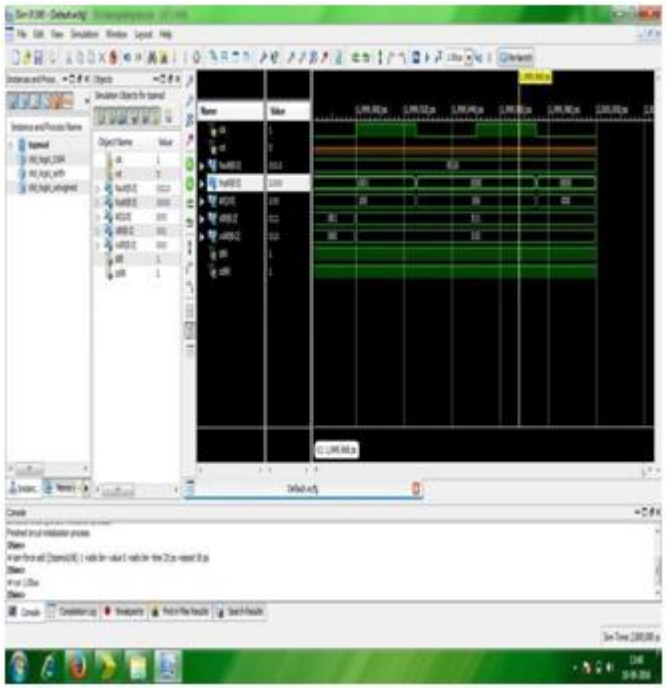
complement of the content present in temp .Thus, at the end of the cycle, the data present in temp and original is 1010, whereas lut contains 0101.Consider a stuck - At 1 fault at the most significant bit (MSB) position of the word stored in LUT . Thus, alternatively storing of 0101, it actually stores 1101 and as a result, the stuck At fault at the MSB gets excited. During the second iteration of j , when lut is readdressed, the data read into temp is 1101. At this point, the data present in temp and \ original are compared (bitwise XOR ed).

The all 1's pattern is expected as a result. Any 0 if occurs within the pattern that would mean a stuck at fault at that particular bit position.

RESULT:



CONCLUSION:

The major target of this thesis is to devise improved test techniques for NoC based memory systems which incorporate SRAM or DRAM cores interconnection using NoC and FIFO buffers which are present within the routers of the NoC infrastructure. The primary aim of the proposed work is to find out the research gap in the existing works and bring about improvements in them by reducing the expense of the test and system. This assessment of the system cost is done in particulars of testing time, power dissipation and area overhead during testing.

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