A New Approach to Design TPG for Low Power Testing Applications

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Abstract:

VLSI circuit's encounters are rapidly many challenging tasks of semiconductor manufacturing along operating with gigahertz range of frequencies. These challenges are include keeping peak power dissipation and the application time within limits. In this Paper we are proposes a new approach of low power Test Pattern Generator (TPG) designed by modifying parallel Linear Feedback Shift Register (Parallel-LFSR) deployed on Circuit under Test (CUT) to slenderize the dynamic power consumption by CUT. To propose a new output sequence of parallel-LFSR to design a low-power test pattern generator for Built In Self Test (BIST) achieve reduce the overall switching activity in CUT. New architecture for LFSR with parallel mechanism reduces the power significantly at scans. The experimental result shows a best power reduction by low power TPG than compared to LFSR. The proposed work is design and implemented using Verilog HDL and Xilinx ISE.

Keywords: BIST, LFSR, Scan and TPG.

I. INTRODUCTION:

Power dissipation is a challenging problem for today's system-on-chips (SoCs) design and test. In general, power dissipation of a system in test mode is more than in normal mode [1]. This is because a significant correlation exists between consecutive vectors applied during the circuit's normal mode of operation, whereas this may not be necessarily true for applied test vectors in the test mode. The sequence generator circuit, Linear Feedback Shift Register (LFSR), is widely used in data compression circuitry, encryption circuitry, Built-in Self-Test (BIST), communication circuitry, error correction circuitry etc. Built-In Self-Test (BIST) has emerged as a promising solution to the VLSI testing problems. BIST is a DFT methodology aimed at detecting faulty components in a system by incorporating the test logic on chip. BIST is well known for its numerous advantages such as improved testability, at-speed testing and reduced need for automatic test equipment (ATE).

LFSR is mainly used to generate patterns. Scan chain is a group of registers. Here the scan chain is mainly used to store the patterns generated from LFSR. These patterns are applied to CUT and the outputs generated from CUT are again stored in scan chain. For every input response stored in scan chain the corresponding output patterns are stored in the scan chain i.e., located at the output of the CUT. Here in comparator, it compares the input to CUT and corresponding output of CUT.

And here if there is a difference obtained at the output of the comparator fault will be detected, else there is no fault in the circuit. Here more hardware overhead is implemented, Due to this structure more number of transitions occurred and hence more power is consumed. In order to reduce the power consumption with high efficiency we need to include extra circuitry. The main challenging areas in VLSI are performance, cost, power dissipation is due to switching i.e. the power consumed testing, due to short circuit current flow and charging of load area, reliability and power. The demand for portable computing devices and communications system are increasing rapidly. The applications require low power dissipation VLSI circuits.

Several techniques have been reported to address the low power BIST problem. This paper presents a new test pattern generator for low power BIST. The proposed technique increases the correlation between test patterns. In this proposed low power test pattern generator most help at scan based testing and also especially testing of sequential and combinational circuits. The proposed test pattern generator uses parallel mechanism to design LFSR circuit. The detailed description of proposed work is present at section III. This paper id organized as follows: Section II presents previous works for low power BIST; section III presents new approach of low power TPG design; section IV is dedicated to results and V section is for concluding the work.

II.PREVIOUS WORK:

Various authors reported on techniques to cope with power problems during testing. Low power testing scheme is divided in to two categories.

1.Low power testing for external testing.

2.Low power testing for internal testing.

1. Low Power Testing for External Testing:

Reference [2] proposed a heuristic method to generate test sequences which create worst-case power droop by accumulating the high and low frequency effects using a dynamically constrained version of the classical D algorithm for test generation. A novel scan chain division algorithm has proposed in [3]. In [4] presents a low capture power ATPG and power aware test compaction method.

2. Low Power Testing for Internal Testing:

The technique proposed in [5] consists of a distributed BIST control scheme that simplifies BIST architecture for complex IC's, especially during higher levels of test activity. A BIST strategy called dual speed LFSR is proposed in [6] to reduce the circuit's overall switching activities. The technique use two different speed LFSR's to control those inputs that have elevated transition densities. The low power test pattern generator is proposed in [7] is based on cellular automata, reduces the test power in combinational circuits while attaining high fault coverage. Another low power test pattern generator based on modified LFSR is proposed in [8].

Many low power strategies are proposed for full scan and scan based BIST architecture. Recently in [9] a technique called low transition LFSR has proposed. By surveying various research works three different techniques are mostly used for low power testing those are a) generating test vectors by using modified clock scheme, b) generating test vectors by using LPATPG and c) generating test vectors by using low transition LFSR (LT-LFSR).

A) Generating test vectors by using modified clock scheme:

Girard et al. proposed the low-power test pattern generator (TPG) based on modified clock scheme. The low-power BIST technique relies on a gated clock scheme for the pseudorandom test pattern generator and the clock tree feeding the TPG. An n-bit LFSR is divided into two n/2-bit LFSRs. Basically; a clock whose speed is half of the normal speed is used to activate one half of the D flip-flops in the TPG (i.e. a modified LFSR) during one clock cycle. During the next clock cycle, the second half of the D flip-flops is activated by another clock whose speed is also half of the normal speed.

The two clocks are synchronous with a master clock CLK and have the same but shifted in time period. The clock CLK is the clock of the circuit in the normal mode and has a period equal to T.

As one can observe, a test vector is applied to the CUT at each clock cycle of the test session, only one half of the circuit inputs can be activated during the time. Consequently, the average powers as well as the peak power consumed in the CUT are minimized. Moreover, the power consumed in the TPG is also minimized since only one half of the D flip flops in the TPG can be activated in a given time interval.

Another important feature is the total energy consumption during BIST is reduced, since the test length produced by the modified LFSR is roughly the same than the produced by a conventional LFSR to reach the same or sometimes a better fault coverage. The scheme reduces test power in the CUT, generator, and clock tree. The technique achieves important test power savings with no penalty to circuit performance, fault coverage, test time, or design time.
The drawback of the technique is to reduce the randomness property of the LFSR also requires two non-overlapping clocks with half frequency and increases the area overhead.

B) Generating Test Vectors by using LPATPG:

Zhang.X proposed a Low Power Automatic Test Pattern Generator (LPATPG) with peak power reduction. The authors used two n-bit random pattern generators and n (2 x 1) multiplexers but only add one flip flop to an n-bit LFSR, therefore the area overhead of bipartite LFSR is much lower than LPATPG.

C) Generating Test Vectors by using LT-LFSR:

Mohammad Tehranipoor proposed a low-transition LFSR by combining techniques of random pattern generation called R-Injection (RI) and Bipartite LFSR for low-power BIST. The new LT-LFSR generates three intermediate patterns. The RI method inserts a new intermediate pattern between two consecutive test patterns by positioning a random-bit (R) in the corresponding bit of the intermediate pattern when there is a transition between corresponding bits of pattern pairs. The bipartite LFSR generates an intermediate pattern using one half of each of the two consecutive random patterns. The goal is to design a new random pattern generator reduces the total number of transitions among the adjacent bits in each random pattern (horizontal dimension) and transitions between two consecutive random patterns (vertical dimension) as well.

In other words, the new low transition random pattern generator increases the correlation between and within patterns. The main advantage of the technique can be used for both combinational and sequential circuits and the randomness quality of patterns does not deteriorate. The authors also use a K-input AND gate and T-latch to generate a high correlation between neighbouring bits in the scan chain, reducing the number of transitions and the average power.

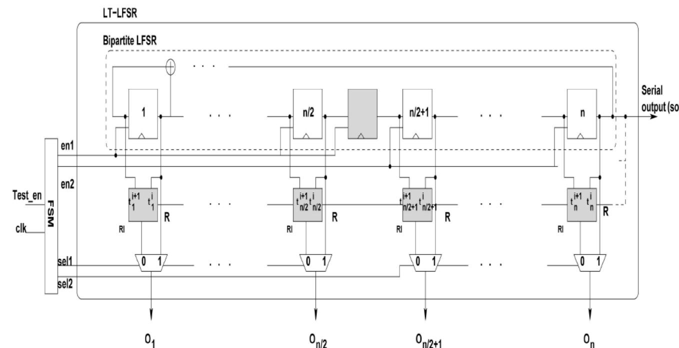

Fig.1. LT-LFSR Architecture.

III.PROPOSED TPG DESIGN

BIST Architecture:

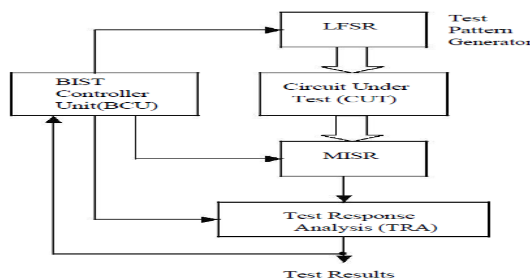

Fig.2. BIST Architecture

Proposed LFSR Design:

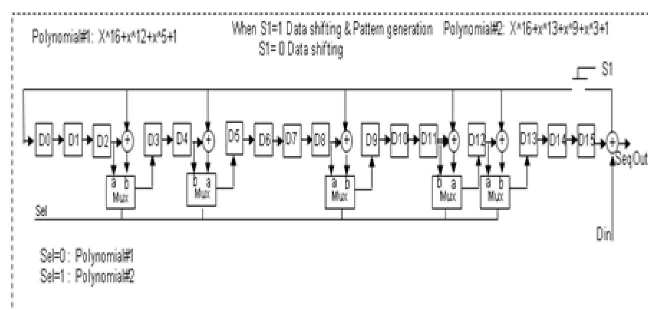

Fig.3.Proposed LFSR Architecture

The proposed LFSR architecture use D-flip flops and multiplexers to produce pseudo random sequence. The proposed LFSR uses two different polynomials to produce two different sequences for different circuits.

The proposed parallel LFSR TPG circuit will support multiple circuits testing at a time by using only one TPG circuit. The selection of multiplexer will produce intermediate patterns. As compared to the LT-LFSR the proposed LFSR circuit uses fewer resources. The proposed LFSR will operate by using single clock cycle; no need of idle the LFSR to produce intermediate patterns.

CUT: Circuit under test is the section of the circuit tested in BIST mode. It can be sequential, combinational or a memory. Their Primary Input (PI) and Primary output (Po) delimit it.

TPG: It generates the test patterns for the CUT. It is dedicated circuit or a microprocessor. The patterns may be generated in pseudorandom or deterministically.

MISR: It is designed for signature analysis, which is a technique for data compression. MISR efficiently map different input streams to different signatures with every small probability of alias.

TRA: It will check the output of MISR & verify with the input of LFSR & give the result as error or not.
BIST Control Unit: Control unit is used to control all the operations. Mainly control unit will do configuration of CUT in test mode/Normal mode, feed seed value to LFSR, Control MISR & TRA. It will generate interrupt if an error occurs.

In BIST, LFSR generates pseudorandom test patterns for primary inputs (PIs) or scan chains input. MISR compacts test responses received from primary output or scan chains output. Test vectors applied to a CUT at nominal operating frequency.

IV.RESULT DISCUSSION

A. Device Utilization Summary

Logic Utilization	Used	Available
Slices	10	1960
4 input LUT's	18	3840
Flip Flops	16	3840
IOBs	21	173
GCLKs	1	8

Table 1: Proposed LFSR Report

The proposed LFSR results are compared with the results existing in [9] in terms of LUT usage, slices, flip flops and IOB's.

B. Analysis table

LFSR type	Speed(MHZ)	Delay(ns)	Power usage(mw)
LT-LFSR	277.697MHz	10.777ns	0.067mw
Parallel-LFSR	277.594MHz	7.635ns	0.037mw

The Fig.4 shows comparison between LFSR, LT-LFSR, and Parallel-LFSR techniques the parallel-LFSR consumed less power compared to LT-LFSR and LFSR. Then automatically the system time delay will be reduced to speed up the system performance.

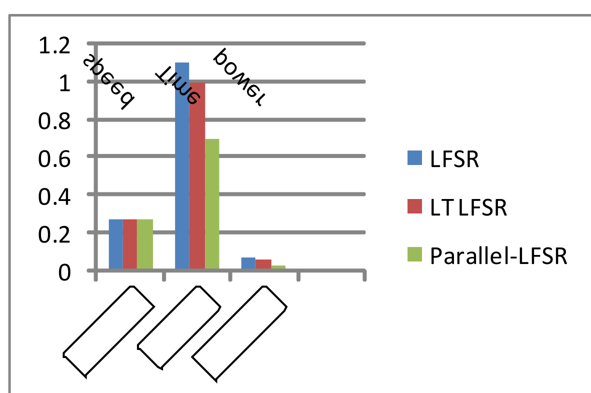

Fig.4 .Comparison between LFSR, LT-LFSR and Parallel-LFSR.

V.CONCLUSION:

The proposed new LFSR technique will reduce power in Test Pattern Generator at Scan BIST. The proposed research work implied using FPGA hardware platform. The proposed TPG reduces the number of transitions that occur at scan inputs during scan where neighbouring bits are highly correlated. The optimized architecture is designed and RTL code is developed using Verilog HDL, simulation is performed using standard EDA tools.

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