IMPROVED 32 BIT CARRY SELECT ADDER FOR LOW AREA AND LOW POWER

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ABSTRACT:

In the design of Integrated circuit area occupancy plays a vital role because of increasing the necessity of portable systems. Carry Select Adder (CSLA) is a fast adder used in data processing processors for performing fast arithmetic functions. From the structure of the CSLA, the scope is reducing the area of CSLA based on the efficient gate-level modification. In this paper 32 Bit Carry Select Adder (CSLA) architectures have been developed and compared with Square-root CSLA (SQRT CSLA). However, the Regular CSLA is still area-consuming due to the Single Ripple-Carry Adder (RCA) structure. For reducing area, the CSLA can be implemented by using X-OR Gate and two Mux circuit instead of using BEC.

Comparing the Regular Linear CSLA with Regular SQRT CSLA, the Regular SQRT CSLA has reduced area as well as comparing the Modified Linear CSLA with Modified SQRT CSLA; the Modified SQRT CSLA has reduced area. The results and analysis show that the Modified Linear CSLA and Improved 32 Bit CSLA provide better outcomes than the Regular Linear CSLA and Regular SQRT CSLA respectively. This project was aimed for implementing high performance optimized FPGA architecture. The carry select adder is programmed by using Verilog HDL and synthesized using Xilinx ISE 13.2.

INDEX TERMS:

Application-specific integrated circuit (ASIC), area-efficient, CSLA, low power.

I. INTRODUCTION:

Design of area- and power-efficient high-speed data path logic systems are one of the most substantial areas of research in VLSI system design.

In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position.

The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum [1]. However, the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input Cin=0 and Cin = 1, then the final sum and carry are selected by the multiplexers (mux).

The basic idea of this work is to use Binary to Excess-1 Converter (BEC) instead of RCA with Cin=1 in the regular CSLA to achieve lower area and power consumption [2]–[4]. The main advantage of this BEC logic comes from the lesser number of logic gates than the n-bit Full Adder (FA) structure. The details of the BEC logic are discussed in Section III.

This brief is structured as follows. Section II deals with the delay and area evaluation methodology of the basic adder blocks.

Section III presents the detailed structure and the function of the BEC logic. The SQRT CSLA has been chosen for comparison with the proposed design as it has a more balanced delay, and requires lower power and area [5], [6]. The delay and area evaluation methodology of the regular and modified SQRT CSLA are presented in Sections IV and V, respectively.

The ASIC implementation details and results are analyzed in Section VI. Finally, the work is concluded in Section VII.

II. DELAY AND AREA EVALUATION METHODOLOGY OF THE BASIC ADDER BLOCKS:

The AND, OR, and Inverter (AOI) implementation of an XOR gate is shown in Fig. 1. The gates between the dotted lines are performing the operations in parallel and the numeric representation of each gate indicates the delay contributed by that gate. The delay and area evaluation methodology considers all gates to be made up of AND, OR, and Inverter, each having delay equal to 1 unit and area equal to 1 unit. Then add up the number of gates in the longest path of a logic block that contributes to the maximum delay. The area evaluation is done by counting the total number of AOI gates required for each logic block. Based on this approach, the CSLA adder blocks of 2:1 mux, Half Adder (HA), and FA are evaluated and listed in Table I.

III. BEC:

As stated above the main idea of this work is to use BEC instead of the RCA with Cin = 1 in order to reduce the area and power consumption of the regular CSLA. To replace the n-bit RCA, an n+1-bit BEC is required. A structure and the function table of a 4-b BEC are shown in Fig. 2 and Table II, respectively. Fig. 3 illustrates how the basic function of the CSLA is obtained by using the 4-bit BEC together with the mux. One input of the 8:4 mux gets as it input (B3, B2, B1, and B0) and another input of the mux is the BEC output.

This produces the two possible partial results in parallel and the mux is used to select either the BEC output or the direct inputs according to the control signal Cin. The importance of the BEC logic stems from the large silicon area reduction when the CSLA with large number of bits are designed. The Boolean expressions of the 4-bit BEC is listed as (note the functional symbols ~ NOT, & AND, ^XOR).

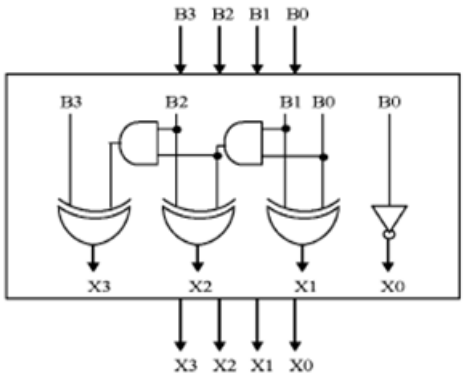

Figure 1: 4-b BEC.

X0 = ~B0;
X1 = B0 ^ B1;
X2 = B2 ^ (B0 & B1);
X3 = B3 ^ (B0 & B1 & B2);

IV. DELAY AND AREA EVALUATION METHODOLOGY OF 16-B SQRT CSLA:

The structure of the proposed 16-b SQRT CSLA using BEC for RCA with Cin = 1 to optimize the area and power is shown in Fig. 6. We again split the structure into five groups. The delay and area estimation of each group are shown in Fig. 7. The steps leading to the evaluation are given here.

1) The group2 [see Fig. 7(a)] has one 2-b RCA which has 1 FA and 1 HA for Cin = 0. Instead of another 2-b RCA with Cin =1 a 3-b BEC is used which adds one to the output from 2-b.

RCA. Based on the consideration of delay values of Table I, the arrival time of selection input c1 [time (t) =7] of 6:3 mux is earlier than the s3 [t = 9] and c3[t=10] and later than the s2 [t=4]. Thus, the sum3 and final c3 (output from mux) are depending on s3 and mux and partial c3 (input to mux) and mux, respectively. The sum2 depends on c1 and mux.

2) For the remaining group's the arrival time of mux selection input is always greater than the arrival time of data inputs from the BEC's. Thus, the delay of the remaining groups depends on the arrival time of mux selection input and the mux delay.

3) The area count of group2 is determined as follows:

$$\text{Gate count} = 43\ (\text{FA} + \text{HA} + \text{Mux} + \text{BEC})$$
$$\text{FA} = 13(1 * 13)$$
$$\text{HA} = 6(1 * 6)$$
$$\text{AND} = 1$$
$$\text{NOT} = 1$$
$$\text{XOR} = 10(2 * 5)$$
$$\text{Mux} = 12(3 * 4).$$

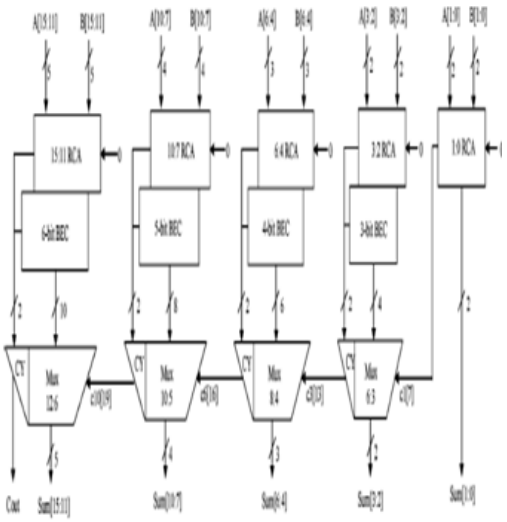

Figure 2: 16-b SQRT CSLA. The parallel RCA with Cin =1 is replaced with BEC.

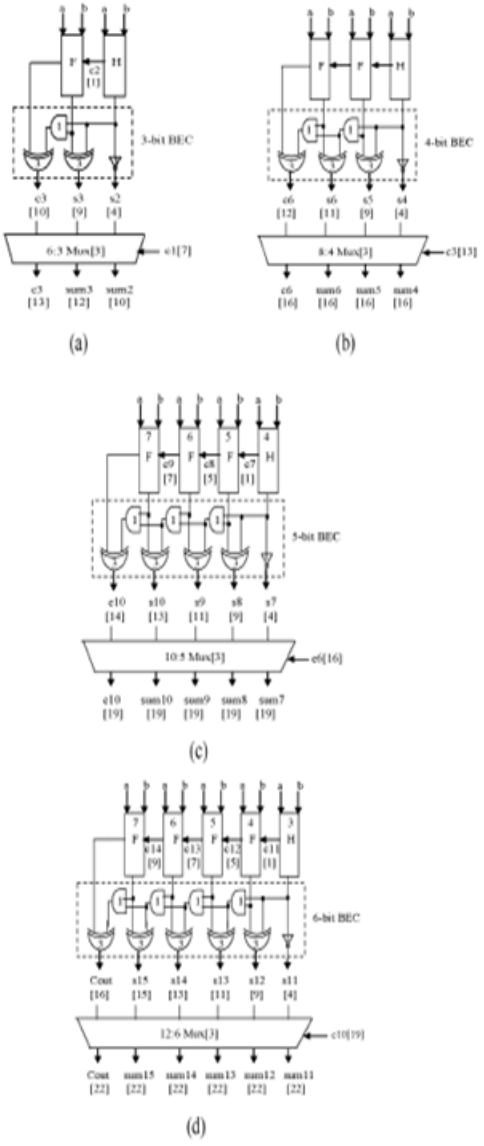

Figure 3. Delay and area evaluation of modified SQRT CSLA: (a) group2, (b) group3, (c) group4, and (d) group5. H is a Half Adder.

TABLE I Delay and Area count of modified sqrt CSLA:

Group	Delay	Area
Group2	13	43
Group3	16	61
Group4	19	84
Group5	22	107

4) Similarly, the estimated maximum delay and area of the other groups of the modified SQRT CSLA are evaluated and listed in Table IV.

The SQRT CSLA saves 113 gate areas than the regular SQRT CSLA, with only 11 increases in gate delays..

V. IMPROVED CARRY SELECT ADDER:

The truth table shown in Fig. 3 of a single-bit full-adder indicates that output sum (So) is Ex-OR of inputs A and B when carry initial is logic "0" while output So is Ex-NOR of inputs A and B when carry initial is logic "1" as illustrate as two red circles in truth table. The improved CSA can be implemented by using this technique of sharing the common Boolean logic term in summation generation as shown in Fig. 3.

Cin	A	B	S0	C0
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Figure 4. Truth table for 1-bit full adder

Hence we need to use Ex-OR gate and INV gate to generate the output sum signal pair. Sum output either the Ex-OR or the Ex-NOR could be selected using the multiplexer with select line as previous carry signal. The truth table also reveals that output carry (Co) is AND of A, B inputs when initial carry is logic "0" while Co is OR of A, B when initial carry is logic "1".Same previous carry as select line to second multiplexer is used to select the

carry output of the first stage which would act as select line of the multiplexers in the second stage. As both sum generation and carry generation is carried out in parallel therefore there exist some competitiveness in speed also the power consumption reduces as duplication of the hardware doesn't exist in improved CSA as in case of the conventional.

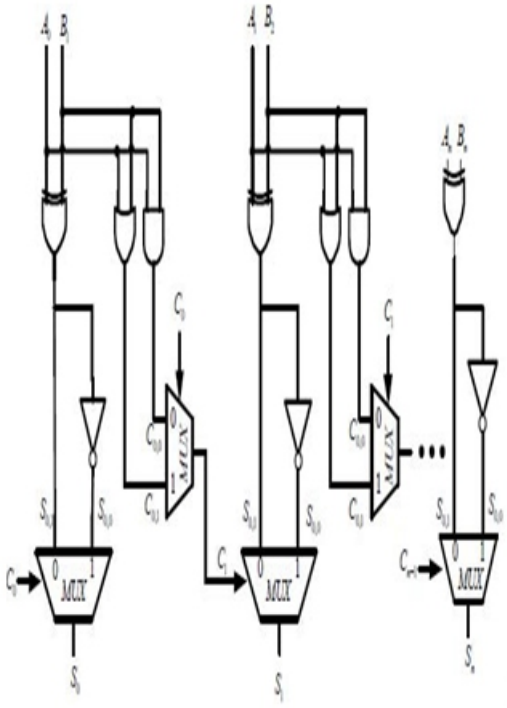

Figure 5. Improved CSLA.

This paper proposed a 32-bit CSA by using improved CSA implementing with HYBRID PTL/CMOS logic style. PTL logic is used to implement the EX-OR, EX-NOR gates and multiplexer while AND, OR, NOT gates are designed using CMOS.

Since PTL logic style doesn't gives a full swing so to overcome this two CMOS inverters are used because CMOS have a high noise margin so it correctly detects the output of PTL and generates a full swing at its output.

An EX-NOR gate is designed using PTL followed by two CMOS inverters whose output again is an EX- NOR logic while for an EX-OR logic output is taken after the first CMOS inverter used in EX-NOR gate.

VI RESULTS:

Simulation Results:

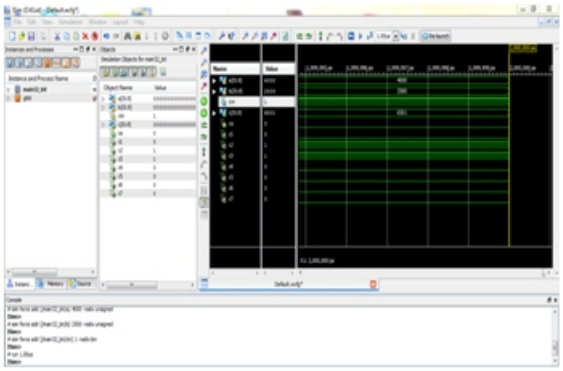

Figure 6: Simulation Result of 32 bit Improved CSLA

RTL Schematic

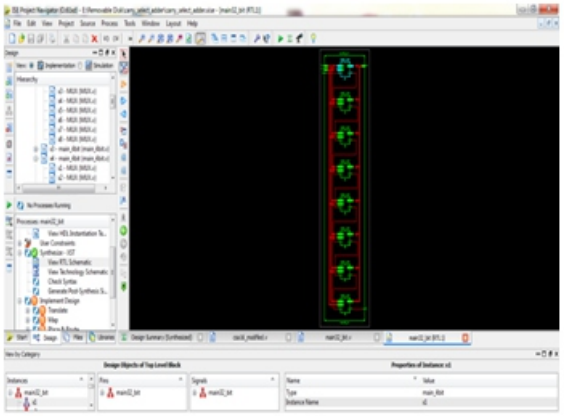

Figure 7: RTL Schematic of 32 bit Improved CSLA

Timing Report:

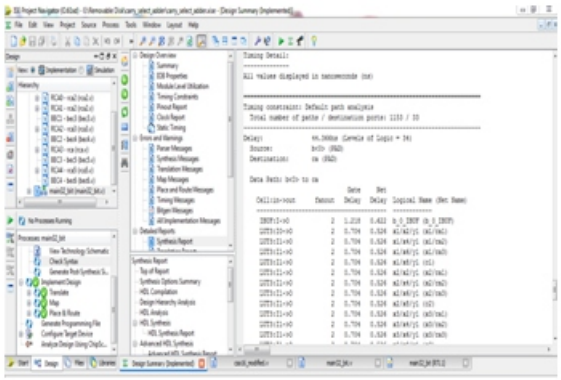

Figure 8: Timing Report of 32 bit Improved CSLA

Device Utilization Report:

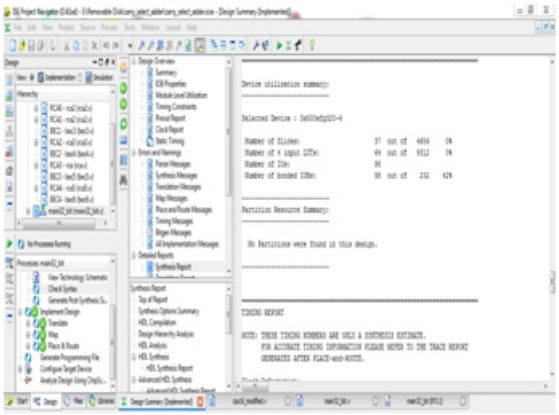

Figure 9: Device Utilization Summary

CONCLUSION:

In VLSI design, power and area are the constituent factors which limit the performance of any circuit. High Performance and power efficient circuits can be designed using Hybrid PTL/CMOS logic style. Hence 32 bit CSA using Hybrid PTL/CMOS logic style has been proposed. It has been found that the Gate count, power dissipation of the improved adder using Hybrid PTL/CMOS logic style is less than that of other conventional designs .And the above illustrated synthesis and simulation results are verified by using Xilinx ISE software.

REFERENCES:

[1] I-chyn Wey, Cheng Chen Ho, Yi-Sheng Lin ,and Chien- Chang Peng "An Area Efficient Carry Select Adder design by sharing the Boolean Logic term"vol-II,IMECS 2012,March 14- 16 2012,Hong Kong.

[2] O.Bedrij,"Carry Select Adder",IRE trans on Electronic Computers Vol EC-II,pp 340-346.1962.

[3] JM Rabaey,"Digital Integrated Circuits",IEEE trans on VLSI SYSTEMS 2003.

[4] Shen Fu Hsiao,Member,IEEE,Mingyu Tsai, and Chia ShengWen "Circuits and Systems-II";Express Briefs ,Vol 57,No1 January 2010.

[5] B. Ramkumar and Hrish M kittur, "Low-Power and Area Efficient Carry Select Adder" in IEEE Transaction on Very Large Scale Integration (VLSI) Systems, Vol.20, No.2, February 2012.

[6] Padma Devi, Ashima Girdhar, Balwinder Singh, "Improved Carry Select Adder with Reduced Area and Low Power Consumption"in International Journal of Computer Applications, Vol.3, No.4, June 2010.

[7] B. Ramkumar, H.M. Kittur, and P. M. Kannan, "ASIC implementation of modified faster carry save adder," Eur. J. Sci. Res., vol. 42, no. 1, pp.53–58, 2010.