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Pulse Triggered Flip Flop For Low Area and Low Power

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ABSTRACT:

A new family of low-power and high-performance flip-flops, namely conditional data mapping flip-flops (CDMFFs), which reduce their dynamic power by mapping their inputs to a configuration that eliminates redundant internal transitions. We present two CDMFFs, having differential and single-ended structures, respectively, and compare them to the state-of-the-art flip-flops. The results indicate that both CDMFFs have the best power-delay product in their groups, respectively. In the aspect of power dissipation, the single-ended and differential CDMFFs consume the least power at data activity less than 50%, and are 31% and 26% less power than the conditional capture flip-flops at 25% data activity, respectively.

In the aspect of performance, CDMFFs achieve small data-to-output delays, comparable to those of the transmission-gate pulsed latch and the modified-sense-amplifier flip-flop. In the aspect of timing reliability, CDMFFs have the best internal race immunity among pulse-triggered flip-flops. A post-layout case study is demonstrated with comparison to a transmission-gate flip-flop. The results indicate the single-ended CDMFF has 34% less in data-to-output delay and 28% less in power at 25% data activity, in spite of the 34% increase in size.

Tags:

low power design, JK flips flop, pulse triggered.

I.INTRODUCTION:

In recent years the power dissipation has become a critical issue for IC designers. For battery-operated systems such as laptops, Ipads, mobile phones and some other digital appliances the power consumption is a major factor because it determines the battery life and also the consumer valuation of the product is directly influenced by this factor. In the IC design the important factors to be taken into consideration are not only the circuit's speed but also their power consumption. Since more circuits are integrated into a single chip, the power consumption becomes a serious challenge to VLSI designers.

Latching and stabilizing data in short intervals are viewed as advantages of single-edge triggered flip-flops. However, wastage of one clock edge per clock cycle is seen. Double-edge triggered flip-flop can latch the data signal changes both on the rising edge and falling edge. Thus, compared to single-edge triggered flip-flops applying such double-edge ones allows the data to be preserved by using lower clock frequency

II.RELATED WORK:

Both master-slave (MS-) and pulsed-triggered (P-) flip-flops (FFs) are commonly used in contemporary synchronous digital systems. Conventional MS-FFs, consisting of two cascaded latches (i.e. master and slave), are characterized by a positive setup time requirement that increases the data-to-output delay. P-FFs are considered to be an interesting alternative to MS-FFs.

Their operation is based on the generation of a narrow transparency window in correspondence of the rising (or falling) clock edge. In this way a near to zero or even negative setup time is allowed and smaller data-to-output delay is achieved. Moreover, since the operation of a P-FF requires only a single latch, as opposed to two latches needed in MS configurations, the logic complexity of the circuit is reduced, thus leading to lower power consumption .

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III.IMPLEMENTATION:

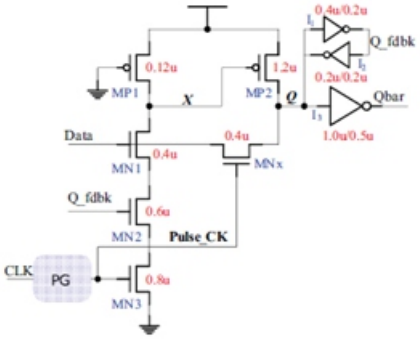

Fig 1.Schematic of the proposed P-FF design.

Referring to above Fig., the proposed design adopts a signal feed-through technique to improve this delay. Similar to the SCDFF design, the proposed design also employs a static latch structure and a conditional discharge scheme to avoid superfluous switching at an internal node. However, there are three major differences that lead to a unique TSPC latch structure and make the proposed design distinct from the previous one.

First, a weak pull-up pMOS transistor MP1 with gate connected to the ground is used in the first stage of the TSPC latch. This gives rise to a pseudo-nMOS logic style design, and the charge keeper circuit for the internal node X can be saved. In addition to the circuit simplicity, this approach also reduces the load capacitance of node X . Second, a pass transistor MNx controlled by the pulse clock is included so that input data can drive node Q of the latch directly (the signal feed-through scheme).

Along with the pull-up transistor MP2 at the second stage inverter of the TSPC latch, this extra passage facilitates auxiliary signal driving from the input source to node Q. The node level can thus be quickly pulled up to shorten the data transition delay. Third, the pull-down network of the second stage inverter is completely removed. Instead, the newly employed pass transistor MNx provides a discharging path. The role played by MNx is thus twofold, i.e., providing extra driving to node Q during 0 to 1 data transitions, and discharging.

IV.RESULTS:

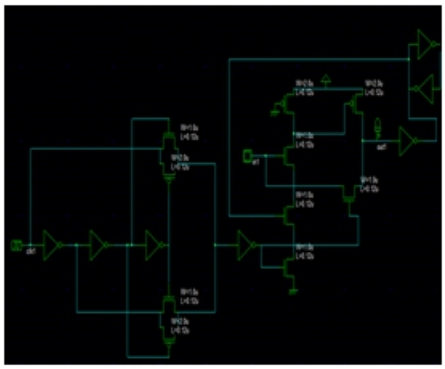

Fig 2 proposed schematic with pulse triggering

Referring to above Fig2.The proposed design adopts a signal feed-through technique to improve this delay. Similar to the CDFF design, the proposed design also employs a static latch structure and a conditional discharge scheme to avoid superfluous switching at an internal node. However, there is a differences that lead to a unique latch structure and make the proposed design distinct from the conventional one.

Fig 3 simulation result of proposed method.

A pass transistor MNx showed in the schematic In fig 2 and its simulation in fig 3 controlled by the pulse clock is included so that input data can drive node Q of the latch directly (the signal feed-through scheme). Along with the pull-up transistor MP2 at the second stage inverter of the latch, this extra passage facilitates auxiliary signal driving from the input source to node Q.

CONCLUSION:

One effective method, reducing capacity of the clock load by minimizing number of clocked transistor, is elaborated. Following the approach, one novel method is proposed, which reduces local clock transistor number and power consumption.

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ANALYSIS:

	NO OF TRANSISTOR	NUMBER OF OUTPUT BITS	AREA (UM)	POWER CONSUMPTION
FLIP FLOP	6	6	600	19.16 UW
CLOCKED PAIR	8	4	300	0.16MW
DOUBLE EDGE FLIPFLOP	10	12	267	0.26MW
DOUBLE EDGE CLOCKED PAIR	10	12	0.3	0.7MW

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