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# **Implementation of Orthogonal Frequency Division Multiplexing**

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#### Abstract:

The demand of wireless communications is increased in high speed, high security applications like missile communication, satellite communication etc. The communication with these features can be achieved by using different carrier modulation techniques like single carrier, multi carrier modulation etc. The multi carrier modulation with orthogonality of carriers provides high speed communication. This process is called Orthogonal Frequency Division Multiplexing (OFDM). The high speed and band width utilization can be achieved by using OFDM. The high security communication can be achieved by using coders and spreaders with different random generator sequences with the help of Spread Spectrum techniques and it is used for high speed and high secured communication system. The OFDM technique consists of a back to back connected transmitter and receiver with 8-point FFT/IFFT and QPSK modulation. This technique is designed by using Verilog HDL with Xilinx ISE Design suite 12.4 version tool.

#### Keywords: OFDM, IFFT, FFT, QPSK

#### **I.INTRODUCTION**

The secured and high speed data wireless data networks are the order of the day in missile communication. Future systems may demand a data communication up to 10 Mbps or more. Communicating at high transmission rates over the harsh wireless environment, however, creates many difficult and challenging problems. The requirement of high RF bandwidth and implementation difficulties discourages the development of such system. R.Vasim Akram Assistant Professor, Department of VLSI, Sir C.V.Raman Institute of Technology and Sciences, Anantapur, India.

The demand for high-speed and high security wireless communications services has grown tremendously. Today, Third Generation (3G) cellular wireless services have become very popular in many countries over the world although their deployment has been slower at the beginning. The 3G standard was created by the International Telecommunication Union (ITU) and is called IMT-2000 in order to harmonize worldwide existing 3G systems to provide global roaming. A 3G system must allow simultaneous use of speech and data services, and provide peak data rates of at least several hundred of kbps, and up to several Mbps according to the original releases of the 3G interfaces:

A Fourth Generation (4G) system is expected to provide many high-speed data services such as Internet Protocol (IP) telephony, ultra-broadband Internet access, gaming services and streamed multimedia. Recently, pre-4G technologies such as mobile Worldwide Interoperability for Microwave Access (WiMAX) and first-release Third Generation Partnership Project (3GPP) Long Term Evolution (LTE) technologies have been available on the market. These technologies are based on the advantages of OFDM technology which offers high-speed data transmission and robustness to multipath fading without having to provide powerful channel equalization. A number of the World's operators and vendors are already committed to LTE deployments and developments, making LTE the market leader in the upcoming evolution to 4G wireless communication systems. The OFDM is a multi carrier technique. Multi carrier modulation technique has more advantages compared to single carrier modulation technique. The difference between the single carrier modulation



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technique and multi carrier modulation technique are explained below.

## 1.1 Single-Carrier Vs Multi-Carrier Modulation



Fig 1: Single Carrier Vs Multi Carrier

## II ORTHOGONAL FREQUENCY DIVISION MULTIPLEXING

The Orthogonal Frequency Division Multiplexing (OFDM) is a multi-carrier modulation scheme that transmits data over a number of orthogonal subcarriers. A conventional transmission uses only a single carrier modulated with all the data to be sent. OFDM breaks the data to be sent into small chunks, allocating each sub-data stream to a sub-carrier and the data is sent in parallel orthogonal sub-carriers.

OFDM is actually a special case of Frequency Division Multiplexing (FDM). In general, for FDM, there is no special relationship between the carrier frequencies, f1, f2 and f3. For OFDM on the other hand, there must be a strict relation between the frequency of the sub-carriers, i.e.  $fn = f1 + n\Delta f$  where  $\Delta f = 1/TU$  and TU is the symbol time. These subcarriers have different frequencies which are orthogonal to each other. Each sub channel requires a longer symbol period. Therefore OFDM systems can overcome the Inter Symbol Interference (ISI). As a consequence, the OFDM systems can result in lower bit error rates and higher data rates than conventional communication systems. The difference between the Frequency Division Multiplexing (FDM) and Orthogonal Frequency Division Multiplexing is shown in Figure.

Splitting the channel into narrowband channels enables significant simplification of equalizer design in multipath environments. Flexible bandwidths are enabled through scalable number of sub-carriers.



#### 2.1 Orthogonality between the subcarriers:

The essential property of the OFDM signal is the orthogonality between the subcarriers. Orthogonal means "perpendicular", or at "right angle". Two functions,  $X_q$  (*t*) and  $X_k$  (*t*), are orthogonal over an interval [a, b] if the inner product between them is zero for all *q* and *k*, except for the case that q = k, i.e. when  $X_q$  (*t*) and  $X_k$  (*t*) are the same function. Mathematically this can be written as:



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$$\left\langle x_q, x_k \right\rangle = \int_{a}^{b_U} x_q(t) \cdot x_k(t) dt = \begin{cases} 1, & k = q \\ 0, & k \neq q \end{cases}$$

The orthogonality allows simultaneous transmission on a lot of sub carriers in a tight frequency space without interference from each other. In essence this is similar to CDMA, where codes are used to make data sequence independent (also orthogonal) which allows many independent users to transmit in same space successfully. In this all the frequencies are harmonic to one frequency. In this case these carriers are orthogonal to each other, when added together; they do not interfere with each other.

The complexity of OFDM system can be reduced by applying the Discrete Fourier Transform (DFT) to generate the orthogonal subcarriers waveforms. In this model, baseband signals are modulated by the Inverse DFT (IDFT) in the transmitter and then demodulated by DFT in the receiver. Therefore, all the subcarriers are overlapped with others in the frequency domain, while the DFT modulation still assures their orthogonality. Moreover, the windowing technique is used to attack the Inter-Symbol Interference (ISI) and Inter-Carrier Interference (ICI) problems.



Fig 3: Block diagram of OFDM

#### 2.2 Spreader:

The Spreader can be implemented by using the Linear Feedback Shift Register (LFSR). The generator polynomial governs all the characteristics of generator. The feedback generator uses only the output bit to add several stages of shift register. This is desirable for high speed hardware implementation as well as software implementation. The m stage linear feedback shift register is shown in Figure



It consists of a shift register made up of m flip flops and a logic circuit. The flip flops in the shift registers are regulated by a single timing clock. The binary sequences are shifted through the shift registers and output of the various stages are logically combined and feedback as the input to first stage. The initial contents of flip flops determine the contents of memory. The generated PN sequence is mainly generated by three factors that are length m of the shift register, initial state of flip flops and feedback logic.

The number of possible states of the shift register is at most  $2^m$  for an m flip flop. So the generated PN sequence must be periodic with a period at most  $2^m$ . When the feedback logic consists of Exclusive-OR gates, the shift register is called linear and in such a case, the zero state is not permitted. Therefore the period of PN sequence produced by a linear m-stage shift register cannot exceed  $2^m$ -1. When a sequence of period  $2^m$ -1 is generated, it is called Maximal Length (ML) sequence.



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#### 2.3 QPSK framer:

Information such as sound (audio), images (video) and digital data can be transmitted from one point to other using radio waves. This is done by modulating an RF signal carrier with the information to be transmitted. The Modulation is variation of one or more properties of RF signal to represent the information being transmitted.

The different types of modulation techniques to be used are Amplitude Shift Keying (ASK), Frequency Shift Keying (FSK), Phase Shift Keying (PSK), Quadrature Phase Shift Keying (QPSK) etc. Amplitude Keying (ASK) is a form of amplitude Shift modulation that represents digital data as variations in the amplitude of a carrier wave. Frequency Shift Keying (FSK) is a frequency modulation scheme in which digital information is transmitted through discrete frequency changes of a carrier wave. Phase Shift Keying (PSK) is a digital modulation scheme that conveys data by changing, or modulating, the phase of a reference signal (the carrier wave). The difference between ASK, FSK and PSK are shown in Figure 5



#### 2.4 QPSK Modulation:

The Quadrature Phase Shift Keying (QPSK) is the digital modulation technique. The Quadrature Phase Shift Keying (QPSK) is a form of Phase Shift Keying in which two bits are modulated at once, selecting one of four possible carrier phase shifts (0,  $\Pi/2$ ,  $\Pi$ , and  $3\Pi/2$ ). The Quadrature Phase Shift Keying (QPSK) is effectively two independent BPSK systems (I and Q), and therefore exhibits same performance but twice bandwidth efficiency.

QPSK perform by changing the phase of the In-phase (I) carrier from  $0^{\circ}$  to  $180^{\circ}$  and the Quadrature-phase (Q) carrier between  $90^{\circ}$  and  $270^{\circ}$ . This is used to indicate the four states of a 2-bit binary code. Each state of these carriers is referred to as a Symbol.

Quadrature Phase-shift Keying (QPSK) is a widely used method of transferring digital data by changing or modulating the phase of a carrier signal. In QPSK digital data is represented by 4 points around a circle which correspond to 4 phases of the carrier signal. These points are called symbols. The constellation diagram of QPSK modulation technique is shown in Figure 6



Fig 6: Constellation diagram of QPSK modulation technique

The binary data modulates each phase, producing four unique sine signals shifted by  $45^{\circ}$  from one another. The two phases are added together to produce the final signal. Each unique pair of bits generates a carrier with different phase. This is shown in Table



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# Table 1: Carrier phase shift for each pair of bits represented

Bit pairs	Phase(degrees)
00	0
01	90
10	180
11	270

## **2.5 IFFT Modulator:**

To reduce the complexity, Inverse Fast Fourier Transform (IFFT) technique is used in transmitter. The IFFT is used to convert from frequency domain to time domain. IFFT is an algorithm that is useful for speeding up the computation.

When applied in time domain, the algorithm is referred to as a Decimation-In-Time (DIT) FFT. The Decimation refers to significant reduction in the number of calculations performed on time domain data.

The Fast Fourier Transform (FFT) is an algorithm that efficiently computes the Discrete Fourier Transform (DFT). The DFT of a sequence  $\{x(n)\}$  of length N by a complex valued sequence  $\{X(K)\}$ 

$$X(K) = \sum_{n=0}^{N-1} x(n) e^{(-\frac{j2\pi nk}{N})} , 0 \le k \le N-1.$$

Let  $W_N$  be the complex-valued phase factor, which is an N th root of unity expressed by

 $W_N = e^{-j2\pi/N}$ 

Hence X (K) becomes

X (K) = 
$$\sum_{n=0}^{N-1} x(n) W_N^{-nk}$$
,  $0 \le k \le N-1$ .

Similarly Inverse Discrete Fourier Transform (IDFT) become

X (n)=1/N 
$$\sum_{k=0}^{N-1} X(K) W_N^{nk}$$
,  $0 \le n \le N-1$ .

The Decimation In frequency Fast Fourier Transform (DIF-FFT) decomposes the DFT by recursively splitting the sequence elements X (K) in the frequency domain into sets of smaller and smaller subsequences.

## **2.6 DIF-IFFT construction rules:**

- The given sequence of length  $N=2^{M}$  , where m is the integer
- The numbers of stages in DIF-FFT algorithm are  $\log_2^{N}$ .
- The numbers of complex multiplications are  $N/2 \log_2^{N.}$
- The numbers of complex additions are N log<sub>2</sub><sup>N.</sup>
- The exponent of the twiddle factor as a function of stage index(m) is given as
- $K = \frac{Nt}{2^{(M-m+1)}}$ , where t=0,1,2.....2<sup>M-m</sup>-1.
- The output is in bit reversal form.

The butterfly diagram of 8-point DIT-FFT is shown in Figure



## 2.6 Parallel in Serial out (PISO):

The parallel in serial out block converts the parallel data in to serial data in each clock pulse. The output of

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the Inverse Fast Fourier transform (IFFT) consists of 8 real and 8 imaginary parts. So the parallel data is converted into serially in 16 clock cycles. This can be shown in Figure



Fig 8: Output of parallel in serial out in each clock pulse

To eliminate ISI in OFDM a guard time is inserted with duration longer than the multipath channel maximum delay. Moreover, to eliminate ICI in OFDM the guard time is cyclically extended. Note that in a multipath channel an appropriate guard time avoids ISI but not ICI, unless it is cyclically extended. The cyclically extension of an OFDM symbol is shown in Figure 2.19. Here the cyclic prefix to be added is the least significant bits (LSB) of the OFDM frame are added to the most significant bits (MSB).



The cyclic prefix to be added is at most 1/4 th of the OFDM frame. It may be noted that is the serial data of real and imaginary numbers are actually time domain signals when converted from digital to analog. And the frequencies that they represent are orthogonal to each other. The orthogonality of sub-channels is key point for higher capacity of the OFDM because it allows overlapping of sidebands. Overlapping results in 50% increase in capacity of the wireless channel. The guard delay between two OFDM symbols must maintain this orthogonality. The Cyclic Prefix is copied from tail portion of the OFDM symbol and added to the beginning of next OFDM symbol in such a way that orthogonality of the sub-channels is maintained. This combined data of the OFDM symbol and cyclic prefix constitutes the full OFDM symbol in time domain to be converted into analog signal I and Q which will be

transmitted after multiplying the I and Q separately with sine and cosine of the IF signal and added together to form base band signal. The base band signal is RF modulated and given to RF front end.

## 2.7 Serial in Parallel out (SIPO):

The Serial in Parallel out (SIPO) is used to convert serial data into parallel data. In the receiver after RF front end analog to digital conversion is done separately for I and Q channels and the cyclic prefix is removed. The serial data is converted into parallel eight streams representing the same time domain signal as transmitted by the IFFT.

## **III FFT Demodulator:**

To reduce the complexity Fast Fourier Transform (FFT) technique is used in receiver. The FFT is used to convert from time domain to frequency domain. The FFT is an algorithm that is useful for speeding up the computation.

When applied in time domain, the algorithm is referred to as decimation-in-time (DIT) FFT. Decimation refers to significant reduction in number of calculations performed on time domain data.

The Fast Fourier Transform (FFT) is an algorithm that efficiently computes the Discrete Fourier Transform (DFT). The DFT of a sequence  $\{x (n)\}$  of length N by a complex valued sequence  $\{X (K)\}$ 

X (K) = 
$$\sum_{n=0}^{N-1} x(n) e^{(-\frac{j2\pi nk}{N})}$$
, Where  $0 \le k \le N-1$ .

Let  $W_N$  be the complex-valued phase factor, which is an N th root of unity expressed by  $W_N = e^{-j2\pi/N}$ 

Hence X(K) becomes  $X(K) = \sum_{n=0}^{N-1} x(n) W_N^{-nk} \qquad , 0 \le k \le N-1.$ 

Similarly Inverse Discrete Fourier Transform (IDFT) become

X (n) =1/N  $\sum_{k=0}^{N-1} X(K) W_N^{nk}$ ,  $0 \le n \le N-1$ .



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The Decimation In frequency Fast Fourier Transform (DIF-FFT) decomposes the DFT by recursively splitting the sequence elements X (K) in the frequency domain into sets of smaller and smaller subsequences.

## **3.1 DIT-FFT construction rules:**

- The given sequence of length  $N=2^{M}$ , where m is integer
- The input is in bit reversal form.
- The numbers of stages in DIT-FFT algorithm are  $\log_2^{N}$ .
- The numbers of complex multiplications are  $N/2 \log_2^{N}$
- The numbers of complex additions are  $N \log_2^{N}$ .
- The exponent of the twiddle factor as a function of stage index(m) is given as
- $K = \frac{Nt}{2^{n}m}$ , where t=0, 1, 2.....2<sup>m-1</sup>-1.

The butterfly diagram of 8-point DIT-FFT is shown in Figure



Fig 10: Butterfly diagram of 8-point FFT

#### 3.1.1 QPSK Deframer:

The parallel data bits are taken two bits together and converted from I, Q to the data bit pattern. The parallel data is converted into serial data. This operation is exactly reverse to QPSK framer.

## **3.2 Despreader:**

The serial data is again Exclusive-OR with the PN pattern and resulting in original data bit pattern.

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N	ime	Yalue	Das	500 ns	1,000 ns	1,500 ns
,	💐 cut[15:0]	0000000000000		1000000010111100	10100000010	111 (001000001)
	🐚 dk	0				
	1 rst	1				
,	📢 in(7:0]	11101100	11101100 )	00111011	χ	1010111

Fig 11: Simulation results of Spreader

Name Value		Ons	50 ns	100 ns	150 ns	200 ns	250 ns	300 rs	350 n
li <mark>n</mark> dk	0								
🔓 rst	1								
🕨 👹 in[15:0]	0001	0001	0010	0011 ( 0100	) 0101	0110	0111 )	1000 ( 100	i )(
🕨 🙀 DIRO[31:0]	3£800000	(3f800000) 000	0000 ( 398000	00 / 0000000	3f800000	doccocco ( 3f8	0000 ( 0000	JOOD ( 3F800000	100
🕨 🙀 DR1[31:0]	3£800000				3f800000				
🕨 👹 DIR2[31:0]	3£800000	3f800000		0000000	3f8000	0)	00000000	3f8000	00
🕨 🙀 DR3(31:0]	00000818				3f800000				
▶ 👯 DR4[31:0]	3£800000		3f800000			00000000		3f8000	00
🕨 🙀 DR5[31:0]	00000818				3f800000				
🕨 👹 DR6[31:0]	3£800000	<u></u>		3	F800000			00000	00
🕨 🙀 DR7[31:0]	3£800000				3f800000				
🕨 🙀 DXD0[31:0]	00000000	(0000000) 3f8		00 ( 36800000	0000000	\$60000 000	0000 ( 3/80/	.000 ( 0000000	31.
🕨 🙀 DK11[31:0]	00000000				0000000				
🕨 🙀 DX12[31:0]	00000000	00000000		3/800000	00000	) 0	3f800000	( 00000	00
🕨 🙀 DXI3(31:0]	00000000				00000000				
<b>) 👯</b> DX14[31:0]	00000000		00000000			3/800000		00000	00
🕨 🙀 DAD5[31:0]	00000000				0000000				
🕨 🙀 DX16[31:0]	0000000			0	000000			398000	00
• 1007[31:0]	00000000				0000000				

Fig 12: Simulation results of QPSK Framer

ame	Value 0	ns	50 ns	100 ns
M IXR0[31:0]	00000000	3f800000	00000000	3f800000
😽 DR1[31:0]	00000000		00000000	
M IXR2[31:0]	3£800000	00000000		3f800000
NR3[31:0]	00000000		00000000	
M IXR4[31:0]	3£800000	00000000		3f800000
M IXR5[31:0]	00000000		00000000	
NR6[31:0]	00000000		0000000	3f800000
1XR7[31:0]	00000000		0000000	bf80000
KI0[31:0]	3f800000	00000000	3f800000	0000000
M IXI1[31:0]	00000000		0000000	k bf80000
M IXI2[31:0]	00000000		0000000	x 3f80000
M IXI3[31:0]	00000000		00000000	
M IXI4[31:0]	00000000		00000000	
M IXI5[31:0]	00000000		0000000	k bf80000
XI6[31:0]	00000000		00000000	
M IXI7[31:0]	00000000		00000000	
zr0[31:0]	3e800000	3e000000	3e800000	3ec0000
W zr1[31:0]	be000000	3e000000	be000000	be5a7el
zr2[31:0]	00000000	3e000000	00000000	3e8000
zr3[31:0]	be000000	3e000000	be000000	3e5a7el
zr4[31:0]	3e800000	3e000000	3e800000	3f20000
zr5[31:0]	be000000	3e000000	be000000	bd1604:
W zr6[31:0]	00000000	3e000000	00000000	be80000
zr7[31:0]	be000000	3e000000	be000000	3d1604
🖌 zi0[31:0]	3e000000	00000000	3e000000	be0000
zi1[31:0]	3e800000	00000000	3e800000	3db4fdi
zi2[31:0]	3e000000	00000000	3e000000	000000
👹 zi3[31:0]	00000000	00000000	00000000	3db4fdi
zi4[31:0]	3e000000	00000000	3e000000	3ec0000
z5[31:0]	3e800000	00000000	3e800000	bdb4fd
zi6[31:0]	3e000000	00000000	3e000000	be80000
207[31:0]	00000000	00000000	00000000	bdb4fdf

Simulation results of



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Fig 14: Simulation results of PISO

		782.638 rs
Name	Value	1,000 ns 1,000 ns 1000 ns 11,000 ns 11,000 ns 11,200 ns
light	1	
lint	0	
Sett 1	3+000000	
M at[31:1]	00000000	
📲 q1[31:0]	00000000	
N (2315)	be800000	
1 at[111]	befafeta	
M a4(11.5)	32000000	
N a5[31.5]	3e000000	
Madital	00000000	
Ma7316	34531740	
101116	00000000	
M adated	00000000	
Matual	20000000	
Materia	1+00000	
Madad	1+000000	
Mated	3-000000	
Madad.	34034545	
M salara	34300000	
in the second se	3000000	
and the state		
W meat/rai	0000000	
lig vaid	1	
ig en_trate	0	
<b>W</b> led[31:0]	00111301010	199999999999999999999999999999999
<b>W</b> (40)	7	
M a[4:0]	13	131456739000000000000000000000000000000000000

Fig15: Simulation results of SIPO

lame	Value	0 ns	500 ns		1,000 ns		1,500 n	s	2,00	Ons	12,500 ns		3,000
la ck	1			MERIL	UNIVERSITY		L. MIL		mn	NAMANAN	LING CONTRACTOR	USIAA	
la rst	1	1							-			_	
• 🚮 qr0[31:0]	00000000	000000	00	$\Sigma$	3e800000	0000	0000	3e80000		3ec00000	be000000	X	3ec0000
<b>ar</b> 1[31:0]	00000000	000000	00	<u>)</u>	3e000000	( be9a	7efa	bd96041		be9a7efa	be34fdf4	X	beb4fd
<b>W</b> qr2[31:0]	00000000	000000	00	X	3e800000	(3f00	0000	3e80000			3e000000		
<b>Ref</b> qr3[31:0]	00000000	000000	00	X	3d53f7d0	3e69	fbe8	be34fdf4		3d53f7d0	be800000		Be34Fd
<b>ar4[31:0]</b>	00000000	( 000000	00		3f000000	$\langle -$	be80	0000		be000000	3e	00000	á –
<b>ar5[31:0]</b>	00000000	000000	00		3e000000	3d53	7d0	beda7efa		3d53f7d0	3e34fdf4	X	Beb4fo
💐 qr6[31:0]	00000000		00000000				3e80	0000		3e000000	Х Зе	:0000	4
<b>Ref</b> qr7[31:0]	00000000	000000	00	X	be9a7eFa	bef4	fdf4	3e34fdf4		be9a7efa	be800000	X	be34fr
<b>ngi</b> qi0[31:0]	00000000	000000	00		be80	0000		0000000		be0	00000	X	3e0001
<b>a</b> i1[31:0]	00000000	000000	00		be9a7efa	( be00	0000	be34fdf4		bd53f7d0	00000000	X	d960-
<b>a</b> [31:0]	00000000	000000	00		3F000000	$\square$	0000	0000		bec00000	3ec00000	X	e000
ni3[31:0]	00000000	000000	00	$\Sigma$	3e000000	( 3d53	7d0	beda7efa		bf0d3f7d	beda7efa	20	e800
<b>ai4[31:0]</b>	00000000			0	0000000					be000000	bec00000		e000
<b>ng</b> q5[31:0]	00000000	000000	00		3d53f7d0	( be00	0000	3e34fdf4		3e9a7efa	00000000	20	beda7
Ng qi6[31:0]	00000000	000000	00	$\supset$	be80	0000		bf000000		3e000000	bec00000	X	e000
<b>a</b> 7[31:0]	00000000	000000	00		3e000000	be9a	7efa	bd96041		be4b020c	bd960418	X	3e800
Marco [31:0]	00000000	000000	00	X	3F800000	0000	0000	0000000		00000000	00000000		3f800
<b>11</b> oxr1[31:0]	00000000	000000	00	X	391e5000	( 391e	5000	3f800000		bf7fec36	391e5000	X	91e5
<b>11</b> oxr2[31:0]	00000000	000000	00	$\supset$	00000000	bf80	0000	0000000		3f800000	00000000		6f8001
<b>11</b> oxr3[31:0]	00000000	000000	00	$\supset$	6F800000	3f7h	ec36	bf7fec36		3f800000	bf800000		Sf7fe
<b>1</b> oxr4[31:0]	00000000	000000	00		3f800000	3f80	0000	3f800000		3f800000	3f800000		3f8001
<b>11</b> oxr5[31:0]	00000000	000000	00		3f7ff61b	3171	61b	3f800000		3f7fec36	3f7ff61b	X	Sf7ff6
nxr6[31:0]	00000000	000000	00	$\overline{x}$	3F800000	bf80	0000	bf800000		bf800000	bf800000	X	3f8001
nxr7[31:0]	00000000	000000	00	X	6F800000	bf7f	ec36	3f7fec36		3f800000	bf800000	X	bf7fei
axi0[31:0]	00000000	000000	00	X	00000000	bf80	0000	bf800000		bf800000	bf800000	X	0000
nxi1[31:0]	00000000	000000	00	$\Sigma$	of7ff61b	bf7f	61c	0000000		00000000	3f7ff61b	X	3f7ffe
nxi2[31:0]	00000000	( 000000	00		6f800000	0000	0000	3f800000		00000000	bf800000	20	00000
nxi3[31:0]	00000000	000000	00	X	00000000	0000	0000	0000000		00000000	00000000	X	0000
Dirite 131:01	00000000	000000	00	V	00000000	0000	000	0000000	Ev	00000000	00000000	V	0000

Fig 16: Simulation results of FFT

Name	Value	0.ns 500.ns	1,000 ns	1,500 m	F. P	00 ns	2,500 ns	B,000 r
• 📲 ==[111]	00000000	concepto	) 39800000	00000000	00000000	00000000	00000000	390000
m[na]	00000000	00000000	) 191e5000	391,45000	3/500000	billeció	391e5000	3160
Pingasi .	00000000	0000000	( 0000000	5Headacoo	1000000	3900000	( 0000000 )	\$180000
M state		100000	\$F800000	379636	billeciti	3900000	54800000 )	27iec3
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Fig 17: simulation results of QPSK Deframer



Fig 18: simulation results of Despreader

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## **IV. CONCLUSION AND FUTURE WORK**

The objective is the implementing the core processing blocks of an Orthogonal Frequency Division Multiplexing (OFDM) system, namely the Fast Fourier Transform (FFT) and Inverse Fast Fourier Transform (IFFT). The Fast Fourier Transform (FFT) and Inverse Fast Fourier Transform (FFT) have been chosen to implement the design instead of the Discrete Fourier Transform and Inverse Discrete Fourier Transform because they offer better speed with less computational time. These methods requires the odd and even samples inputs are process separately before they are combine to give the final output. The result of the computation is in integer bits which might comprises of real and imaginary components. The decimal value of the output if greater than 0.5 is approximated to 1 and vice versa. The design implementation is done using VHDL coding. Direct mathematical method is adopted because it is an efficient and optimized method instead of the structural implementation which is based on butterfly operation.

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