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High Performance NP Dynamic Adder Circuit with Carbon NANO Tube Technology

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Abstract:

Low-power, compact, and high-performance NP dynamic CMOS circuits are presented in this paper assuming a 16 nm carbon nano tube transistor technology. The performances of two-stage pipeline 32-bit carry lookahead adders are evaluated based on HSPICE simulation with the following four different implementations: silicon MOSFET (Si-MOSFET) domino logic, Si-MOSFET NP dynamic CMOS, carbon nanotube MOSFET (CN-MOSFET) domino logic, and CN-MOSFET NP dynamic CMOS. While providing similar propagation delay, the total area of CN-MOSFET NP dynamic CMOS adder is reduced by 35.53%, 77.96%, and 15.52% as compared to the Si-MOSFETdomino, Si-MOSFET NP dynamic CMOS, and CN MOSFET domino adders, respectively. Miniaturization of the CN-MOSFET NP dynamic CMOS circuit reduces the dynamic switching power consumption by 80.54%, 95.57%, and 25.66% as compared to the Si-MOSFET domino, Si-MOSFET NP dynamic CMOS, and CN-MOSFET domino circuits, respectively. Furthermore, the CN-MOSFET NP dynamic CMOS adder provides up to 99.98% savings in leakage power consumption as compared to the other adder circuits that are evaluated in this study.

Keyword:

Carbon based electronics, carbon nanotube transistor technology, domino logic, dynamic logic, electron mobility, high performance, hole mobility, low power.

I.INTRODUCTION:

Dynamic CMOS circuits are commonly employed for-enhanced propagation speed on the critical signal paths of microprocessors [1]–[9]. Inputs are evaluated with a network that is composed of only NMOS transistors in an n-type dynamic CMOS gate (see Fig. 1(a)).

Alternatively, in a p-type dynamic CMOS circuit (see Fig. 1(c)), the inputs are evaluated with a network of PMOS transistors. N-type dynamic CMOS gates are preferred for smaller silicon area and lower power consumption in traditional silicon-based integrated circuits [1]–[3], [5]–[9]. An n-type dynamic logic gate produces a monotonically falling output. N-type dynamic CMOS circuits however require monotonically rising inputs for proper operation. The output of an n-type dynamic logic gate therefore cannot directly drive the inputs of other n-type dynamic gates [5]. Two different techniques exist to satisfy the monotonicity requirement in dynamic circuits: the domino logic circuit technique and NP dynamic CMOS circuit technique [4], [5]. The domino logic circuit technique satisfies the monotonicity requirement by placing a static CMOS inverter between two successive n-typedynamic logic gates as show in Fig. 1(b). Alternatively, an NP dynamic CMOS circuit is formed by cascading alternating n-type and p-type dynamic logic gates as shown in Fig. 1(d).For proper operation, p-type dynamic CMOS circuits require monotonically falling inputs. The output of an n-type dynamic logic gate can therefore directly drive the input of a p-type dynamic logic gate. Furthermore, a p-type dynamic CMOS gate produces a monotonically rising output. Cascading alternating stages of n-type and p-type dynamic logic gates therefore satisfies the monotonicity requirements of inputs in dynamic CMOS circuits. In NP dynamic CMOS logic circuits, static CMOS inverters on the critical data propagation path are avoided, thereby reducing the propagation delay as compared to standard domino logic circuits [4]. The NP dynamic CMOS circuits however typically consume high power and occupy large area when implemented with the conventional silicon MOSFETs. The mobility of holes is substantially lower as compared to electrons in silicon. In order to provide similar evaluation speed, the sizes of p-channel Si-MOSFETs are enlarged in the pull-up transistor networks of p-type dynamic logic gates as compared to the sizes ofn-channel devices in the pull-down transistor networks of n-type dynamic gates.

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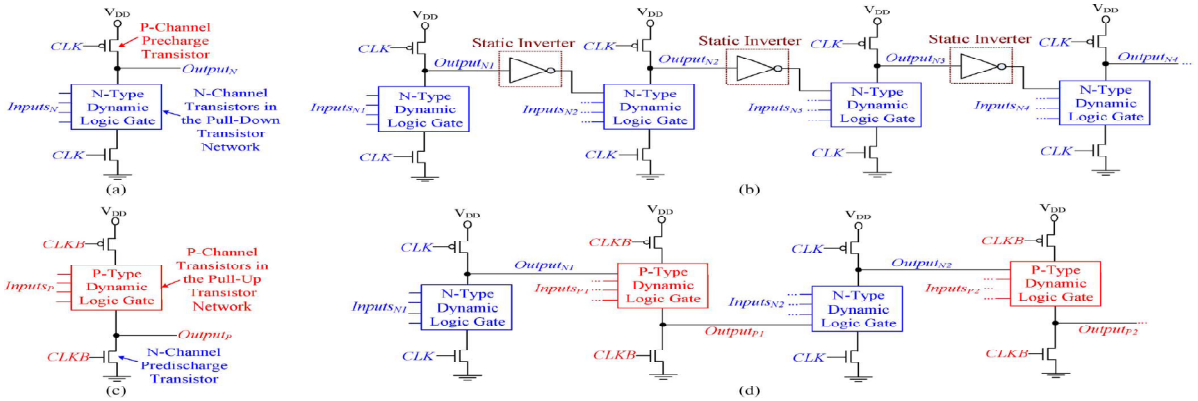
The area and power consumption overheads are therefore significant in NP dynamic CMOS circuits with the conventional silicon CMOS technology. Furthermore, as the CMOS technology is scaled into the sub-22 nm regime, the short-channel



effects and subthreshold leakage currents of Si-MOSFETs are increased. With the scaling of Si-MOSFET technology, the reliability of CMOS circuits is degraded while the power consumption is increased [1], [10], [11]. Reducing power consumption and miniaturizing silicon area while providing high data processing speed are currently important challenges in dynamic CMOS circuits [1]–[3], [10].Alternative materials and devices are needed to extend the scaling of CMOS technology. Carbon nanotube MOSFETs (CN-MOSFETs) display desirable characteristics such as higher carrier mobility and smaller device footprint (area) as compared to the conventional Si-MOSFETs [12]–[17]. While moving along a carbon nanotube, electrons and holes display near ballistic transport with similar mobilities [15]. N-channel and p-channel CN-MOSFETs with identical physical dimensions therefore produce similar active currents in a carbon nanotube transistor technology [13]–[15].The evaluation speed of a p-type CN-MOSFET dynamic gate is comparable to the same sized n-type CN-MOSFET dynamic gate. The well-known area and power consumption disadvantages of NP dynamic CMOS circuits are therefore eliminatedby employing a carbon nanotube transistor technology. The NP dynamic CMOS logic family can be thereby rejuvenated as a better alternative to the conventional domino logic for the implementation of future high speed digital integrated circuits with carbon nanotube transistors. In this paper, low power, compact, and high performance NP dynamic CMOS circuits with carbon nanotube transistors are presented. The paper is organized as follows. Device profiles of high-performance complementary CN-MOSFETs with 16 nm channel length are presented in Section II.

To demonstrate the advantages of NP dynamic CMOS circuit technique as compared to the domino logic circuit technique, 32-bit carry lookahead adders (CLAs) are designed with carbon nanotube transistors. The adder circuits are described in Section III. The performances of the Si-MOSFET and CN-MOSFET adders are compared in Section IV. Finally, some conclusions are offered in Section V.

II. HIGH-PERFORMANCE COMPLEMENTARY CN-MOSFETS:

The physical parameters of high-performance n-channel and p-channel CN-MOSFETs are presented assuming a 16 nm CMOS technology in this section. The active currents (Ion), subthreshold leakage currents (Ioff), overall switch performance (Ion/ Ioff), and subthreshold slopes of CN-MOSFETs are compared with the minimum sized bulk Si-MOSFETs. The 16 nm Predictive Technology Model for high-performance from the Arizona State University (PTM HP [18]) is used to evaluate the Si-MOSFETs. Alternatively, the evaluation of CN-MOSFETs is based on the Stanford University CN-MOSFET HSPICE compact model [19]–[21].

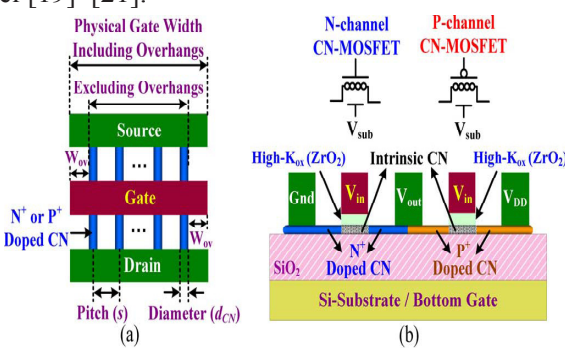


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Fig.2: (a) Top-view of a CN-MOSFET. (b) Cross sectional view of a static CMOS inverter with CN-MOSFETs.

Circuit symbols of n-channel and p-channel CN-MOSFETs are indicated. The source/drain contact material: Chromium/Aurum (Cr/Au). The gate material: Platinum/Aurum (Pt/Au) [24].The full set of physical parameters of 16 nm CN-MOSFETs is presented in [12]. Due to the high switching activity factor (α), power consumption of dynamic CMOS circuits are typically high [2], [3], [5], [22]. Dynamic CMOS circuits therefore tend to be located at or near the hot-spots in typical microprocessors [2], [3]. The die temperature is assumed to be 900C (a typical hot-spot temperature in current multi-core high-performance microprocessors [23]) in this study. The channel lengths of all the transistors are 16 nm (Lg =16nm) in this study. The power supply voltage (VDD) is 0.7 V [12]–[14].

The top view of a CN-MOSFET is shown in Fig. 2(a). The carbon nanotubes (CNs) are heavily doped with donors (for n-channel) or acceptors (for p-channel) in the source and drain extension regions of a CN-MOSFET. The carbon nanotubes are undoped under the gate. Nanotube diameter and nanoarray pitch determine the performance and area of a carbon nanotube transistor [12]–[14]. N-channel CN-MOSFETs with uniform nanotube diameter (dCN) and uniform nanoarray pitch (s) values that are suitable for VLSI are presented in [13]. A complementary study for p-channel carbon nanotube transistors with uniform diameter and pitch is provided in [14]. The optimum uniform diameter is 0.84 nm with a uniform pitch of 5.3 nm in both n-channel and p-channel CN-MOSFETs for achieving high performance while maintaining high integration density in 16 nm technology node [13], [14].

The substrate acts as a second (bottom) gate below the thick oxide layer in a CN-MOSFET [12]–[14]. The substrate is shared by both n-channel and p-channel CN-MOSFETs in an integrated circuit as illustrated in Fig. 2(b). A substrate bias voltage that is half of the power supply voltage (Vsub = VDD/ 2= 0.35V) is employed for producing similar active currents with the n-channel and p-channel CN-MOSFETs in this study. A substrate bias voltage of 0.35 V, a uniform diameter of 0.84 nm, and a uniform pitch of 5.3 nm are assumed for all the CN-MOSFETs in this study. In the on-state, the charge induced on the nanotubes that form the channel array of a multi-tube CN-MOSFET interact [12].

Charge screening reduces the effective width of the channel, thereby degrading the device current. The active current that is produced by a CN-MOSFET is not directly proportional to the number of tubes (N) due to the charge screening effect in the carbon nanotube channel array [12], [20], [25].The total area of a CN-MOSFET is determined by the physical gate width (Wg) [12]. (Wg) is [12] (Cr/Au). The gate material: Platinum/Aurum (Pt/Au) [24]. Wg (including overhangs)= s* (N-1)+dCN +2* Wov (1)where s is the uniform array pitch, N is the number of tubes in a CN-MOSFET, dCN is the uniform nanotube diameter, and Wov is the overhang width of the gate from the edge of CN array as shown in Fig. 2(a). In a Si-MOSFET, the overhang width ofthe gate from the edge of active region is typically 2λ [26]. Assuming a similar photolithographic manufacturing process for the carbon-nanotube transistors Wov, at each end is assumed to be 2λ (16 nm) in this study. From (1), the physical gate width (including the overhangs) of a minimum sized CN-MOSFET with only one nanotube in the channel is dCN + 2*Wov= 32.84nm. Alternatively, the minimum channel width of active region under the gate of a Si-MOSFET is assumed to be 3λ according to the photolithographic manufacturing process [26].

III. 32-BIT CARRY LOOKAHEAD ADDERS WITH NP DYNAMIC CMOS AND DOMINO LOGIC CIRCUIT TECHNIQUES:

Carry lookahead adders (CLAs) are commonly used in modern processors [2], [3]. To demonstrate the advantages of NP dynamic CMOS circuit technique as compared to the domino logic circuit technique in a carbon nanotube transistor technology, two 32-bit carry lookahead adders are described in this section. The adders are designed as two-stage pipelines for high speed operation. For a fair comparison, each pipeline stage contains 5 levels of dynamic logic gates and 5 levels of domino logic gates in the NP dynamic CMOS and domino adders, respectively.

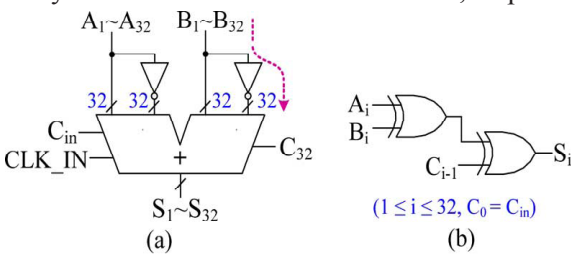

Fig.3: (a) Symbol of a 32-bit carry lookahead adder. (b) Sum generator for the NP dynamic CMOS and domino logic CLAs.

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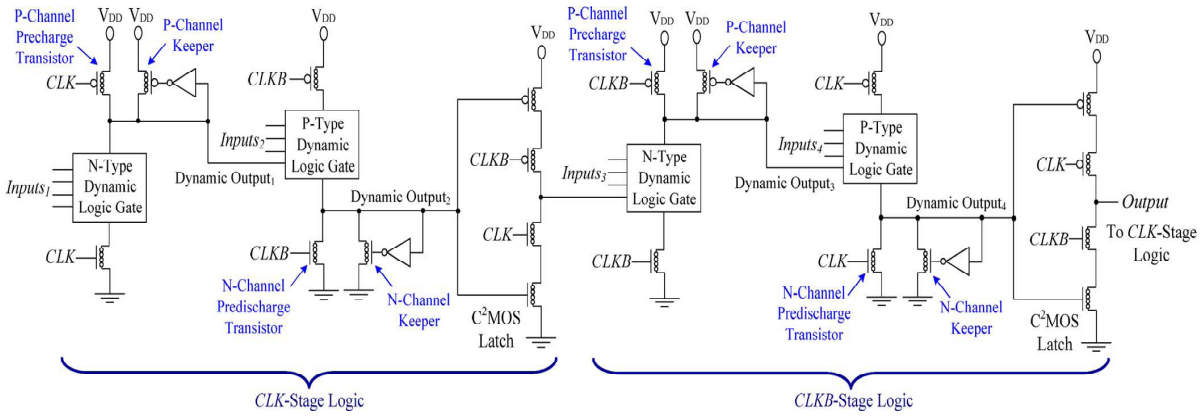
The input vectors of a 32-bit CLA are denoted as A (A0 to A32) and B(B0 to B32) as shown in Fig. 3(a). The carry input and clock input of the adder are denoted as Cin and CLK_IN , respectively. The sum output and carry output for each bit position i (1≤i≤32) are denoted as Si and Ci , respectively. The carry output of the 32-bit CLA is C32 as illustrated in Fig. 3(a). Since the sum outputs (S1 to S32) are not on the critical propagation delay path, each sum bit Si is produced by two static CMOS XOR gates as shown in Fig. 3(b). The structures of the adders with NP dynamic CMOS and domino logic circuit techniques are presented in Sections III-A and III-B, respectively.

A. NP Dynamic CMOS Adder:

An NP dynamic CMOS circuit is formed by cascading alternating n-type and p-type dynamic logic gates as illustrated in Fig. 1(d). The NP dynamic CMOS logic circuits are used to implement race-free pipelines [4].

In a multi-stage NP dynamic CMOS pipeline, a CLK-stage is preceded and followed by a CLKB -stage as illustrated in Fig. 4. In the CLK -stage, the precharging and evaluation of the n-type dynamic logic gates are controlled by the true phase of the clock signal CLK. Alternatively, the predischarging and evaluation of the p-type dynamic logic gates are controlled by the inverted clock signal CLKB. In the CLKB-stage, CLK and CLKB signals are interchanged as compared to the CLK-stage as shown in Fig. 4.To form an NP dynamic CMOS pipeline with proper operation, the output information of each stage should be held constant during the evaluation of the following pipeline stage. Clocked CMOS (C2MOS) latches are used to store the output information of each stage, thereby guaranteeing race free operation in an NP dynamic CMOS circuit [4] as illustrated in Fig. 4.The 32-bit carry generator of the NP dynamic CMOS adder is shown in Fig. 5(a). The first level of each pipeline stage is composed of 16 n-type



footed dynamic propagate (P) and 16 n-type footed dynamic generate (G) circuits. The dynamic propagate and generate circuits are shown in Fig. 5(c). The propagate and generate circuits are followed by alternating p-type and n-type footless dynamic 4-bitmultiple-output carry generators [9], [28] as shown in Fig. 5(a). The n-type and p-type carry generators are illustrated in Fig. 6(a) and (b), respectively.The clock signals are properly delayed to eliminate the short-circuit current paths at each level of footless dynamic logic gates. The circuit that is used to generate the CLK and complementary CLKB is shown in Fig. 5(b). The clock input is a 1.5 GHz square wave with 50% duty cycle. Transmission gate is used as a delay element to control the skew between CLK and CLKB.

The enable signal (EN) is maintained high during the active mode. Alternatively, EN is gated low to disable the local clock signals (CLK and CLKB) in the idle mode. The operation of the NP dynamic CMOS adder is as follows. When the clock signal CLK is low, the complementary clock signal CLKB is high. The CLK pipeline-stage is in precharging/predischarging phase, while the CLKB pipeline-stage is in evaluation phase. In the CLK-stage, the dynamic nodes (P1_b~ P16_b , G1_b~ G16_b, C5_b~ C8_b, and C13_b~ C16_b) of the n-type dynamic logic gates are precharged to VDD through the corresponding p-channel precharge transistors. Alternatively, the dynamic nodes (C1~ C4 and C9~ C12) of the p-type dynamic logic gates are predischarged to 0 V through the n-channel predischarge transistors.

ISSN No: 2348-4845
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The C2MOS latch at the end of the CLK-stage is opaque. The output information (C16_b') of the CLK-stage is therefore held constant by the C2MOS latch during the evaluation of the following CLKB-stage. In the CLKB pipeline-stage, the inputs of the dynamic gates are evaluated. If the pull-down transistor networks of the n-type dynamic logic gates are turned off by the corresponding input vectors, the dynamic outputs (P17_b~ P32_b , G17_b~ G32_b, C21_b~ C24_b, and C29_b~ C32_b) are maintained at VDD by the p-channel keepers. Alternatively, the dynamic outputs are discharged if the pull-down transistor networks of the n-type logic gates are activated. Similarly, the dynamic outputs (C17~ C20 and C25~ C28) are maintained at 0 V by the n-channel keepers provided that the pull-up transistor networks of p-type dynamic gates are cut off. Alternatively, the dynamic nodes are charged to VDD if the pull-up transistor networks of the p-type logic gates are activated. The C2MOS latch at the end of the CLKB-stage is transparent. The carry output of the 32-bit CLA (C32) is determined by A17 ~ A32, A17_ b ~ A32_b, B17 ~ B32, B17_ b ~ B32_b and C16_b' .The sum outputs S17 to S32 are determined by A17 ~A32, A17_ b ~ A32_b, B17 ~ B32, B17_ b ~ B32_b and C16 ~ B31 and B16_ b' ~ C31_b. Subsequently, when CLK and CLKB transition to high and low, respectively, the inputs of the dynamic gates in the CLK -stage are evaluated while the CLKB-stage is inprecharging/ pre-discharging phase. The latch at the end of the CLK -stage becomes transparent while the C2MOS latch at the end of the CLKB -stage is opaque. The output of the C2MOS latch in the CLKB -stage is determined by the inputs A1~ A16, A1_ b ~ A16_b, B1 ~ B16, B1_ b ~ B16_b and Cin'. The sum outputs S1 to S16 are determined by A1~ A16, A1_ b ~ A16_b, B1 ~ B16, B1_ b ~ B16_b ,Cin~ C15 and Cin_b~ C15_-b.

B. Domino Logic Adder:

The 32-bit carry generator of the two-stage pipeline CLA that is implemented with the conventional domino logic circuit technique is shown in Fig. 7. Domino logic circuits are typically constructed with n-type dynamic gates due to the higher electron mobility as compared to the hole mobility in silicon CMOS technology. For a fair comparison with the silicon transistor technology, the CN-MOSFET domino adder is also composed of only n-type dynamic gates in this study. The clock signals are properly delayed to eliminate the short-

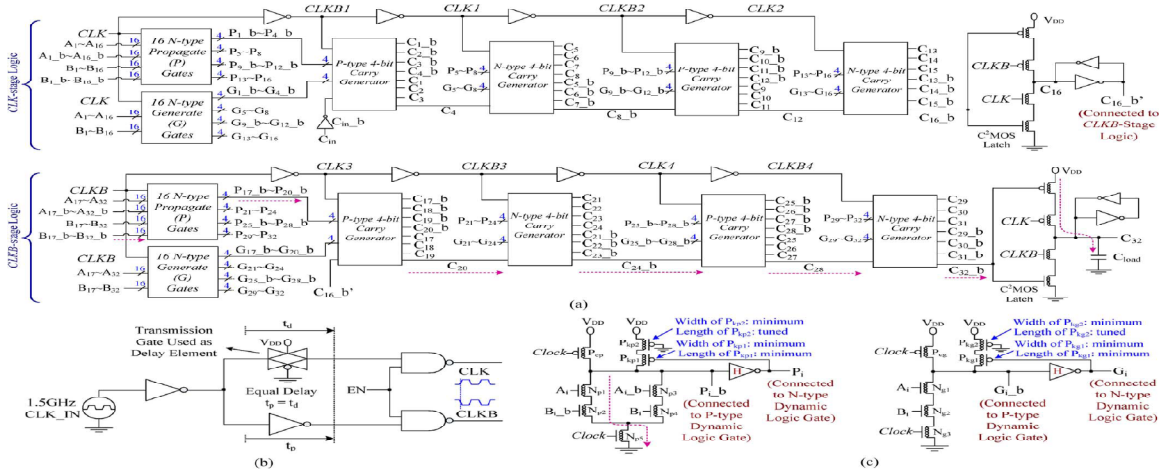

Fig.5: Various components of two-stage pipeline 32-bit carry lookahead adders. (a) 32-bit carry generator of the NP dynamic CMOS CLA. (b) 'CLK' and 'CLKB' signals generator for the NP dynamic CMOS and domino logic adders. 'EN' is enable signal (active high). (c) N-type footed dynamic propagate (Pi) and generate (Gi) circuits. For Si-MOSFET technology: WNp1 = WNp2= WNp3 = WNp4= WNp5= WNg1= WNg2= WNg3≈4 WPcp=4 WPcg. W: the physical gate width excluding the overhangs of a Si-MOSFET. For CN-MOSFET technology: NNp1 = NNp2= NNp3 = NNp4= NNp5= NNg1= NNg2= NNg3≈6 NPcp=6NPcg.. N: the number of tubes in a CN-MOSFET. The critical propagation delay paths are illustrated with dashed lines.

ISSN No: 2348-4845
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circuit current paths at each level of footless n-type dynamic CMOS gates [1] as shown in Fig. 7. The operation of the domino logic CLA is similar to the NP dynamic CMOS CLA.

IV. COMPARISON OF NP DYNAMIC CMOS AND DOMINO LOGIC CIRCUITS WITH CARBON NANOTUBE AND SILICON TRANSISTOR TECHNOLOGIES:

In this section, the propagation delay, total transistor area, dynamic switching power consumption, and leakage power consumption of adders with the following four different implementations are evaluated and compared: Si-MOSFET domino logic, Si-MOSFET NP dynamic CMOS, CN-MOSFET domino logic, and CN-MOSFET NP dynamic CMOS. The adders are designed to operate with a 1.5 GHz clock. The transistor sizing for achieving similar propagation delay with the four adders is presented in Section IV-A. The total transistor area, dynamic switching power consumption, and leakage power consumption of the adders are compared in Sections IV-B to IV-D.

A. Transistor Sizing in Dynamic Adders:

For all of the four adders, the transistors are sized to achieve similar (within 2%) propagation delay along the critical signal paths. The load capacitors at sum outputs (S1 to S32) and carry output (C32) are assumed to be 0.25 fF (which is equal to the gate capacitance of a Si-MOSFET inverter that is 4 larger as compared to the minimum sized un-skewed static CMOS inverter).

The physical gate widths (including the overhangs) of Si-MOSFETs in the minimum sized un-skewed static CMOS inverter are: WPMOS = 74nm and WNMOS = 56nm . Precharge and predischarge delays are not critical in dynamic CMOS circuits [1], [4], [5]. Alternatively, the delays of the worst-case pull-down paths of the n-type dynamic logic gates and the worst-case pull-up paths of the p-type dynamic logic gates are critical in determining the evaluation speed of a dynamic CMOS circuit.

The critical evaluation (discharge) path of the n-type dynamic 4-bit carry generator is along the Nd5 ~ Nd9path as illustrated in Fig. 6(a). Alternatively, the critical evaluation (charge) path of the p-type dynamic 4-bit carry generator is along the Pu5 ~ Pu9 path as shown in Fig. 6(b). In every dynamic gate, the precharge or predischarge device is sized to provide approximately half [5] of the strength of the worst-case evaluation path. In the domino logic adders, the output static CMOS inverter of each domino gate is high-skewed since the high-to-low transition of domino output is not critical.

The size of the n-channel transistor in each output static CMOS inverter is tuned to have approximately half of the strength of the p-channel device. The keeper in each dynamic logic gate is designed to provide approximately 10% [5] of the strength of the worst-case pull down (for n-type dynamic gate) or pull-up (for p-type dynamic gate) transistor stack. For small dynamic gates, the keeper is weaker than the minimum sized transistor. The weak keeper is composed of two transistors that are connected in series [5] as shown in Figs. 5(c) and 6.

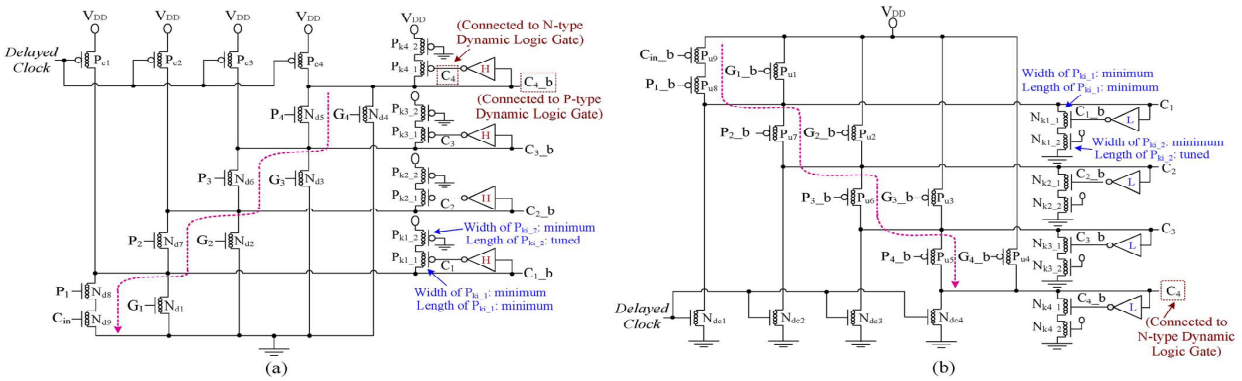

Fig.6: 4-bit multiple-output carry generators. (a) N-type footless dynamic 4-bit multiple-output carry generator. For Si-MOSFET technology: 2WNd1 = 3WNd2 = 4WNd3 = 5WNd4 = WNd5 = WNd6 = WNd7 = WNd8 = WNd9, 2WPc1 = 3WPc2 = 4WPc3 = 5WPc4, WNd4≈ 1.5 WPc4. For CN-MOSFET technology: 2NNd1 ≈ 3NNd2 ≈ 4NNd3 ≈ 5NNd4 ≈ NNd5 = NNd6 = NNd7 = NNd8 = NNd9, 2NPc1 ≈ 3NPc2 ≈ 4NPc3 ≈ 5NPc4, NNd4≈ 2 NPc4 ,

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(b) P-type footless dynamic 4-bit multiple-output carry generator. For Si-MOSFET technology: 2WPu1 = 3WPu2 = 4WPu3 = 5WPu4 = WPu5 = WPu6 = WPu7 = WPu8 = WPu9, 2WNdc1 = 3WNdc2 = 4WNdc3 = 5WNdc4, WPu4≈ 8 WNdc4. For CN-MOSFET technology: 2NPu1 ≈ 3NPu2 ≈ 4NPu3 ≈ 5NPu4 ≈ NPu5 = NPu6 = NPu7 = NPu8 = NPu9, 2NNdc1 ≈ 3NNdc2 ≈ 4NNdc3 ≈ 5NNdc4, NPu4≈ 2 NNdc4. The critical propagation delay paths for C4 _b and C4 are illustrated with dashed lines.

The longest propagation delay path is observed for the C32 output in all four adders. The propagation delay path for C32 is excited with (Cin, A, B) = (1,FFFFFFFF, 00000000) when the enable signal EN is high. The propagation delay of C32 is the time interval from 50% high-to-low transition of the clock input CLK_IN (CLKB transitions from low to high) until the carry output C32 is pulled up to VDD/2 from 0. The critical propagation delay paths of the NP dynamic CMOS and domino logic adders are illustrated with dashed lines in Figs. 5(a) and 7, respectively, assuming (Cin, A, B) = (1,FFFFFFFF, 00000000). The design criteria for the conventional Si-MOSFET domino adder are described next. The precharge devices are minimum sized in all of the n-type dynamic gates. The strengths of the worst-case pull-down paths of all the n-type gates are tuned to provide approximately twice [5] the strengths of the precharge devices. The physical gate widths (including the overhangs) of n-channel transistors along the worst-case pull-down path of each n-type dynamic gate in the Si-MOSFET domino adder are listed in Table IV. Both CLK- and CLKB-stages are ended with the same sized C2MOS latches. The propagation delay for C32 is 302 ps in the Si-MOSFET domino adder.For a fair comparison, the transistor sizes of the Si-MOSFET NP dynamic CMOS CLA are tuned to achieve similar propagation delay as compared to the Si-MOSFET domino logic adder. In the 32-bit carry generator of Si-MOSFET NP dynamic CMOS adder, the required physical gate widths (including the overhangs) of Si-MOSFETs along the worst-case pull-down path of each n-type dynamic gate and the worst-case pull-up path of each p-type dynamic 4-bit carry generator are listed in Table I. The mobility of holes is substantially lower as compared to electrons in silicon. In order to provide similar evaluation speed with the n-type and p-type dynamic carry generators, the p-channel Si-MOSFETs (Pu5 ~ Pu9 : 1880 nm) are enlarged as compared to the n-channel Si-MOSFETs (Nd5 ~ Nd9 : 944 nm) as listed in Table IV. The NMOS transistors in the n-type dynamic gates are sized sufficiently wide to be able to drive the huge PMOS transistors of the following p-type dynamic gates while satisfying the propagation delay goal. The transistors are therefore significantly larger in the Si-MOSFET NP dynamic CMOS adder as compared to the Si-MOSFET domino adder, as listed in Table I. The propagation delay for C32 is 306 ps in the Si-MOSFET NP dynamic CMOS CLA. The numbers of tubes are tuned to achieve similar propagation delay with the CN-MOSFET domino logic CLA as compared to the Si-MOSFET circuits. The required numbers of tubes and physical gate widths (including the overhangs) of n-channel CN-MOSFETs along the worst-case pull-down path of each n-type dynamic logic gate are listed in Table IV.The propagation delay for C32 is 301 ps in the CN-MOSFET domino adder.The numbers of tubes are also tuned in the CN-MOSFET NP dynamic CMOS CLA in order to

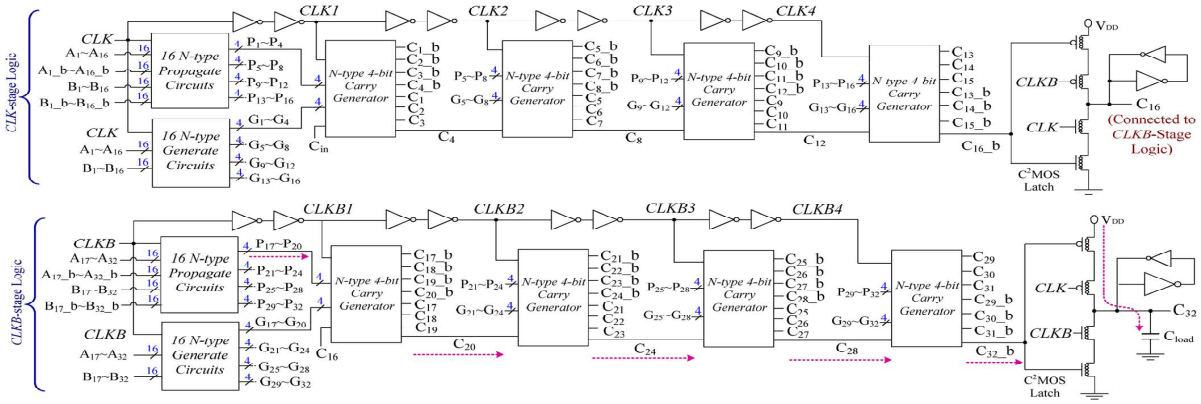

Fig.7: 32-bit carry generator of the domino logic CLA. The critical propagation delay paths are illustrated with dashed lines.

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provide similar propagation delay as compared to the Si-MOSFET circuits. The required numbers of tubes of transistors are listed in Table I. Unlike the conventional silicon CMOS technology, electrons and holes have similar mobilities in the carbon nanotube transistor technology [15]. As listed in Table I, the required numbers of tubes of p-channel CN-MOSFETs (Pu5 ~ Pu9) are therefore equal to the n-channel CN-MOSFETs (Nd5 ~ Nd9) in the multiple-output carry generators. The propagation delay for C32 is 299 ps in the CN-MOSFET NP dynamic CMOS CLA.Unlike the CN-MOSFET domino circuit, the static CMOS inverters are avoided on the critical propagation delay path of the CN-MOSFET NP dynamic CMOS CLA. The required numbers of carbon nanotubes are thereby reduced and the transistor sizes are miniaturized in the CN-MOSFET NP dynamic CMOS adder as compared to the CN-MOSFET domino logic adder, when the two circuits are designed for similar propagation delay, as listed in Table I.

B. Overall Transistor Area:

The area of an adder is a rough estimate based on the summation of the area of each individual transistor in the circuit (∑[physical gate width x channel length]). The mobility of holes is substantially lower as compared to electrons in silicon. In order to provide similar propagation delay, the sizes of transistors are significantly enlarged in the p-type dynamic logic gates of the NP dynamic CMOS adder with the conventional silicon transistor technology. The cumulative transistor area of the Si-MOSFET NP dynamic CMOS adder is therefore 2.92 x larger as compared to the Si-MOSFET domino logic circuit as listed in Table I. Furthermore, there are no static CMOS inverters on the critical data propagation path of the NP dynamic CMOS adder. The cumulative transistorarea of the CN-MOSFET NP dynamic CMOS circuit is therefore reduced by 15.52% while providing similar propagation delay as compared to the CN-MOSFET domino logic circuit as listed in Table I.

C. Dynamic Switching Power Consumption:

The dynamic switching power consumption of the four adders is measured for (Cin, A, B)=(1,FFFFFFFF, 00000000) when the enable signal (EN) is high. The dynamic output switching power consumption is

$$P_{dynamic} = \alpha C_L V_{DD}^2 f \qquad (2)$$

Where $\alpha(0 \le \alpha \le 1)$ is the switching activity factor, CL is the capacitive load at the dynamic output, and is the clock frequency. Since the dynamic output needs to be charged and discharged every clock cycle, the activity factor α is maximized (α=1) with (Cin, A, B)=(1,FFFFFFFF, 00000000). Due to the smaller sizes of transistors in the CN-MOSFET NP dynamic CMOS CLA as listed in Table I, the parasitic capacitors at the dynamic nodes are also smaller as compared to the other adders. As listed in Table I, the dynamic switching power consumption of the CN-MOSFET NP dynamic CMOS CLA is 80.54%, 95.57%, and 25.66% lower as compared to the Si-MOSFET domino logic, Si-MOSFET NP dynamic CMOS, and CN-MOSFET domino logic adders, respectively.The simulation of the proposed designs is carried out by using H-Spice tool. The simulation results of the dynamic and domino 16-bit and 32-bit adders are shown in below figures.

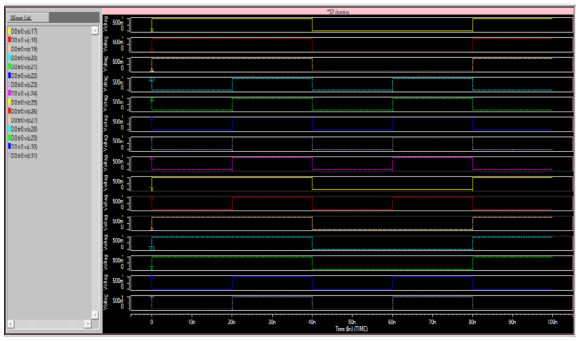

Fig.8: 32-bit domino adder results

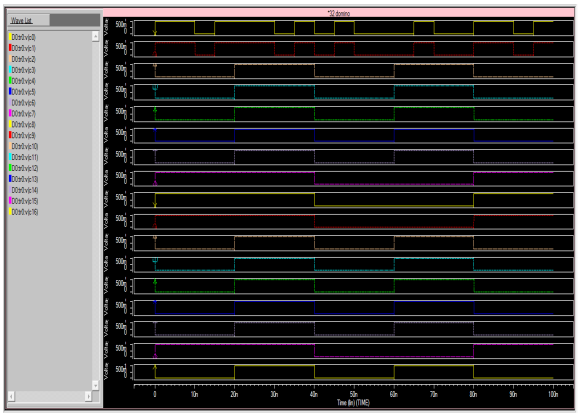

Fig.9: 16-bit domino adder results

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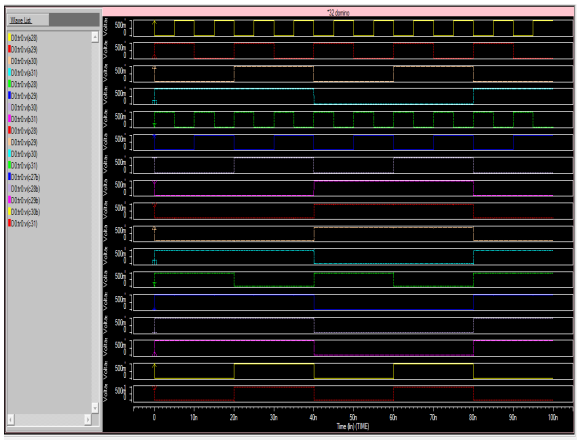

Fig.10: 32-bit dynamic adder results

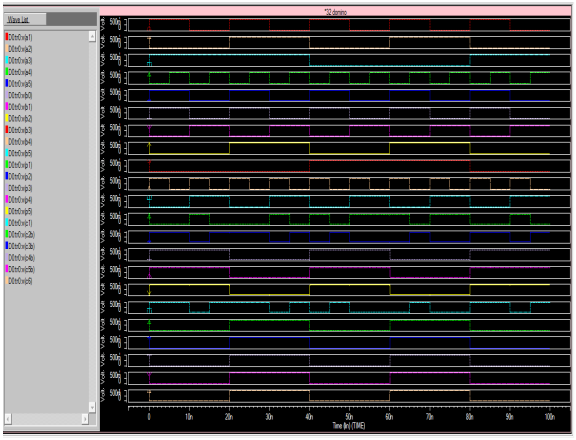

Fig.11: 16-bit dynamic adder results

Table I

Technology of 32-Bit Carry Look Ahead Adder	Dynamic Switching power consumption(W)	Propagation delay of CLA for C_{32}(ps)	Power Delay Product(fJ)
Si-MOSFET Domino Logic	4.42×10^{-6}	13.50	16.74
Si-MOSFET NP Dynamic CMOS	4.32×10^{-6}	8.103	35.01
CN-MOSFET Domino Logic	1.24×10^{-6}	195.03	241.83
CN-MOSFET NP Dynamic CMOS	1.19×10^{-6}	193.95	230.01

V.CONCLUSIONS:

Low-power, compact, and high-performance NP dynamic CMOS circuits with a 16 nm carbon nanotube transistor technology are presented in this paper. The performances of four 32-bit carry lookahead adders with different circuit techniques and technologies are characterized: Si-MOSFET domino logic, Si-MOSFET NP dynamic CMOS, CN-MOSFET domino logic, and CN-MOSFET NP dynamic CMOS. The well-known area and power consumption disadvantages of the NP dynamic CMOS circuits are eliminated by employing a carbon nanotube transistor technology. The CN-MOSFET NP dynamic CMOS circuit effectively suppresses both dynamic switching and leakage power consumption while providing similar propagation delay and miniaturizing the area as compared to bothsilicon and carbon nanotube domino logic circuits. The NP dynamic CMOS logic family is recommended as a better alternative to the conventional domino logic for the implementation of future high speed digital integrated circuits with carbon nanotube transistors.

The total area of the CN-MOSFET NP dynamic CMOS adder is reduced by 35.53%, 77.96%, and 15.52% while providing similar propagation delay as compared to the Si-MOSFET domino logic, Si-MOSFET NP dynamic CMOS, and CN-MOSFET domino logic circuits, respectively. Miniaturization of the CN-MOSFET NP dynamic CMOS circuit reduces the dynamic switching power consumption by 80.54%, 95.57%, and 25.66% as compared to the Si-MOSFET domino logic, Si-MOSFET NP dynamic CMOS, and CN-MOSFET domino logic circuits, respectively. Furthermore, the leakage power consumption of the carbon-based NP dynamic CMOS adder is suppressed by up to 99.98% as compared to the conventional silicon-based dynamic circuits, due to the steeper subthreshold slopes and smaller sizes of CN-MOSFETs as compared to Si-MOSFETs.

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