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Design of Push Pull Pulsed Latches by Using Dual Stack Method

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Abstract:

In this paper, an improved class of pulsed latches is introduced and experimentally assessed in 45-nm CMOS. Its topology is based on a push–pull final stage driven by two split paths with a conditional pulse generator, which differentiates two circuit implementations which can be either shared (CSP3L) or not (CP3L). Highest performance is achieved with this proposed topology as it outperforms the well-known transmission gate pulsed latch (TGPL) by 1.7×–2× along with that improved the energy efficiency is obtained. Improvement in designs targeting minimum ED3 product (energy × delay3) over leading TGPL was found 2.4× for ED3, for minimum ED is about 1.5×. But this comes to existence with a slight circuit complexity which in turn increases cell area of a 1.15×−1.35× in typical systems. Using methods likes dual stack and clock gating flexibility can be increased to greater extent that confirm that the above benefits are kept in the presence of variations. Area penalty can be overcome with the 45-nm CMOS technology which may increase area below 1% compared to existing systems. Hence high performance and energy efficiency requirements are achieved using proposed latches for VLSI systems.

Index Terms:

Energy-delay tradeoff, flip-flops (FFs) , nanometer CMOS, pulsed latches, VLSI, clock gating, dual stack .

I.INTRODUCTION:

High performance and energy efficiency are the most important requirements in the VLSI system design FLIP-FLOPS (FFs) and latches are widely used in all such system designs known to be responsible for a large fraction of the power budget of microprocessors and VLSI systems . Typically, they dissipate 80% of the total clock power , and 30% of the overall power budget. Energy efficiency of FFs and latches is nowadays even more critical than in the past, considering that speed can be increased only through improvements in energy efficiency, since VLSI systems are power. Therefore, the search for novel topologies with a targeted speed under a relatively low consumption (with their tradeoff quantified by composite Ei Dj metrics) is highly required.

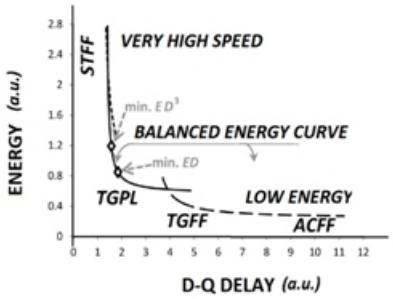

Fig. 1. Pareto-optimal energy-delay curve of existing FF topologies for a typical load of 16 minimum inverters (energy per cycle and D–Q delay are in arbitrary units).

So in order to optimize power of a device the simplest control technique is to shut off the clock of the sequential block of the device. The power reduction must be achieved without trading-off performance which makes it harder to reduce leakage during normal (runtime) operation. On the other hand, there are several techniques, such as dual stack, clock gating .., dual stack approach [1], in sleep mode, the sleep transistors are off, i.e. transistor N1 andP1 are off.

We do so by making S=0 and hence S'=1. As we know that static power is proportional to the voltage applied, with the reduced voltage the power decreases but we get the advantage of state retention. Another advantage is got during off mode if we increase the threshold voltage of N2, N3 and P2, P3. The transistors are held in reverse body bias. As a result their threshold is high.

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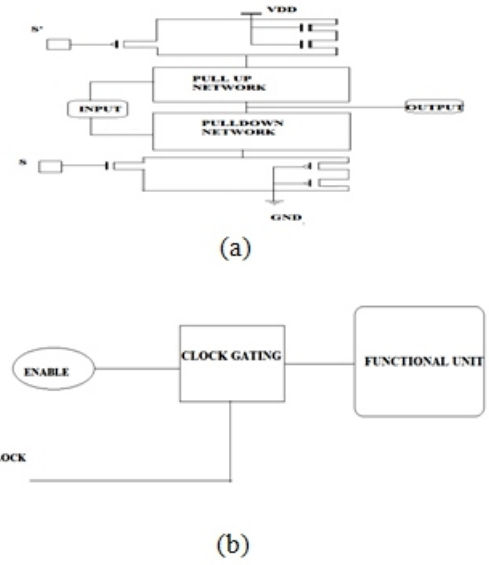

Fig.2 power reduction techniques (a) dual stack (b) clock gating

High threshold voltage causes low leakage current and hence low leakage power. As a result of stacking, P2 and N2 have less drain voltage. While in active mode i.e. S=1 and S'=0, both the sleep transistors (N1 and P1) and the parallel transistors (N2, N3 and P2, P3) are on. They work as transmission gate and the power connection is again established. Further they decrease the dynamic power. Clock Gating is a technique that can be used to control power dissipated by Clock net. In synchronous digital circuits the clock net is responsible for significant part of power dissipation (up to 40%). Clock gating reduces the unwanted switching on the parts of clock net by disabling the clock Topologies like STFF, TGPL, TGFF, ACFF represent high speed energy efficient FF, based on the criteria that ranging from high-speed (i.e., points with minimumEDj product with j > 1) to energy-efficient designs (i.e., points with minimum ED). The transmission gate pulsed latch (TGPL) (see Fig. 3) used in various Intel microprocessors is the most energy-efficient FF in a rather wide portion of the Pareto-optimal curve. Only the skew-tolerant FF (STFF) is able to outperform transmission gate flip-flop (TGFF) for extremely high-speed design targets (i.e., points with minimum EDj for j ≥ 5). In this region, the STFF speed advantage in terms of D–Q delay is typically about 10%, at the cost of a 2× greater energy . Hence, although STFF is slightly better than TGPL in terms of pure performance, but its significantly worse energy efficiency does not make it as competitive as TGPL in applications where energy efficiency is a concern.

Hence, in the following, TGPL will be adopted as a reference for high-speed energy-efficient designs. When slower design slower design targets are considered, master-slave FFs exhibit better energy efficiency. The traditional TGFF and the recently proposed Toshiba ACFF are, respectively, the most efficient among designs with balanced energy-delay (i.e., minimum ED) and ultralow energy designs (i.e., minimum E j D with j > 1).

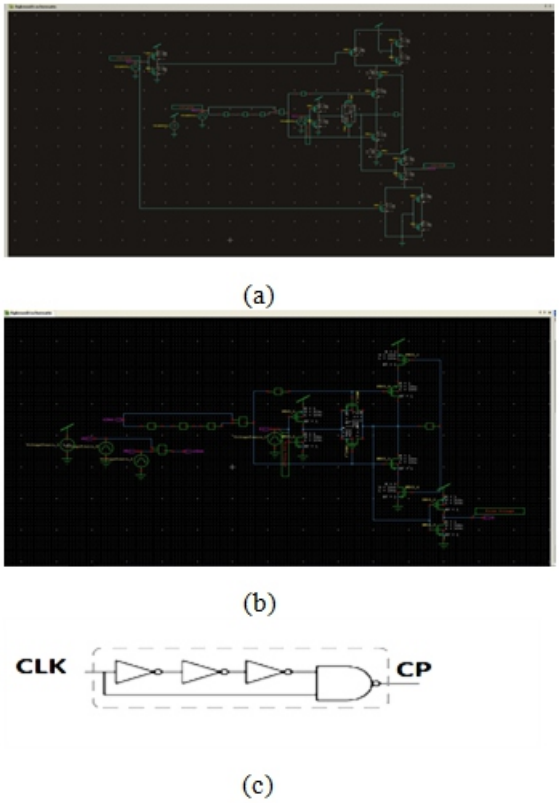

Fig. 3. (a) TGPL in dual stack and (b) clock gating (c) Pulse generator topologies (area in dashed line is shareable among multiple cells)

An improved class of pulsed latches (conditional push–pull pulsed latch) is introduced with the main idea is to adopt a push–pull output stage, which is driven by two split paths for rise and fall output transitions, with the explicit aim of reducing both the path effort and the parasitic delay . In addition, the capacitance at the output of the first stage is further reduced by adopting half-latches in the split paths and moving the cross-coupled inverters to the output . (CP3L) and (CSP3L) are the two versions respectively without and with shareable conditional pulse generator. The proposed pulsed latches have larger area than TGPL, with a resulting increase in the area of practical VLSI systems that is well below 0.9%.Implementation of this paper is as follows.

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In Section II, the basic idea of proposed novel topologies and their operation is described, and their detailed circuit implementation is discussed in Section III. The potential speed advantage compared to TGPL is analytically evaluated in Section IV, and aspects related to physical design and layout parasitics are discussed in Section V. Measurements results and simulations are discussed in Section VI. Conclusions are reported in Section VII.

II.OVERALL IDEA ON STRUCTURE AND OPERATION OF CONDITIONAL PUSH–PULL PULSED LATCH:

As shown in Fig. 4, the proposed class of pulsed latches, push–pull output stage is adopted (M7-M8) as opposed to the traditional output inverter stage employed in most existing topologies (see P5–N5 in TGPL in Fig. 3). Such a technique allows for reducing the load of the driving circuitry by a factor 2–3, thereby making it faster and more energy efficient. This also allows M7–M8 in Fig. 4 to be up-sized, and hence have a faster output stage. The push–pull output stage in Fig. 3 is driven by two split paths that generate the active-high R (active-low set ¯S) pulsed signal, which resets (sets) the output when active. Pulses R and ¯S are alternatively generated to enable a fall/rise output transition,

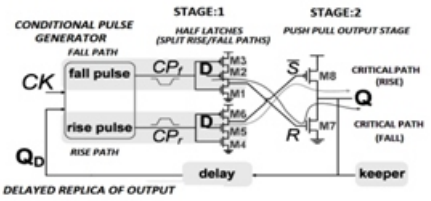

Fig. 4. general structure of proposed class of pulsed latches.

respectively. These pulses are generated at the falling clock edge by the conditional pulse generator in Fig. 3, and are transferred to the output stage by either the half latch M1–M3 or M4–M6, depending on whether input D is, respectively, low or high (see below for detailed description of pulse waveforms). These half latches in the first stage within the D–Q critical path have less parasitics compared to typical clocked inverters or inverters with cascaded transmission gate [10]–[18] (see P1,N1,P2,N2 in Fig. 3). The input D drives two different paths, respectively, through an nMOS (M5) and a pMOS (M2) transistor in Fig. 4, which is equivalent to the load of a traditional input inverter stage (see P1-N1 in TGPL in Fig. 3).

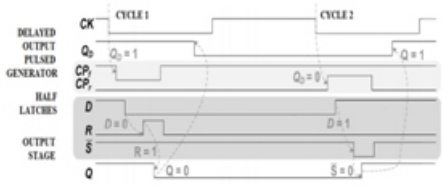

Fig. 5.internal waveforms of general structure

The operation of the scheme in Fig. 3 is explained in detail in Fig. 5, which depicts the main waveforms of the internal signals. After the falling clock edge (cycle 1 in Fig. 5), the pulse generator checks if the previous output1 QD in Fig. 3 is high or low. If previous output is QD = 1, next output Q can stay at the same value or make a falling transition, hence a pulse is generated in the fall path in Fig. 4 through the active-low signal CP f , whereas nothing changes in the rise path (active-high signal CPr is kept low, thus latch M4–M6 keeps ¯S high and maintains M8 OFF). Subsequently, if input stays at the previous value D = 1, the latch M1–M3 is not enabled; hence R is dynamically kept at the previous value R = 0 (then, it is statically tied to ground once the pulse expires). On the other hand, if input changes to D = 0, the latch M1–M3 is enabled and the CP f pulse determines a high pulse in R, which turns M7 ON and brings the output Q to low.

Afterwards, its delayed output replica QD experiences the same transition. If the previous output is QD = 0, right after the falling clock edge (cycle 2 in Fig. 4), a pulse is generated in the rise path through the active-high signal CPr (nothing changes in the fall path). If input stays at the previous value D = 0, the latch M4–M6 is disabled and ¯S is kept high, so that nothing changes in the rise path.If input changes to D = 1, the latch M4–M6 is enabled and the CPr pulse pulls down ¯S, thereby turning M8 ON and bringing Q to high. Afterwards, the delayed output replica QD experiences the same transition. At the steady state, R (¯S) in Fig. 3 is set to 0 (1), there by turning OFF the output transistors M7–M8, with the output being maintained at the desired value by a keeper. In other words, the memory element within the proposed topology in Fig. 3 is actually placed at the output node, as opposed to most of the existing topologies where it is placed before the output stage (see the gated cross-coupled inverter pair in Fig. 3, which is connected to the input of the output stage P5-N5). This permits to move the parasitics associated with the memory element to the output node, thereby making the input node of the output stage lightly loaded, and hence faster and more energy efficient.

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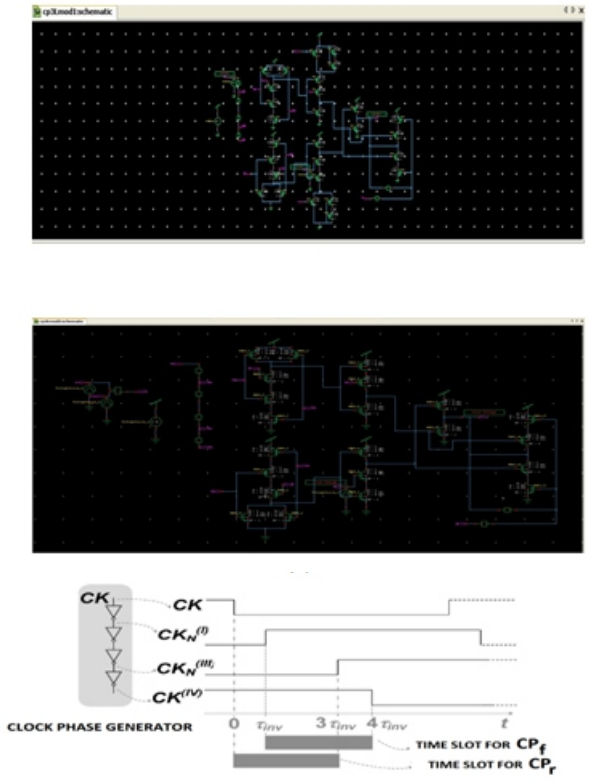
III.IMPLEMENTATION OF CP3L AND CS-P3L TOPOLOGIES:

As discussed above, the proposed class of pulsed latch in Fig. 4 tends to have a lightly loaded D–Q critical path, thereby making it potentially fast and energy-efficient. Such features can be implemented in different ways.

A. CP3L:

Conditional Push–Pull Pulsed LatchThe schematic of CP3L topology is depicted in Fig. 6. The keeper (P11,P10,N10,N11 in Fig. 6) drives the output Q and comprises a cross-coupled inverter pair, whose forward inverter.



(b)

Fig.6 (a) CP3L dual stack & clock gating topology (b) wave forms of pulse generator(which can be shareable among multiple cells)

is gated to avoid current contention with the output stage N9-P9. Indeed, if R = 1 the pull-down N9 of the output stage is ON and the pull-up network of the keeper is OFF through P10. Analogously, if ¯S = 0 the pull-up P9 of the output stage is ON and the pull-down network of the keeper is OFF through M10. As an additional advantage brought by placing the keeper after the output stage rather than before, CP3L has lighter loan on its critical path since the half latch P7,P8,N8 (P6,N6,N7) in the first stage has to drive the single transistor M11 (M10). Also, since the two pulses R and ¯S are alternatively generated, either M10 or M11 in the keeper are actually subject to transitions of the gate terminal in a given cycle. In contrast, the first stage of traditional topologies must drive two transistors associated with the keeper, and both of them are subject to transitions (see transistors M11–M12 in Fig. 3, which load transistors M3–M4 lying in the critical path). This clearly reduces the parasitic load of the first stage of CP3L and reduces activity at the keeper capacitances, thereby making the first stage faster and potentially more energy efficient.Regarding the pulse generator, it comprises a clock phase generator, a pseudo-NAND for the fall path (P1,P2,N1,N2,N3 in Fig. 6), and a pseudo-NOR gate for the rise path (N4,N5,P3,P4,P5).

Operation is summarized in Fig. 5(b), which depicts the waveforms of the signals involved in the generation of the CP f and CPr pulses. Accordingly, during the time slot τinv–4τinv in Fig. 6(b), the pseudo-NAND temporarily sets CP f low through transistors N1-N3 if QD = 1 (otherwise, CP f remains high). Similarly, during the time slot 0–3τinv in Fig. 6(b), the pseudo-NOR temporarily sets CPr high through transistors P3-P5 if QD = 0 (otherwise, CP f remains low). Hence, the clock phase generator and the pseudo-NAND/NOR gates implement a conditional pulse generator, which alternatively produce a pulse on either CP f or CPr , as determined by the previous output value QD.

The clock phase generator can be shared among multiple latches to amortize its overhead. It is useful to observe that the width of CP f and CPr pulses determines the width of the transparency window of CP3L latch in which the input can affect the output. From a design point of view, the width of the transparency window can be modified by changing the delay of the inverters within theclock phase generator in Fig. 6(a).Process variations are even controlled with no tune-ability is added to the considered pulsed latches since the addition of such feature would impact area/energy of any pulsed latch equally. Indeed, almost all existing pulsed latches adopt the same pulse generator topology. The delay stage in the feedback path in Figs. 3–5 generates a delayed replica QD of the output Q, and is implemented by the two inverters inv5 and inv6 in Fig. 6.

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Actually, only slow transistors inv6 are added to implement such delay, as the inverter inv5 is already available (i.e., inv5 are used to both latch and delay the output). This delay stage makes sure that QD is kept stable at its previous value during the transparency window, thereby preventing glitches in CPr and CP f and reducing dynamic energy, as discussed in the following Without the delay stage, the output Q would be connected directly to the pseudo-NAND/NOR in Fig. 5, hence any output transition within the transparency window immediately triggers the generation of an additional (undesired) pulse.

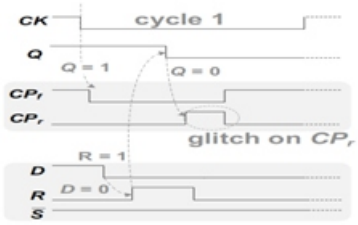

Fig.7 Occurrence of glitches in feedback path if no delay stage is inserted.

As shown in detail in Fig. 7, which refers to the case where Q is directly connected to the pseudo-NAND/NOR, a falling transition of Q following the same input transition immediately triggers a high pulse in CPr , as the pseudo- NOR in Fig. 5 temporarily has all pMOS transistors P3-P5 ON during the transparency window (i.e., the CPr time slot in Fig. 6(b). Observe that this glitch in CPr pulse increases the dynamic energy, but it does not affect correct operation. Indeed, if previous output was Q = 1 and the current input is D = 0 as in Fig. 7, the CPr glitch cannot propagate through the half latch P6,N6,N7since N6 is OFF. On the other hand, if the previous output was Q = 1 and the current input is D = 1, the CPr glitch propagates through the half latchM4–M6 and temporarily sets $\bar{S} = 0$, but it does not affect the output anyway since the latter is kept at the desired value Q = 1 through M8.

A.CSP3L: Conditional Shareable Push–Pull Pulsed Latch:

In CP3L, the pulse generator cannot be shared among multiple latches since pseudo-NOR/NAND are driven by QD, which is different for each latch. In this subsection, we present a different implementation of the same concept by integrating the conditional logic in the latch so that the whole pulse generator can be shared. The resulting conditional shareable push–pull pulsed latch (CSP3L) topology is depicted in Fig.8.

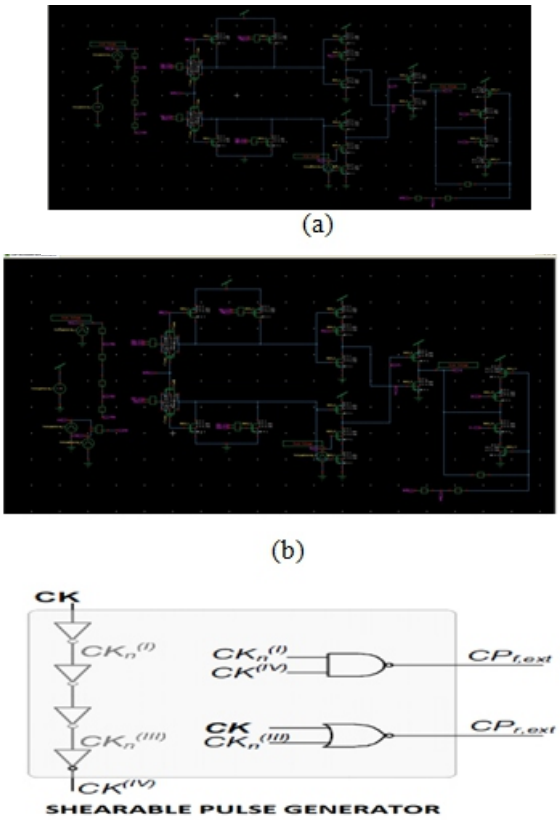

Fig.8 (a) CSP3L topology and its clock gating topology (b) pulse generator(which can be shareable among multiple cells)

In CSP3L, static NAND/NOR gates are introduced in the shareable pulse generator to generate the pulses CPf, ext and CPr ,ext that are distributed to multiple latches and have the same role as CP f and CPr had in CP3L. In each latch, such external pulses are enabled through the switches implemented by P1–N3 in Fig. 8, which implement the conditional pulse selection logic. The latter comprises two transmission gates and two small keepers to maintain the same operation as before. As discussed above, the delay stage M23–M26 is introduced in the feedback path (two more than CP3L since the transmission gates need complementary control signals). The resulting transistor count is the same as CP3L, hence CSP3L area is expected to be roughly the same as CP3L (excluding the shareable part).Since CSP3L is based on the same concept as CP3L, operation is very similar. The main difference is in the conditional pulse selection logic, which enables the propagation of either CPf ,ext or CPr ,ext to the half latches, according to the value of the delayed output replica QD. In particular, if QD = 1 (QD = 0) the fall (rise) path is activated, as the transmission gate N8,P8,P7 (N7,N6,P6)

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transfers the CPf, ext (CPf ,ext) pulse to the input of the half latch N8,P8,P7(N7,N6,P6), similar to the pseudo-NAND (pseudo-NOR) of CP3 L in Fig. 6. As a minor difference from CP3L, the input capacitance seen from CPf, ext and CPr, ext in CSP3L depends on Q, which may lead to data-dependent clock skew (see Fig. 8). In practical cases, this is not a concern considering that pulsed latches inherently tolerate a significant amount of skew.

IV.ANALYSIS OF PERFORMANCE POTENTIAL:

Here in this section, CP3L and CSP3L are comparatively evaluated to TGPL in terms of maximum achievable performance through logical effort analysis. According to the analysis under the assumptions in the Appendix, CP3L, CSP3L and TGPL topology is where CL and Cin are, respectively, the load and the input capacitance of the pulsed latch. CP3L and CSP3L have basically the same minimum D–Q delay, as is expected by considering that they have the same D–Q critical path (M1–M8 in Figs. 6 and 8). CP3L and CSP3L are always faster than TGPL. Their theoretical maximum speed advantage is about2.4× and is obtained at light loads (i.e., electrical effort CL / Cin ~ 1..The above speed improvement is justified by the lighter load of the stages lying in the critical path.

$$D_{\min,CP^3L} \approx D_{\min,CSP^3L} \approx \sqrt{\frac{4}{3}\cdot\frac{C_L}{C_{in}}} + \frac{5}{3}$$

$$D_{\min,TGPL} \approx \sqrt{\frac{5}{3}\cdot\frac{C_L}{C_{in}}} + \frac{34}{9}$$

Logical effort analysis in the Appendix permits to quantify the advantages of CP3L and CSP3L in each critical path stage. CP3L and CSP3L have a speed advantage over TGPL both in the first and second stage. In particular, the first stage has 1.25× lower logical effort and 2× lower parasitic delay thanks to the lighter loading effect of parasitics, compared to TGPL.

V. SIMULATION RESULTS:

The above discussion regarding the CP3L, CSP3L, and TGPL latch. Here below figures represent the output waveforms in simulations and their contribution to-wards low power and high efficiency by the reduction of D-Q delays. This figure shows that energy of CP3L andCSP3L is from 40% to 60% higher than TGPL depending on the specific activity. Energy itself is clearly not representative of energy efficiency, as it should be evaluated as iso-performance.

The energy-delay tradeoff of the above topologies for the different design targets is depicted in Fig. 15(a), which shows that the minimum- ED CP3L and CSP3 L (which are once again very close to each other) is even faster and consumes less energy than the minimum-ED3 TGPL. More quantitatively, the energy of CP3L, CSP3L, and TGPL for 25% data activity is, respectively, 42, 41.5, and 26.1 fJ for minimum-ED energy, hence CP3L and CSP3L exhibit a 1.3× better energy-delay product compared to TGPL. For minimum-ED3 design, the energy of CP3L, CSP3L, and TGPL is 73.7, 75.7, and 46.1 fJ, hence CP3L and CSP3L improve ED3 by 2.3×, compared to TGPL. From Fig. 14, similar or better energy efficiency is expected at other realistic values of data activity. The energy improvement enabled by CP3L and CSP3 L is intuitively explained by considering that these topologies are significantly faster than TGPL (see Section IV).

Hence, CP3L and CSP3 L tend to have smaller transistor sizes for a given performance target, which in turn translates into smaller dynamic and leakage energy compared to TGPL.Leakage can also be a concern in FF and latches, for example, in VLSI systems operating in standby mode while retaining information in registers and power gating all other gates . The leakage current under equiprobable inputs for CP3L, CSP3L, and TGPL is 316, 401.6, and 424.6 nA, respectively, for a minimum-ED design. As shown in Fig. 15(b), this translates into a more favorable leakage-delay tradeoff, with a 2.7× improvement in the leakage-delay product. For minimum-ED3 design, leakage of CP3L, CSP3L, and TGPL is 561.7, 685.7, and 832.5 nA, which translates into a 5.4× improvement in the leakage-delay3 product.

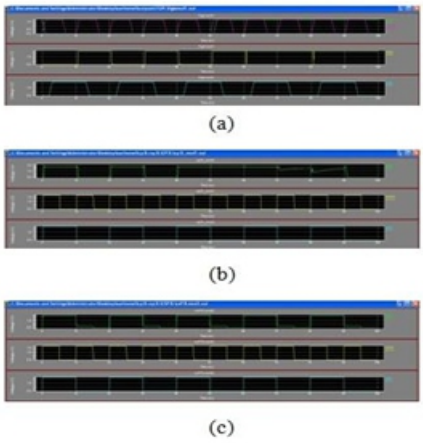

Fig.9Simulation results of (a) TGPL (b) CP3L (c) CSP3L

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	A	B	C	D
1		DELAY	RISE	FALL
2	ACFF	1.10E-08	4.00E-08	6.00E-12
3	TGFF	1.00E-08	3.10E-11	2.25E-10
4	CP3L	4.10E-11	8.00E-12	8.00E-12
5	CSP3L	5.00E-10	5.00E-10	9.90E-10
6	CP3LEX	4.00E-09	1.00E-08	5.70E-11
7	CSP3LEX	1.50E-08	2.50E-08	9.00E-09

Table: Comparison Table.

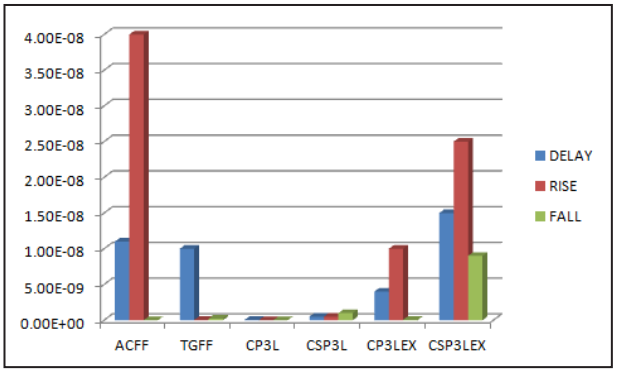

Fig11: Dealy , Rise, Fall Time Graphs

VI.CONCLUSION AND FUTURE WORK:

In this paper a new improved latches in which its push–pull final stage and split paths in the first stage enable a significant reduction in path and parasitic effort. More importantly, pulsed latches enables a significant improvement beyond TGPL.. Finally, the CP3L and CSP3L were shown to be equivalent in terms of energy and performance, also equally worth considering when designing highly energy efficient systems. The choice between CP3L and CSP3L is driven by preliminary de-sign through power gating techniques clock gating and dual stack which in turn reduces the static and dynamic power dissipations.Indeed, CP3L does not allow for sharing a pulse generator, but has lower area than CSP3L if the pulse generator is included. Hence, CP3L is preferable when only a small subset of FFs needs to be replaced by a pulsed latch .Indeed, in this case latches tend to be far from each other, and hence it does not make sense to share their pulse generator. On the other hand, CSP3L is prefer-able in systems where a significant number of FFs need to be replaced.

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