

Multi Port Router Architecture

Chimata.Venkateswarlu

VLSI System Design,

AVR and SVR CET, Nandyal, Kurnool.

N.Md.Bilal, M.Tech

Associate professor,

AVR and SVR CET, Nandyal, Kurnool.

ABSTRACT:

The users which are want to set-up a LAN (Local Area Network) or WLAN (wireless LAN) and connect all computers to the Internet without having to pay a full broadband subscription service to their ISP for each computer on the network. The router consists of one input port and three output ports for the purpose of packet enter at the source terminal and the packet is driven out at the destination terminal respectively. This type of packet travels through a router it is called as NETWORK ROUTER. In the network router specific Packet contains 3 parts. Those are header part, data part and frame check sequence part. Packet width is 8 bits and the length of the packet can be between 1 byte to 63bytes. In the packet the Destination address (DA) of the packet is of 8 bits. The switch drives the packet to the related ports based on this destination address of the packets. In this process every output port has 8-bit unique port address. If the destination address of the packet matches the port address, then switch drives the packet to the output port, Length of the data is of 8 bits. This network router supports three parallel connections at the same time. The router uses store and forward type of flow control and FSM Controller deterministic routing which improves the performance of router.

MULTI PORT ROUTER:

In the functional verification it decides the silicon quality and more than 50% of the design cycle time is for the verification /simulation. Due to the functional bugs as more as possible ASIC fault responses are occurring in the design cycle. For the avoid the delay and meet the TTM, we use the latest Verification methodologies and technologies and accelerate the verification process. This project helps to understand the complete functional verification process of complex ASICs an SOC's and it gives opportunity to learn the trending verification methodologies, programming concepts like Object Oriented Programming of Hardware Verification Languages and sophisticated EDA tools, for the high quality verification.

Essential necessity of router:

Broadband or ICS routers will manufacture as quite as different with the value of brand in the quality. Those hardware devices are generally a small box shape with the front and back ports for the purpose of switchable operations in the each computer with the plugging of port in your broadband modem. Depending on the modem and Internet connection formats you have available, and also the user choose a router with phone or fax operating ports. Router operates on the functions of direct trafficking. A packet of data is forwarded in the internetwork operations till it grasps the node of destination. The router applications are so useful in the home to setup a LAN or WLAN for the connection of all computers with a single router network. Those are the internet services to pay the full broadband subscription to their Internet Service Protocol. In many cases, an ISP will give the permission to use a router and connect multiple computers to a unique Internet connection and pay a normal fee for each additional computer sharing the connection.

In the business or organization the need of connections of multiple computers to the Internet, but also want to the multiple links between the private networks and it will not be created equal when ever their job will differ slightly between different networks. A router doesn't define its shape, color, size or manufacturer, but its operation of routing data packets between computers. A modem which routes data between your PC and your ISP can be considered a router. In its most basic form, a router could simply be one of two computers running the Windows 98 (or higher) operating system connected together using ICS (Internet Connection Sharing). In this scenario, the computer that is connected to the Internet is acting as the router for the second computer to obtain its Internet connection. Going a step up from ICS, we have a specific type of hardware routers that are used to perform the same basic task as ICS with more features and functions. Ethernet is a computer networking technology which enhances for local area networks (LANs) and metropolitan area networks (MANs).

It has been refined to support complex and high mode of bit rates and longer link distances. In Ethernet broadband router the type of wired network will typically have a built-in Ethernet switch to allow for the services of expansion and also those support NAT (network address translation), which gives permission to all of the computers by the access of single IP address on the Internet. Internet connection sharing routers will also provide users with much needed features such as an SPI firewall or serve as a DHCP Server.

DESIGN OF ROUTER:

In the manner of target contest and accomplishment adopted a set of principles about the implementation of particular size of router within the concept of minimal design window for the efficient performance. Provisional of specifications for the Router is totally depends on the type of packet based protocol. In the incoming packet the router wires in between the port of input to output port on the basis of address which is consists in the packet. The router implements in the network mode which has a one port of input where the packet enters and three output ports where the packet is driven out. In the format of packet there are three parts. Those are Header, data and frame check sequence.

The width of packet is in terms of 8 bits and the length of packet defined in between 1 to 63 bytes. The header of packet consist of three fields DA and lengthDA is nothing but Destination address of the particular packet and each packet consists of 8bits address data. The packet is driven by the switch with respect to the ports based on the destiny address of particular packets. The size of output port has 8-bit and this address of port is unique. The port address matches to the destination address in the automatic mode the processing of switch wires the packet to the output port, length of the data is of 8 bits and from 0 to 63.

Data must be in the form of bytes and it accepts anything. Actually the binary logic parameter bytes are measured for length in the design of router. The security issues of checking the packet by the frame check sequence of the packet and calculate over the header and data. The router carried out the communication on network on chip for the design of effective NOC and in this case the router operated as well as effective. In this type of NOC's which are used in the operations of router used here is packet switching.

The router works on the store and fetch mode of operations with the controller of FSM and it improves the performance of router by the deterministic routing. The router operates on the size of three ports with the efficient connections. In the transfer of data packets the store, fetch and flow mechanism is the best one because of no requirement for channel reservation and thus does not avoid the effect of idle physical channels. In the operation of ROUTER the role of buffering is to utilize the avoidance of both sides of directions without the effect of congestion.

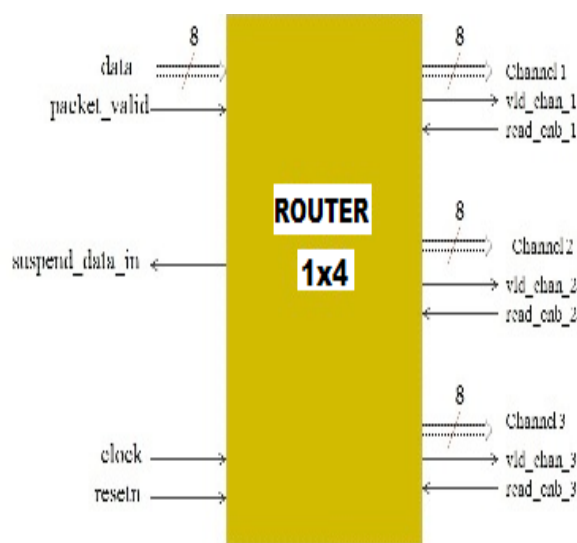


Fig. 1- Block Diagram of four Port Router

FEATURES:

- * Full duplex synchronous serial data
- * Variable length of transfer word up to 64 bytes.
- * HEADER is the first data transfer.
- * Rx and Tx on both rising or falling edge of serial clock independently.
- * Fully static synchronous design with one clock domain
- * Technology independent
- * Fully synthesizable
- * Multi receivers select lines
- * ROUTER is a Synchronous

The clock signal is provided by the master to provide synchronization. The clock signal controls when data can change and when it is valid for reading. Since ROUTER is synchronous, it has a clock pulse along with the data. RS-232 and other asynchronous protocols do not use a clock pulse, but the data must be timed very accurately. Since ROUTER has a clock signal, the clock can vary without disrupting the data.

October 2015
Page 661

Logic Utilization	Used	Available
Number of Slices	602	4656
Number of Slice	659	9312
Flip Flops		
Number of 4 input	533	9312
LUTs		
Number of bonded	53	232
IOBs		
Number of GCLKs	1	24

[2]Bluespec Inc, <http://www.bluespec.com>

[3]Xilinx, “ML605 Hardware User Guide”, http://www.xilinx.com/support/documentation/boards_and_kits/ug534.pdf.

[4]Xilinx, “LogiCORE IP Processor Local Bus (PLB) v4.6”, http://www.xilinx.com/support/documentation/ip_documentation/plb_v46.pdf.

[5]M. Pellauer, M. Adler, M. Kinsy, A. Parashar, and J. Emer, “HASim: FPGA-Based High-Detail Multicore Simulation Using Time-Division Multiplexing”, HPCA, 2011.

[6]P. Wolkotte, P. Holzspies, and G. Smit, “Fast, Accurate and Detailed NoC Simulations”, NOCS, 2007.

TOTAL DELAY - 6.831ns

Final Register Report:

Macro Statistics

Registers : 659

Flip-Flops : 659

CONCLUSION:

In the router functional analysis of ports we define the topologies of multiple ports of the router with the enhanced methodologies of verification. In the project we verify the 3 port router operations and extended to the size of for five ports. This ROUTER improves the performances by the reducing of delay values with the increment of ports and we define the topology in the manner of efficient functional verification. The router ports are verified by the data read ports as output the device to allow the access of multiple computers usage. The router technology will enhance the real time applications MODEM and ETHER-NET protocols in the usage of broadband networks and internet wireless networks.

REFERENCES:

[1]“D. Chiou, “MEMOCODE 2011 Hardware/Software CoDesign Contest”,<https://ramp.ece.utexas.edu/redmine/attachments/DesignContest.pdf>.