ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

# VLSI Architecture Design for Image Compression Using Modified DCT

**E.Divya Teja**
PG Scholar,
Dept of ECE,
Global College of Engineering & Technology,
Kadapa, YSR (Dt), AP, India.

**Y.Maheswar Reddy**
Associate Professor,
Dept of ECE,
Global College of Engineering & Technology,
Kadapa, YSR (Dt), AP, India.

## ABSTRACT:

DISCRETE COSINE TRANSFORM (DCT) is a widely used transform engine for image and video compression applications. In recent years, the development of visual media has been progressed towards high-resolution specifications, such as high definition television (HDTV)..

The proposed spatial scheduling strategy includes the ability to choose the proposed methodology precision bit lengthi.e 8 bit , a hardware sharing architecture that reduces the hardware cost, and the proposed time scheduling strategy arranges different dimensional computations in that it can calculate first-dimensional and second-dimensional transformations simultaneously with hardware utilization of 100%.

A multiplierless methodology is chosen by replacing the multiplier with adders is based on test image simulations. In addition, the proposed hardware sharing architecture employs a binary signed-digit architecture that enables the arithmetic resources to be shared for all blocks of image implementation.

**Tags:** DCT transform, image compression.

## I.INTRODUCTION:

The growth of multimedia technology over the past decades demanded the increased use of digital information. The advances in technology have made the use of digital images prevalent to a large extent. Digital images comprised of large amount of data. Reduction in the size of the image data for both storing and transmission of digital images are becoming increasingly important as they find more applications. Image compression maps from a high dimensional space to a low dimensional space.

The main aim of the compression of image is to represent an image with minimum number of bits with an acceptable anality of image. Transformation is a very useful tool in image compression. It transforms the image data in time domain to frequency domain. By transforming the data into frequency domain, the spatial redundancy in the time domain can be minimized.

The energy of the transformed data is mainly condensed in low frequency region; therefore image can be represented by a few transform coefficients by discarding most of these coefficients without significantly affecting the reconstructed image quality.

## II. RELATED WORK:

### 2D DCT Algorithm:

The 2D DCT architecture uses the row—column distributed arithmetic version of the Chen fast DCT algorithm [2]. The first step of the Chen algorithm is a factorization of the DCT-I matrix such that the subsequent computation of the even indexed coefficients are fully separated from the computation of the odd indexed coefficients. The 1D DCT coefficients Xk, k=0,l, …, 7 for an 8-point input vector xn, n=0,l, …, 7 can be expressed as follows:

$$\begin{bmatrix} X0 \\ X2 \\ X4 \\ X6 \end{bmatrix} = \begin{bmatrix} A & A & A & A \\ B & C & -C & -B \\ A & -A & -A & A \\ C & -B & -B & C \end{bmatrix} \begin{bmatrix} x0+x7 \\ x1+x6 \\ x2+x5 \\ x3+x4 \end{bmatrix} \quad (1)$$

$$\begin{bmatrix} X1 \\ X3 \\ X5 \\ X7 \end{bmatrix} = \begin{bmatrix} D & E & F & G \\ E & -G & -D & -F \\ F & -D & G & E \\ G & -F & E & -D \end{bmatrix} \begin{bmatrix} x0-x7 \\ x1-x6 \\ x2-x5 \\ x3-x4 \end{bmatrix} \quad (2)$$

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

where $A=\cos(\frac{\pi}{4})$, $B=\cos(\frac{\pi}{8})$, $C=\sin(\frac{\pi}{8})$, $D\cos(\frac{\pi}{16})$, $E=\cos(\frac{3\pi}{16})$, $F=\sin(\frac{3\pi}{16})$ and $G=\sin(\frac{\pi}{16})$

## Distributed Arithmetic:

Distributed arithmetic (DA) is an important FPGA technology. It is extensively used in computing the sum of products.

$$y = \langle c, x \rangle = \sum_{n=0}^{N-1} c[n] \times x[n]. \quad (3)$$

To understand the DA design paradigm, consider the "sum of products" inner product shown below:

$$y = \langle c, x \rangle = \sum_{n=0}^{N-1} c[n] \times x[n] = c[0]x[0] + c[1]x[1] + \ldots + c[N-1]x[N-1]. \quad (4)$$

Assume further that the coefficients c[n]are known constants and x[n] is a variable. An unsigned DA system assumes that the variable x[n] is represented by

Where xb[n] denotes the bth bit of x[n], i.e., the nth sample of x . The inner product y can, therefore, be represented as

Redistributing the order of summation (thus the name "distributed arithmetic") resulted

$$x[n] = \sum_{b=0}^{B-1} x_b[n] \times 2^b \quad \text{with } x_b[n] \in [0,1] \quad (5)$$

$$y = \sum_{n=0}^{N-1} c[n] \times \sum_{b=0}^{B-1} x_b[n] \times 2^b \quad (6)$$

## III. IMPLEMENTATION

Computation of the DCT
The 8 x 8 DCT coefficient matrix can be written as

$$C(DCT)_{8\times 8} = \begin{bmatrix} a & a & a & a & a & a & a & a \\ b & d & e & g & -g & -e & -d & -b \\ c & f & -f & -c & -c & -f & f & c \\ d & -g & -b & -e & e & b & g & -d \\ a & -a & -a & a & a & -a & -a & a \\ e & -b & g & d & -d & -g & b & -e \\ f & -c & c & -f & -f & c & -c & f \\ g & -e & d & -b & b & -d & e & -g \end{bmatrix}. \quad \ldots..(7)$$

Even rows of C are even-symmetric and odd rows are odd-symmetric. Therefore by exploiting this symmetry in the rows of C and separating even and odd rows we can get 1D-DCT as follows,

$$\begin{bmatrix} y_0 \\ y_2 \\ y_4 \\ y_6 \end{bmatrix} = \begin{bmatrix} a & a & a & a \\ c & f & -f & -c \\ a & -a & -a & a \\ f & -c & c & -f \end{bmatrix} \begin{bmatrix} x_0+x_7 \\ x_1+x_6 \\ x_2+x_5 \\ x_3+x_4 \end{bmatrix} \quad \begin{bmatrix} y_1 \\ y_3 \\ y_5 \\ y_7 \end{bmatrix} = \begin{bmatrix} b & d & e & g \\ d & -g & -b & -e \\ e & -b & g & d \\ g & -e & d & -b \end{bmatrix} \begin{bmatrix} x_0-x_7 \\ x_1-x_6 \\ x_2-x_5 \\ x_3-x_4 \end{bmatrix} \quad \ldots\ldots(8)$$

1D-DCT is written as follows,

$$\begin{bmatrix} y_0 \\ y_1 \\ y_2 \\ y_3 \end{bmatrix} = \begin{bmatrix} a & c & a & f \\ a & f & -a & -c \\ a & -f & -a & c \\ a & -c & a & -f \end{bmatrix} \begin{bmatrix} x_0 \\ x_2 \\ x_4 \\ x_6 \end{bmatrix} + \begin{bmatrix} b & d & e & g \\ d & -g & -b & -e \\ e & -b & g & d \\ g & -e & d & -b \end{bmatrix} \begin{bmatrix} x_1 \\ x_3 \\ x_5 \\ x_7 \end{bmatrix}$$

$$\begin{bmatrix} y_7 \\ y_6 \\ y_5 \\ y_4 \end{bmatrix} = \begin{bmatrix} a & c & a & f \\ a & f & -a & -c \\ a & -f & -a & c \\ a & -c & a & -f \end{bmatrix} \begin{bmatrix} x_0 \\ x_2 \\ x_4 \\ x_6 \end{bmatrix} - \begin{bmatrix} b & d & e & g \\ d & -g & -b & -e \\ e & -b & g & d \\ g & -e & d & -b \end{bmatrix} \begin{bmatrix} x_1 \\ x_3 \\ x_5 \\ x_7 \end{bmatrix} \quad ,\ldots\ldots(9)$$

$$\text{where} \begin{bmatrix} a \\ b \\ c \\ d \\ e \\ f \\ g \end{bmatrix} = \sqrt{\frac{2}{N}} \begin{bmatrix} \cos\frac{4\pi}{16} \\ \cos\frac{\pi}{16} \\ \cos\frac{2\pi}{16} \\ \cos\frac{3\pi}{16} \\ \cos\frac{5\pi}{16} \\ \cos\frac{6\pi}{16} \\ \cos\frac{7\pi}{16} \end{bmatrix}$$

| $Z_0$ | | $Z_4$ | |
|---|---|---|---|
| weight | value | weight | value |
| $-2^0$ | 0 | $-2^0$ | $A_1$ |
| $2^{-1}$ | $A_0+A_1$ | $2^{-1}$ | $A_0$ |
| $2^{-2}$ | 0 | $2^{-2}$ | $A_1$ |
| $2^{-3}$ | $A_0+A_1$ | $2^{-3}$ | $A_0$ |
| $2^{-4}$ | $A_0+A_1$ | $2^{-4}$ | $A_0$ |
| $2^{-5}$ | 0 | $2^{-5}$ | $A_1$ |
| $2^{-6}$ | $A_0+A_1$ | $2^{-6}$ | $A_0$ |
| $2^{-7}$ | 0 | $2^{-7}$ | $A_1$ |
| $2^{-8}$ | $A_0+A_1$ | $2^{-8}$ | $A_0+A_1$ |

Table 5.1

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Input data A0 and A1, the transform output Zee needs only one adder to compute (A0 + A1) and two separated ECATs to obtain the results of Z0 and Z4. Similarly, the other transform outputs Zeo and Zo can be implemented in proposed method-based forms using 10(=1 + 9) adders and corresponding ECATs. Consequently, the proposed 1-D 8-point DCT architecture can be constructed as illustrated in Fig. 3 using a DA-Butterfly-Matrix, that includes two DA even processing elements (DAEs), a proposed method odd processing element (DAO) and 12 adders/subtractors, and 8 ECATs (one ECAT for each transform output Zn). The eight separated ECATs work simultaneously, enabling high-speed applications to be achieved. After the data output from the proposed method-Butterfly-Matrix is completed, the transform output Z will be completed during one clock cycle by the proposed ECATs. In contrast, the traditional shift-and-add architecture requires Q clock cycles to complete the transform output Z if the proposed method-precision is Q-bits.

## IV. RESULTS:

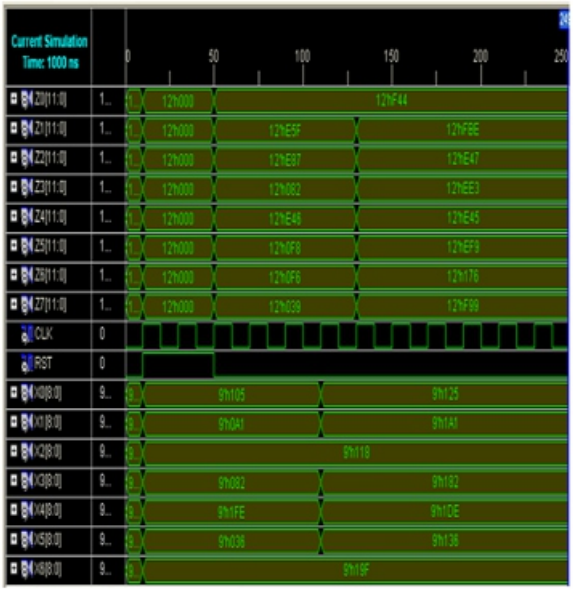


**Fig1: Simulation results of Distributed Arithmetic DCT**

DA-based DCT core with an error-compensated adder-tree (ECAT) program Modules will be taken to the Xilinx tool. The check syntax, synthesis and simulation completed successfully. The test bench written for main module, initially clock and reset pins set to '0' and all the inputs considered as '0'.After 10ns the reset pin set to '1' upto 40ns and we give the desired input values of 9-bit hexadecimal values then we obtain the 12-bit output values.

After 40ns the reset pin set to zero, similarly for 100ns and 200ns we give the input values and obtain the output values.

### Input Image

### Output resultant

| | Conventional (kb) | Proposed(kb) |
|---|---|---|
| Input.jpg | 10 | 2 |

## V. CONCLUSION:

The proposed method Discrete Cosine Transform (DCT) was designed successfully and the coding was done in Verilog HDL. The RTL simulations were performed usingxilinx. The synthesis was done using Xilinx ISE 12.3i DA DCT Design is verified for all test cases. The DCT works properly for all the test values.

## REFERENCES:

1. Y.Wang, J. Ostermann, and Y. Zhang, Video Processing and Communications,1st ed. Englewood Cliffs, NJ: Prentice-Hall, 2002.

2. Y. Chang and C.Wang, "New systolic array implementation of the 2-Ddiscrete cosine transform and its inverse," IEEE Trans. Circuits Syst.Video Technol., vol. 5, no. 2, pp. 150–157, Apr. 1995.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

3. C. T. Lin, Y. C. Yu, and L. D. Van, "Cost-effective triple-mode reconfigurable pipeline FFT/IFFT/2-D DCT processor," IEEE Trans. VeryLarge Scale Integr. Syst., vol. 16, no. 8, pp. 1058–1071, Aug. 2008.

4. S. Uramoto, Y. Inoue, A. Takabatake, J. Takeda, Y. Yamashita, H.Yerane, and M. Yoshimoto, "A 100-MHz 2-D discrete cosine transformcore processor," IEEE J. Solid-State Circuits, vol. 27, no. 4, pp.492–499, Apr. 1s992.

## Author's Profile:

**Eskala Divya Teja**, Pursuing M.Tech (VLSI), Global College of Engineering & Technology, Kadapa, Andhra Pradesh, India.

**Y.Maheswar,**M.Tech,(Ph.D), Associate Prof.,Department of ECE,Global College of Engineering & Technology,Kadapa, Andhra Pradesh,India