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Improved DDR3 SDRAM with Added Proficiencies

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ABSTRACT

Operating memory for faster applications is required for the advanced computer systems. For advance memory technology for the fast searching and high speed applications at present we use the DDR3 SDRAM as the alternative approach but it goes back word by its timing specifications. In order to provide the proper schedule transactions for the high end multibank parallel systems we proved the novel method with advance features like CAM memory utilization for fast searching applications which able to perform the hole search operation in single clock cycle, it is lot faster than RAM in almost all search applications.

INTRODUCTION

In present electronic engineering, DDR3 SDRAM or double-data-rate three synchronous dynamic random access memories is well used memory technology for high bandwidth storage of the exploiting data of a computer or early digital electronic devices.

DDR3 is piece of the SDRAM category of technologies and is one of the many DRAM (dynamic random access memory) implementations. The DDR3 SDRAM is similar to that of the traditional previous DDR SDRAM principles and designing.The major advantage of DDR3 has the ability to transfer the data 8 times faster between the cells this much faster bus transfer rate and high pipelined stage compare to the previous versions. Which gives the less latency related to that of the operations. In accession, the DDR3 criterion allows for chip capacities of 512 megabits to 8 gigabits, in effect enabling a maximal memory module size of 16 gigabytes.

This paper distributed as the Introduction at session I, DDR technologiesin session II followed by the content-addressable memory (cam), IV deals proposed design, next session can be results and discussions and followed by the conclusion and references

DDR TECHNOLOGIES

Double Data Rate-SDRAM (DDR) was designed to exchange SDRAM. DDR was originally stated to as DDR-SDRAM or simple DDR1. When DDR2 was brought in, DDR became referred to as DDR1. Names of constituents constantly change as novel technologies are introduced, especially when the advancement in previous method.

The concept introduced in DDR as the name implies “double data rate” the transferring the data at both rising and falling edges of the reference digital pulse. Where as in the previous method the data transfer were happened only ones per reference digital pulse.

In DDR, transfers of data twice faster than SDR because transferring data on both the rising and falling edges of the reference digital pulse.

DDR2 is the next coevals of memory arose after DDR.DDR2 enhanced the data transfer rate often called as bandwidth by increasing the operational frequency to cope with the high FSB frequencies and by doubling the prefetch buffer data rate. There will be more concerning the memory prefetch buffer data rate later in this section.

DDR2 is a 240 pin DIMM design which can be able to operate at 1.8 volts. Often in lower voltage counters

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can affect heat for higher frequency data transfer. DDR2 uses a dissimilar motherboard socket than DDR, and is not simpatico with motherboards designed for DDR.

The DDR2 DIMM key and DDR DIMM key are not aligned. If we inserted DDR2 socket in DDR causes the damage of the memory because the excess of the voltage.

DDR3 introduced in 2007 as the next generation to DDR2. DDR3 enhanced the data transfer rate often called as bandwidth by increasing the operational frequency than DDR2 to cope with the high FSB frequencies and by doubling the prefetch buffer data rate. There will be more concerning the memory prefetch buffer data rate later in this section.

The operating voltage is lowered to 1.5v to reduce the heating effect by increasing the high frequency. Whereas DDR3 is also projected with 240 pins, but the notched key is positioned differently to avoid insertion in motherboard RAM socket which is designed for DDR2

CONTENT-ADDRESSABLE MEMORY (CAM)

Content-addressable memory (CAM) is one of the special types of computer memory used in several very high speed searching applications. It is also familiar as associative memory, associative storage, or associative array, whilst the last term is more frequently used for a programming data structure.

Hardware associative array:

Dissimilar to traditional computer memory (random access memory or RAM) in which the user renders a memory address and the RAM brings back the data word stored at that address, Whereas CAM is designed such a way when user supplies a data word then CAM searches its entire memory to see whether same data word stored anywhere in it.

If certain data word found, the CAM produces the list of one or more storage addresses where the word was ascertained.

PROPOSED METHOD

The operational block diagram of the DDR3 controller is shown in below figure. The architecture of DDR3SDRAM controller comprises of Initialization FSM, Command FSM, data path, Address FIFO, command FIFO, bank control, clock counter, refresh counter, Wdata FIFO and R_data reg.

Initialization FSM affords proper i-State to initialize the modules in the design. Command FSM concedes c-State to execute the normal write, read and fast write, read operations. The data path module performs the data latching and sending off the data between Hash CAM unit and DDR3SDRAM banks

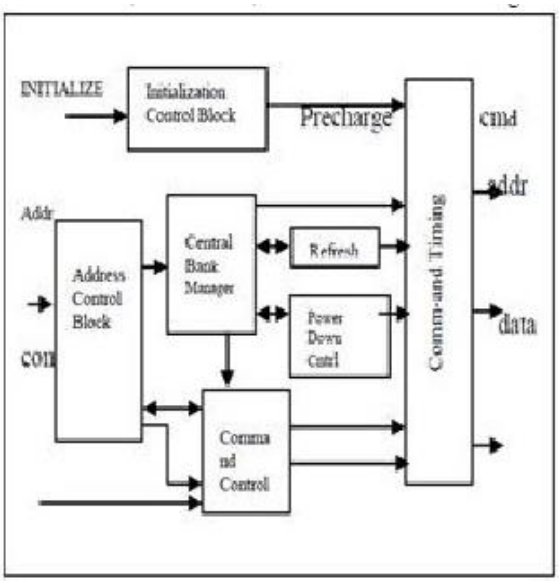

Fig1. Block diagram of DDR3SDRAM

The Address FIFO provides the address to the Command FSM so the bank control unit can open specified bank and particular address location in that bank.

The Wdata FIFO used to provide the normal and fast write operational data to the data path module

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The R_datareg acquires the data from the data path module normal and fast read operation.

In our proposal we projected DDR3 controller provides interface to the HASH CAM circuit and the DDR Memory Banks, in CAM memory when user supplies a data word then CAM searches its entire memory to see whether same data word stored anywhere in it. If certain data word found, the CAM produces the list of one or more storage addresses where the word was ascertained.Because a CAM is designed to explore its entire memory in a single operation, it is lot faster than RAM in almost all search applications.The DDR3 controller fetches the corresponding address, data and control words from the HASH CAM circuit in to the Address FIFO. Write data FIFO and control FIFO.

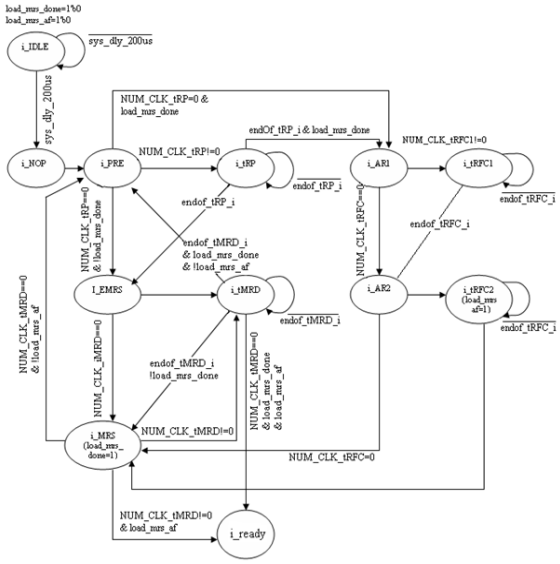

Fig2.Initial FSM State Diagram

Before normal memory accesses to be executed, DDR3 must to be initialized by successive commands. The INIT_FSM state machine deals this initialization.

Figure 2shows the state diagram of the INIT_FSM. During reset, the INIT_FSM is accreted to the i_IDLE state. since reset, the sys_dly_200US signal will be sampled to ascertain if the 200µs power/clock stabilization delay is accomplished. After the power/clock stabilization is finish, the DDR initialization sequence will begin and the INIT_FSM will shift from i_IDLE to i_NOP state and in the next clock to I_PRE.

The initialization commenced with the PRECHARGE ALL command. Later a LOAD MODE REGISTER command will be imposed for the extended mode register to enable the DLL inside DDR, abided by another LOAD MODE REGISTER command to the mode register to reset the DLL. Then a PRECHAGE command will be enforced to make all banks in the device to idle state. Then two, AUTO REFRESH commands, and later the LOAD MODE REGISTER command to configure DDR to a particular mode of operation.

After accretion of the LOAD MODE REGISTER command and the tMRD timing delay is quenched, INIT_FSM goes to i_ready state and stays there for the normal memory access cycles until reset is insisted.

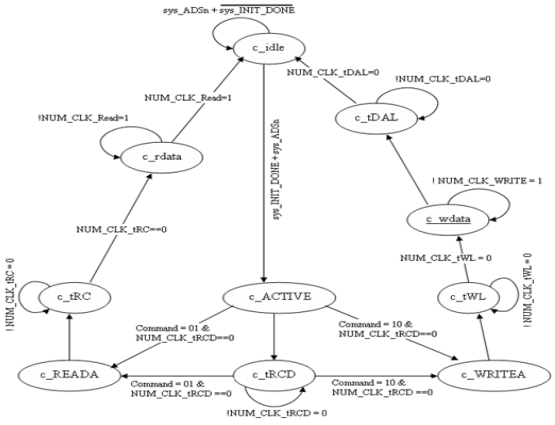

Fig3. Command FSM State Diagram.

The figure3 evinces the state diagram of CMD_FSM, which covers operations such as read, write and refresh of the DDR. The CMD_FSM state machine is initialized to c_idle on reset.After reset, CMD_FSM stays in c_idle as long as sys_init_done is active low which describes the DDR initialization succession is not yet finished.From this state, a READA/WRITEA/REFRESH cycle starts corresponding to sys_adsn/ rd_wr_req during ref_req signals as evinced in the state diagram.

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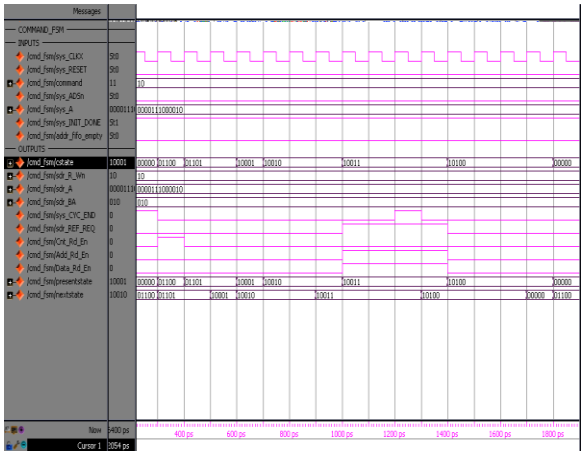
SIMULATION RESULTS

As discussed above our design unit can perform the different operations such as normal read, write and fast read operations.

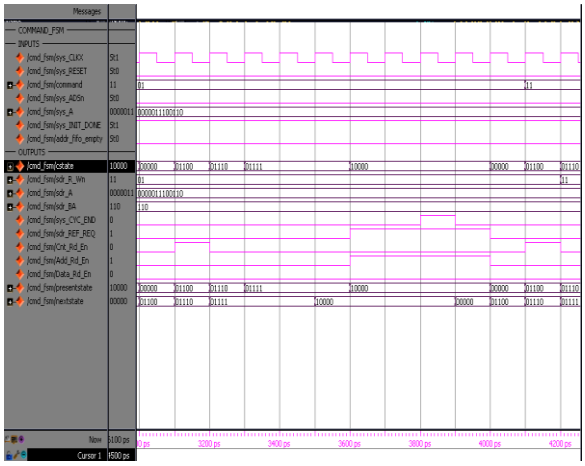
In order to perform the different operations the command word can be used when command word 01 it performs the normal read operation, if command word is 10 it performs the normal write and command word is 11 it performs fat read operation

Normal Write operation



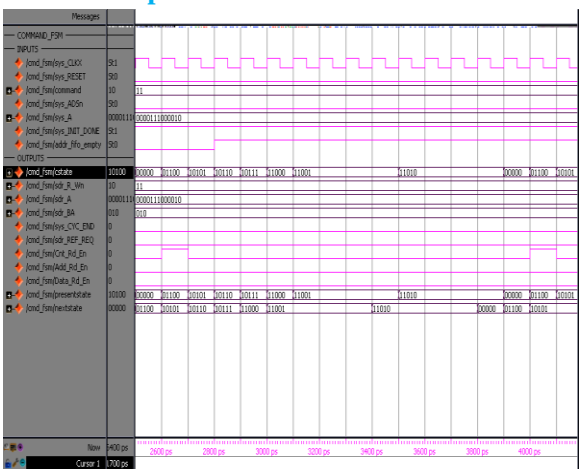
When we applied data, address and command word for the normal read operation, from the above we can see the i_states and the c_states when c_state is in normal read(5'b01110) it performed read.

Normal Read operation



When we applied data, address and command word for the normal write operation, when c_state is in normal write (5'b10001) it performed write.

Fast Read operation



When we applied data, address and command word for the fast read operation, from the above we can see the i_states and the c_states when c_state is in fast read (5'b10101) it performed fast read and it provided the similar data stored in memory.

CONCLUSION

In this thesis we have designed a novel High speed DDR3 SDRAM Controller with 64-bit data transfer which contemporizes the transfer of data among DDR RAM and External peripheral devices such as host computer, laptops and so on. The advantages of this controller compared pervious DDR3 SDRAM is that the production cost is also very low and more over in our concept we introduces the CAM memory for fast searching applications. We have successfully designed using Verilog HDL and simulated using ModelSim, synthesized using Xilinx tool

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