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Implementation of Low Power Six Transistor Embedded Memory SRAM and ROM

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Abstract:

Performance of sense amplifiers has considerable impact on the speed of caches used in microprocessors. A small difference in voltage level of bit lines of memory cell is amplified by the sense amplifier. Due to higher density of memory, the bit line capacitance increases and that limits the speed of voltage sense amplifiers. Current sense amplifier which is independent of bit line capacitance is a good choice in high density RAM. Under the aegis of the Moore's law, we have to deal with its darker side with problems like leakage and short channel effects. Once we go beyond 45nm regime, process variations have emerged as a significant design concern. Process variation induced mismatches in sense amplifiers lead to significant loss of yield for that we need to come up with process variation tolerant circuit styles and new devices. Multiple sense amplifier techniques - in addition to the conventional voltage sense amplifier. It analyzes current sense amplifier, charge transfer sense amplifier as wells as current latched sense amplifier and compares them in speed and power consumption to the voltage sense amplifier. All the sense amplifiers are also analyzed in the presence of process variations and some reported FET based techniques are implemented in planar MOSFET technology to combat mismatch. All circuits are designed and simulated in a 45nm process technology using Ng-Spice circuit simulator.

Keywords: ***Delay, Power dissipation, Sense amplifiers-VSA, CSA, CTSA***

I.INTRODUCTION

Static Random Access Memories (SRAMs) are an important component of microprocessors and system-on-chips. SRAMs are used as large caches in microprocessor cores and serve as storage in various system-on-chips like graphics, audio, video and image processors. SRAMs used in high performance microprocessors and graphics chips have high speed requirements.

At the same time, SRAMs used in application processors which go into mobile, handheld and consumer devices have very low power requirements. Since SRAMs serve as large storage on these chips, it's very important to get maximum density out of these. Traditionally a large number of SRAM bit cells, up to 1024 in some cases, are connected to a common bit-line to get the highest density and array efficiency. This results in a large capacitance on the bit-lines which necessitates using differential sense amplifiers for speed reasons. Sense amplifiers detect the data being read by sensing a small differential voltage swing on the bit-lines rather than waiting for a full rail-to-rail swing. Depending on the performance and power requirements, it's very important for the sense amplifiers to operate fast and do so while burning a minimum amount of power.

The large bit-line capacitance is a big performance bottleneck. Conventional Voltage Sense Amplifiers need a minimum amount of differential voltage to be developed on the bit-lines for reliable operation. The amount of time required to develop this differential voltage is linearly proportional to bit-line capacitance.

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The dynamic power consumed in pre-charging the bit-lines increases with the differential voltage that needs to be developed. Low power requirements of mobile and embedded chips require sense amplifiers which burn less power than the traditional voltage sense amplifier techniques.

From the past few decades, the growth of the electronics industry is very fast and also the use of integrated circuits in computing, telecommunications and consumer electronics. In the 1958, there was only a single transistor on the chip called single transistor era and at present day ULSI (Ultra Large Scale Integration) systems with more than 50 million transistors in a single chip. Today the size of the memory is decreasing and the storing capacity is increasing. As the storing capability increased, the time response for the data writing and reading from the memory should be very fast. The speed gap between the MPUs and memory devices has been increased in the past decade. The MPU speed has improved by a factor of 4 to 20 in the past decade. On the other hand, in spite of the exponential progress in storage capacity, minimum access time for each quadrupled storage capacity has improved only by a factor of two. In the memory, it is common to reduce the voltage swing on the bit lines to a value significantly below the supply voltage. This reduces both the propagation delay and the power consumption. Noise and other disturbances may be occurred in the memory array, for this sufficient noise margin is obtained even for these small signal swings. During the interfacing of the memory to the external field, the amplification of the internal swing is required. This is achieved by the sense amplifiers. Design of a high performance and efficient sense amplifier is very important to design SRAMS but with increasing parameter variations, the developing of a reliable and fast sense amplifier is a big challenge in itself. Sense amplifiers play a major role in the functionality, performance and reliability of memory circuit. In a large embedded SRAM there may be many thousands of sense amplifiers and each one of them will have a very high yield requirement for the product to have a good overall yield. A single failing sense amplifier implicates the whole memory but as technology becomes more and more advanced and Moore's law still governing the semiconductor industry, the control of process variations and manufacturing uncertainty becomes more and more critical. The sense amplifier performance degradation due to process variation and resulting yield loss is more pronounced than before.

It is important for the designer to be able to understand mismatch effects, since sensing should be done as fast as possible, subject to sensitivity constraints imposed by the parameter variations inherent in fabrication processes. Despite careful designing, small variations in parameters like threshold voltage and effective channel length due to process operating conditions [4], lead to an input offset which affects the performance of the sense amplifier. The analysis of these variations provides a good understanding of the impact of device mismatches in differential sense amplifier. To guarantee reliability of the sense amplifiers either we have to come up with new process variation tolerant circuit styles, techniques or the replacement of conventional bulk type MOSFET.

This work explores multiple sense amplifiers – Current Sense Amplifier (CSA), Charge Transfer Sense Amplifier (CTSA), and compares them in speed and power to the Voltage Sense Amplifier (VSA). A current sense amplifier operates by sensing the bit cell current directly rather than waiting on a differential voltage to develop on the bit-lines. The operation of charge transfer sense amplifier is based on charge sharing from the high capacitance bit-lines to the low capacitance sense amplifier nodes. This also is presents the design of a six transistor bit cell which is used in all the experiments. All work is done in 45nm CMOS technology with a 1V supply. The sense amplifier designs are evaluated in a 128x128 SRAM array with 128 bit cells on the word-line and 128 bit cells connected to the bit-line.

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II. RELATED WORK

Modern digital systems require the capability of storing large amount of data information with high speed. Memories circuits or systems store digital information in large extent. Memory circuits are of different types like, SRAM, DRAM, ROM, EPROM, EEPROM, Flash and FRAM, each form has a different cell design, the basic structure and organization. Reliability and power dissipation are large concern of the semiconductor memory designer. The propagation delay and the power consumption of the memory cell can be reduced by lowering the voltage swing on the bit lines. By reducing the voltage on the bit lines there will be a very small difference between bit lines and it will be very difficult to differentiate logic "0" and logic "1" on the bit lines. This problem is eliminated and better results are achieved by the Sense Amplifier.

2.1 Static Random Access Memory (SRAM)

The most compelling issue in designing large memories is to keep the sizes of the cell as small as possible, this should be done so that other important design qualities such as speed and reliability do not highly affected. There are different type of memories like read only, volatile, non-volatile, and read-write memories. Here, only SRAM is discussed. RAM is a volatile memory. The data stored in this memory is lost when the power supply is switch off. It retains its memory patterns for as long as power is being supplied. Basically, RAM can be classified into two categories:-

1. Static RAM (SRAM)
2. Dynamic RAM (DRAM)

SRAM utilizes a flip flop mechanism. It does not need to refresh as DRAM. A block diagram of RAM is shown in Fig.1.At the intersection of row line (word line) and column line (bit line) is a memory cell. Some peripheral circuits like latches, decoders and buffers are used to select particular memory cell from the array provided row and column addresses. Sense amplifiers are included for the full swing output voltage level after reading the data on memory cells.

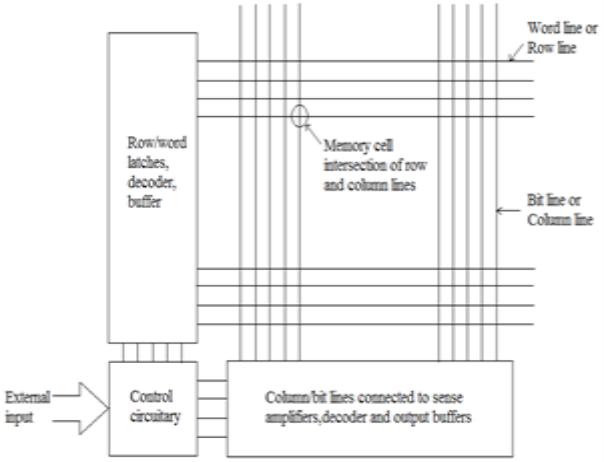

Figure 1 Block diagram of RAM.

The SRAM cell should be sized as small as possible to achieve high memory densities. A 6T SRAM is shown in Fig.2. It is made of six transistors so it is called 6T SRAM. In this 6T SRAM two inverters (M1, M2 and M3, M4) are cross coupled. Each bit of data is stored on these four transistors in an SRAM cell. This storage cell has two stable states which are as "0"and "1". Two additional access transistors M5 and M6 are used to control the access to a storage cell during read and write operations and these are connected to the bit lines and word line. For the accurate operation the size of the transistors are designed properly.

2.1.1 6T SRAM cell

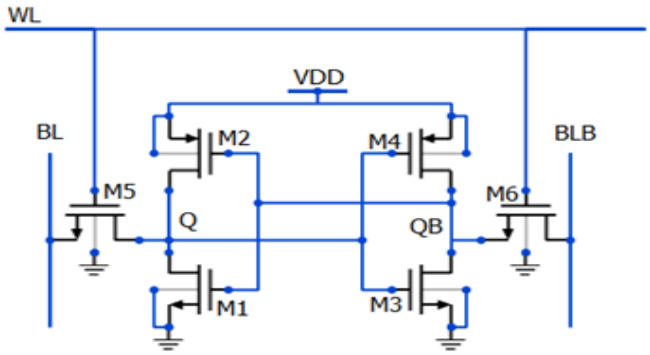

Figure 2 Six-transistor CMOS SRAM cell.

2.1.2 CMOS SRAM Read Operation

Assume that a "1" is stored at Q, so the "0" will be at QB. Both the bit lines are pre-charged to VDD. Read cycle will not start until the word line is low. As the

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word line will be high, both the access transistors M5 and M6 will be turned on and the read cycle initiate. During a correct read operation, the values stored in Q and QB are transferred to the bit lines by leaving BL at its pre-charge value and by discharging BLB through M1-M5. As the "1" is stored at Q, due to which the transistor M1 will be turned ON and the transistor M3 will be turned OFF as the "0" is stored at QB. Transistor M5 is already on due to high word line, a direct path will be forms between BLB and ground as both the transistors M1and M5 are ON. Now the BLB will be discharged through transistors M1 and M5. BL remains high in this case and BLB is discharged and it takes long time to reach ground level due to high bit line capacitance. Therefore, sense amplifier is needed to amplify the differential voltage of bit lines to full swing voltage levels at the faster rates.

2.1.3 CMOS SRAM Write Operation

For the proper SRAM write operation, assume that a "1" is stored in the cell Q, and then the value stored at QB will be "0". Due to the values stored at Q and QB, transistors M2 and M3 will be turned off. As the word line becomes high, the write cycle will start. Now, for the value "0" is to be stored at Q, bit line BL is kept at "0".By keeping the proper sizes of the transistors, the transistor M6 will discharge the node Q very fast as compare to the charging of the node by transistor M4. Due to the fast discharging of the Q, a value "0" will be set at this node.

2.2 Sense Amplifiers

2.2.1 Voltage Mode Sense Amplifier (VSA)

Sense amplifier which detects the voltage difference on the bit lines is called voltage mode sense amplifier. There are some voltage mode sense amplifiers like single ended sense amplifiers, differential amplifiers and Cross-coupled sense amplifiers. Different types of sense amplifier are used in different types of memory cells according to the proper design and efficient performance.

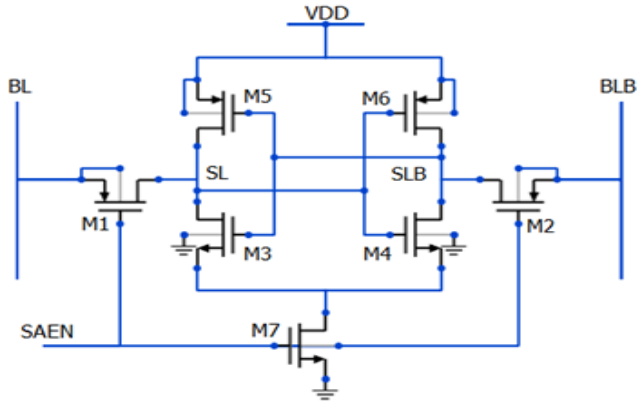

Figure .3 Cross-coupled voltage modes SA.

Fig.3 shows the schematic of Cross-coupled voltage mode SA. M1 and M2 are the access transistors, whereas M3-M6 forms cross-coupled inverters. When SAEN is low, M1 and M2 are turned ON and voltage on BL and BLB will be transferred to SL and SLB respectively. Due to positive feedback, higher voltage level goes to VDD and other level goes towards zero. In the basic cross-coupled SA, the nodes SL and SLB are input and output terminals at the same time. Therefore, the circuit cannot be connected directly to the bit line. Since the circuit would attempt to discharge the bit line capacitance during the decision phase and would increase delay and power. A solution is either to separate the bit line by a multiplexer or to use pass gates, forming a decoupling resistor. Both devices cause a voltage drop that deteriorates the available input voltage difference. This way the voltage swing at the bit lines can easily reduce by half, resulting in lower speed and noise margin.

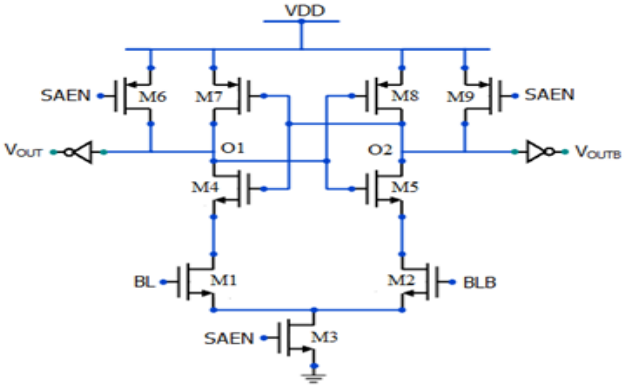

Figure 4 Current latched voltage mode SA.

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III. SENSE AMPLIFIER DESIGN AND SIMULATIONS

This topic shows the designing and simulations of 6T SRAM cell and different sense amplifiers. Simulations are carried out for 45nm CMOS technology Predictive Technology Model (PTM) using NGSPICE circuit simulator. In all sense amplifiers, total width of all the transistors is kept nearly same for fair comparison.

3.1 6T SRAM cell Design

The read operation exposes storage nodes of the bit cell to the pre-charged bit-lines. Under this condition, the data stored in the bit cell should not change. This is known as read stability and is an important factor to be considered while designing the bit-cell. During a read operation, the storage node which has a "0" on it rises in voltage due to voltage divider action between the pass-gate and pull- down transistors. This voltage must remain below the trip point of the cross coupled inverter to ensure internal state is not changed. The level of voltage increase at the internal node is decided by the ratio of the current of the drive transistor M1 (or M3) to that of the access transistor M5 (or M6) in Fig.2. The current ratio between drive transistor and access transistor is called the cell-ratio of the SRAM bit cell. With a large cell-ratio, the voltage on the low state node can be kept low, enhancing read stability of the bit cell. At the same time, increasing cell-ratio also increases the area of the bit cell. Usually, a cell-ratio of 1.5 ~ 2 minimizes bit cell area while ensuring some level of read stability. Writ ability refers to the requirement that data on bit-lines must change the internal nodes of the bit cell within a specified time. This depends on the ratio of currents of the M2 (or M4) and M5 (or M6) transistors. To easily switch the internal node voltage to ground, the current of M5 (or M6) should be larger than that of M2 (or M4). This ratio is called the pull-up ratio, and indicates how easily the data can be changed by the low state bit-line. Pull-up ratio depends on both PMOS and NMOS currents, hence mobility must be considered while sizing the transistors. If NMOS mobility is twice PMOS mobility, same transistor widths can be used for M2 (or M4) and M5 (or M6) for a pull-up ratio of 0.5.

TABLE 1:6T SRAM CELL

	Width (µm)	Length (nm)
M5,M6,M10,M11	0.25	50
M3,M4	1	50
M1,M2,M8,M9	2	50
M7	4	50

3.2 Design and Simulation of VSA

The voltage sense amplifier circuits of Fig.3 and 4 were tuned and the following transistor sizes were arrived at as shown in Table.

TABLE 2: VOLTAGE SENSE AMPLIFIER

	Width(µm)	Length (nm)
Pull-Up Transistors (M2,M4)	1	50
Pull-Down (M1,M3)	1.5	50
Access Transistors (M5,M6)	1	50

	Width (µm)	Length (nm)
M1,M2,M5,M6	1	50
M3,M4	2	50
M7	3	50

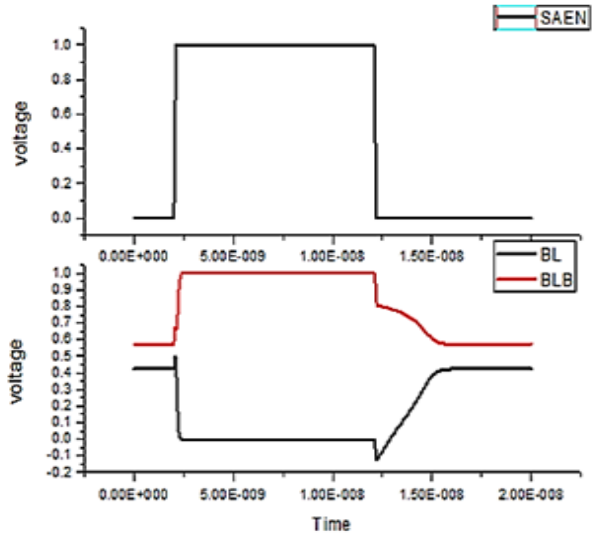

Figure 5

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The NMOS devices M3 and M4 in the cross coupled inverter pair as well as the enable device M7 need to be sized for speed since they are in the critical discharge path. From a raw performance standpoint, you get a few picoseconds of speed improvement if the M7 device is sized higher and the N1/N2 devices correspondingly sized smaller than the numbers given above. But higher widths on M3 and M4 are very important due to process variations as described in [11]. Due to process variations like random doping fluctuations, Vt of transistors have random variations which cause mismatch among neighboring transistors. This can induce trip point mismatch among the cross coupled inverters of voltage sense amplifiers, resulting in operational failures. The initial voltage difference at the output nodes created by bit-line voltage difference may not result in the flipping of the cross-coupled inverters in the right direction if there is sufficient trip point voltage mismatch to offset the difference. Up sizing widths of M3 and M4 is effective in reducing the failure probability because it reduces Vt variation and hence trip point mismatch. Increasing the width of M7 does not lower failure probability because it is a common transistor for the two paths and its variation affects both paths equally. Fig.8 shows simulation results of current latched sense amplifier trying to read data of memory cell containing logic "1". When word line WL is high to access the memory cell, BLB starts to discharge from VDD and BL remains high. After SAEN is asserted, cross coupled inverters amplify small differential voltage between bit lines to full rail output as shown in Fig.8. Here, due to higher BL voltage M1 has higher current. So, O1 discharges faster than O2 and we get logic high after inverted by inverter.

3.3 Design and Simulation of CSA

TABLE 3: CURRENT SENSE AMPLIFIER

	Width (µm)	Length (nm)
M1,M2,M3,M4,M5,M6	0.1	50
M7,M8	0.25	50
M9,M10	2	50
M11	3	50

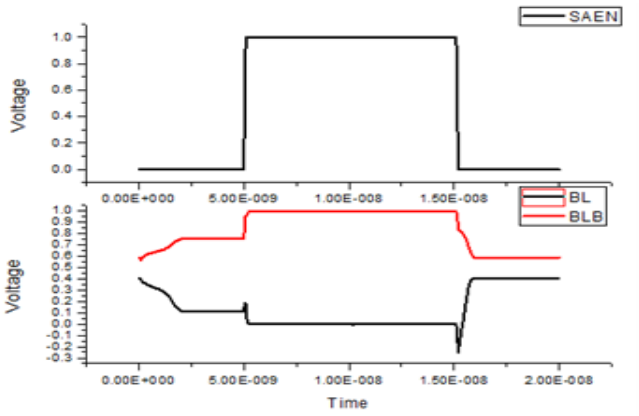

Figure 6

3.4 Design and Simulation of CTSA

TABLE 4: CTSA

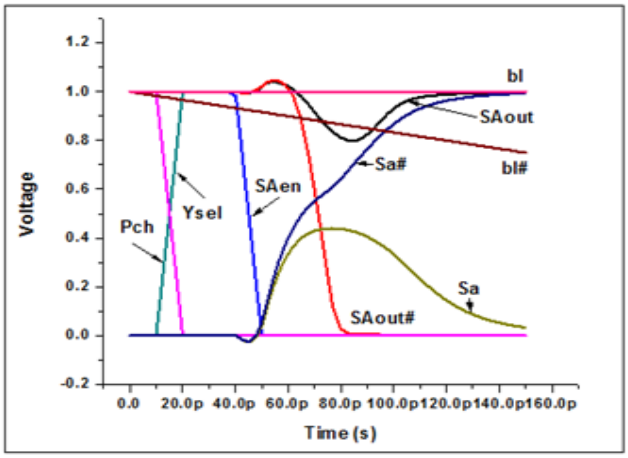

Figure 7

The charge transfer sense amplifier circuit was designed with the transistor sizes as shown in Table 4. The bias voltage Vb is set at 0.3V. It is critical to set this voltage at the right value as the charge transfer device M1/M2 cuts off when its input source voltage falls to Vb+Vtp. Setting Vb at a higher value causes the charge transfer device to be cut off early and not have the differential voltage propagate to the sense nodes Sa and Sa#. Setting this voltage too low prevents the charge transfer device from entering the sub-threshold region and causes the cross coupled positive feedback inverter to further discharge the bit-line resulting in higher pre-charge power. Fig.10 shows simulation waveforms of charge transfer SA.

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3.5 Wave forms of Sense Amplifiers

All three types of sense amplifiers are simulated in 45nm technology using NGSPICE. Below figures shows performance summary of these sense amplifiers.

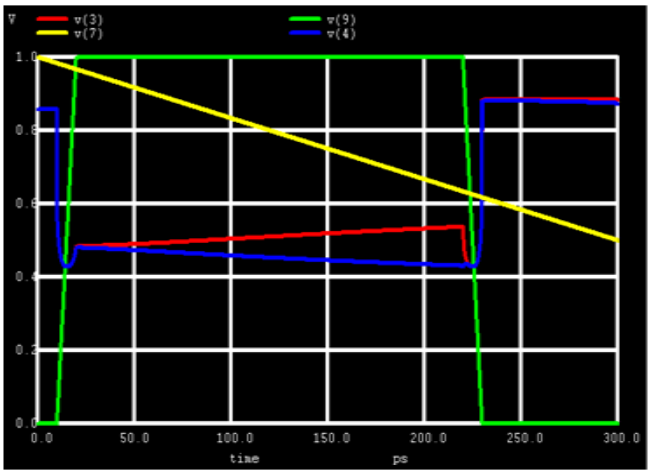

Figure 8 Cross coupled VSA

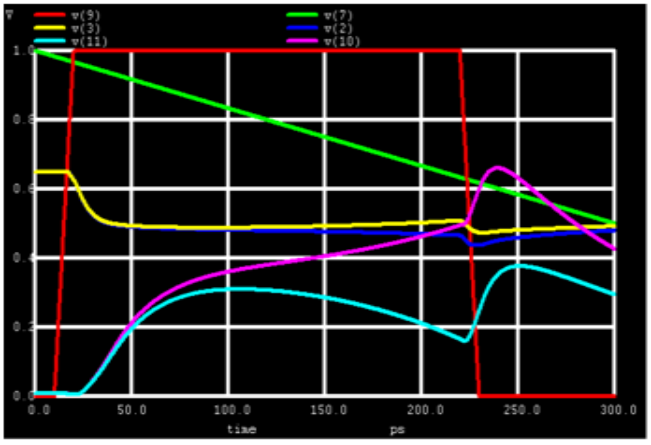

Figure 9 Current latched VS

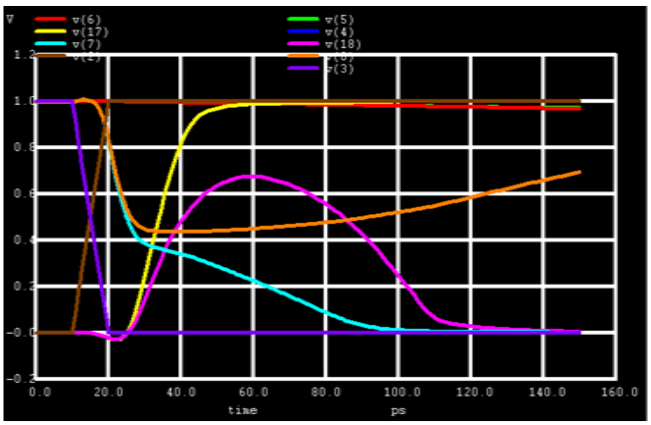

Figure 10 current modes SA

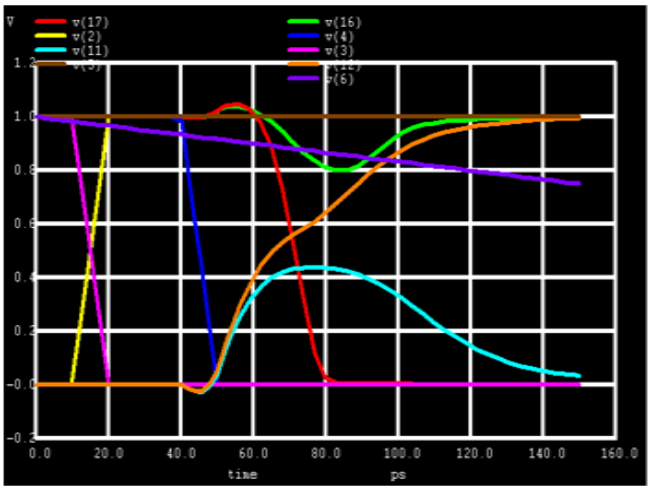

Figure 11 Charge transfer SA

IV. CONCLUSION AND FUTURE WORK

This work presented the design and analysis of three different sense amplifier topologies – Voltage Sense Amplifier (VSA), Current Sense Amplifier (CSA) and Charge Transfer Sense Amplifier (CTSA). The sense amplifiers were compared and characterized to find out their relative performance without and with process variation in transistors. The sense amplifiers were analyzed in a 128x128 SRAM array for which a 6T SRAM bit cell was designed. All work was done on 45nm CMOS technology. This work shows that among the three topologies, charge transfer amplifier is the best choice with minimum delay and power dissipation. Current sense amplifier is faster than VSA with reduction in delay. But it consumes more power dissipation than VSA and CTSA. Charge transfer sense amplifier shows reduction in delay and reduction in power dissipation compared to VSA. But it has additional design complexity to decide bias voltage Vb. Because of the limitation of those techniques, such as increase in area, power and delay in case of no mismatch, other techniques should have been proposed to combat the process variation in sub100nm technology.

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