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DA- Based Reconfigurable Fir Digital Filter For Adaptive Coefficient Change Implementation

Kayala Nagamani
PG Scholar,
Dept of ECE,
Global College of Engineering & Technology,
Kadapa, YSR (Dt), AP, India.

S K Imam Basha
Assistant Professor,
Dept of ECE,
Global College of Engineering & Technology,
Kadapa, YSR (Dt), AP, India.

ABSTRACT:

In the majority of digital signal processing (DSP) applications the critical operations are the multiplication and accumulation. Real-time signal processing requires high speed and high throughput Multiplier-Accumulator (FIR) unit that consumes low power, which is always a key to achieve a high performance digital signal processing system.

The purpose of this work is to design and implementation of a low power FIR unit with block enabling technique to save power FIR filer needs multiplication and accumulation for generating output. Serial input and parallel output process has been implemented by DA-Algorithm for the filter response. To achieve the parallel response of the FIR Filter instead of serial response for the given serial input. Implemented by DA- Algorithm approach.

Index Terms :

Circuit Optimization, DistributedArithmetic (DA), Finite Impulse Response (FIR) filter, Reconfigurable Implementation.

I.INTRODUCTION:

Digital signal processing (DSP) algorithm implementation on hardware requires efficient analysis of area and throughput with high performance and low cost. These algorithms on field programmable gate array (FPGA) provide programmable and dedicated hardware design by enabling fast digital circuit prototypes.

The FIR filters are linear filters that perform shifting, and multiplication operation for K filter taps and provides the output that depends on the present and past (k-1) input samples.

The FIR filters require k multiply and accumulate (MAC) operations. The MAC operation is replaced by look up tables (LUTs) and summations. In DA technique the LUT is used to store the pre-calculated sum of products and during each cycle the least significant bits of each tap is concatenated to form the address for the LUT.

The DA technique provides high throughput since it generates the filter output in least number of clock cycles that depends on the input bit precision. The elimination of hardware multipliers reduces the logic complexity in DA. Due to advancement in memory design technology, memory size is reduced, which makes the DA worth considerable.

II.RELATED WORK:

In recent years, a substantial amount of research work has been carried out in developing efficient architectures for digital FIR filter multipliers. The implementation of multiplier in FIR filters by decomposing the filter coefficients into shift-and-add operation has been studied well in the recent decades. In general, the multiplier performs constant multiplication with the input samples as the filter coefficients are constant in the digital filters. Several techniques for implementation of multiplier have been proposed and categorized in to three classes.

First, the sub-expression sharing (or elimination) aims to identify the recursive pattern of the filter coefficient representation. Second, the difference methods works on the basis of the difference exists between the coefficients and the new coefficients are generated by summing another coefficient. Third, the algorithms for multiplier block which computes the coefficients from the previous coefficients. Furthermore, lot of work focused on Multiplier less digit-serial FIR filters implementation on FPGA.

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In [17], data transition power diminution technique is employed to reduce the dynamic switching power on adders and booth multipliers for fir filter. In [18], the authors have presented an algorithm which reduces the hardware complexity of the multiplier block in the finite impulse response digital filters by reducing the adder depth. Especially, in [19] the trade-off due to digit-size has been studied with the usage of direct multiplier blocks. In [20], a hybrid scheme has been proposed by combining Minimal difference differential coefficients method with Common Sub-expression elimination in order to achieve further reduction in complexity.

III.DISTRIBUTED ARITHMETIC:

Distributed arithmetic (DA) is Associate multiplication-free technique for calculative inner product 1st introduced by Croisier, et al. and Zohar and any developed by Peled and Liu quite 3 decades past. The multiplication operation is replaced by a mechanism that generates partial product and so sums the product along. The key distinction between distributed arithmetic and commonplace multiplication is within the manner the partial product are generated and more along. Since its introduction, distributed arithmetic has been wide adopted in several digital signal process applications, as well as however not restricted to digital filtering, distinct trigonometric function remodel, and distinct Fourier model.

i. Mechanization of DA:

Consider the following inner product of two N dimensional vectors a and x, where a is a constant vector, x is the input sample vector, and y is the result.

$$y = \sum_{k=0}^{N-1} a_k x_k$$

Equation represents the distributed arithmetic computation. The values of bkn are either 0 or 1, resulting in the bracketed term.

$$\sum_{k=0}^{N-1} a_k b_{kn}$$

Since a could be a constant vector, the bracketed term is pre-computed and keep in memory exploitation either a search table (LUT) or memory board. for every bit depth, n, the search table is then addressed exploitation the individual bits of the input samples, xk that area unit usually keep in a very long register chain, and therefore the worth scan out is then accumulated, with the ultimate result y showing when B cycles. It's necessary to notice that with this implementation, despite the lengths of the vectors a and x, the ultimate result y is computed in B cycles.

IV.IMPLEMENTATION:

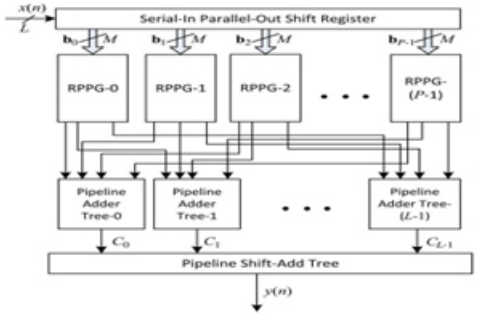

Fig. 1 Proposed structure of the high-throughput

DA-Based FIR filter for FPGA and ASIC implementation.

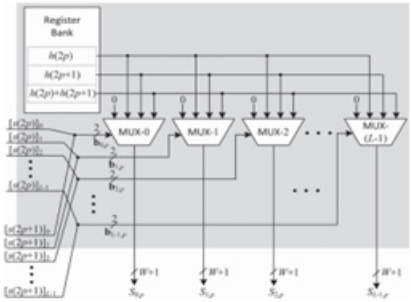

Fig.2 pth RPPG for M = 2.

V.SIMULATION RESULTS AND DISCUSSIONS:

ASIC Simulation:

Fig 3. ASIC implementation Top module result

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RPPG Simulation:

Fig 4. RPPG is the partial product generator of the coefficientsof each 2 bits.

PPA Simulation:

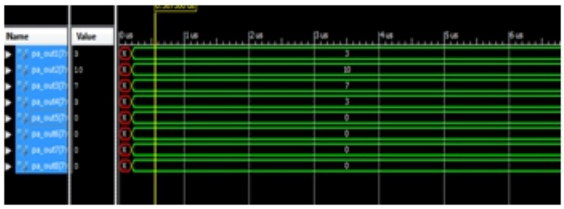

Fig 5. Parallel pipe line adder

FPGA Simulation:

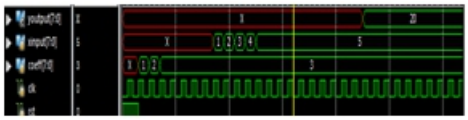

Fig 6. FPGA implementation of fir filter

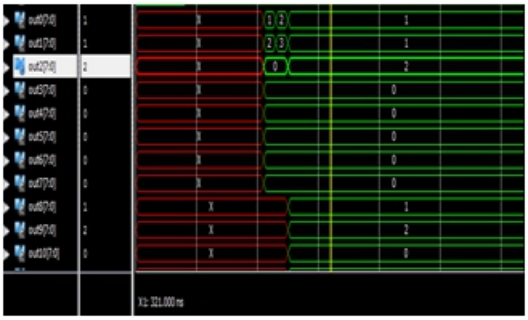

Fig 7. Out pins of the partial product result

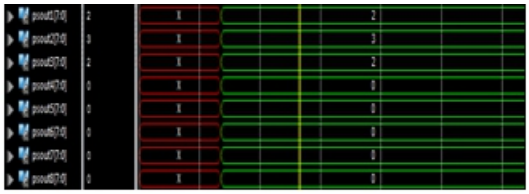

Fig 8. Shift and addition result of the psout

Fig 9. Final result of the FPGA implementation

PARAMETERS	PROPOSED	EXISTING
NO OF SLICES	283	508
NO OF LUTS	313	357
NO OF FLIPFLOPS	369	35

Fig 10. Comparison of Proposed with Existing

V. SUMMARY AND CONCLUSION:

The Distributed Arithmetic fir Transform (FIR filter Multiplier) was designed successfully and the coding was done in Verilog HDL. The RTL simulations were performed using Xilinx from Mentor Graphics. The synthesis was done using Xilinx ISE 9.2 DA fir filter Design is verified for all test cases. The DA fir filters works properly for all the test values.

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Author's Profile:

Kayala Nagamani, Pursuing M.Tech (**VLSI**), Global College of Engineering & Technology, Kadapa, Andhra Pradesh, India.

S Imam Basha, M.Tech, Assistant Professor at Global College of Engineering & Technology, Kadapa, Andhra Pradesh, India.