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Compensation of PQ Problem by DSTATCOM Using Resonant Power Conversion Technique

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Abstract:

A novel soft switching high frequency link converter for medium and high power ac-ac and ac-dc applications is proposed. The transient response of the distribution static compensator(DSTATCOM) is very important while compensatingrapidly varying unbalanced and nonlinear loads. Any change inthe load affects the dc-link voltage directly. The properoperation of DSTATCOM requires variation of the dc-link voltagewithin the prescribed limits. Conventionally, a proportional-integral(PI) controller is used to maintain the dc-link voltage to thereference value.The sudden removalof load would result in an increase in the dc-link voltage abovethe reference value, whereas a sudden increase in load wouldreduce the dc-link voltage below its reference value.

Key words:

DC-link voltage controller, distribution staticcompensator (DSTATCOM),load compensation, power factor, power quality (PQ).

I.INTRODUCTION:

The shunt-connected custom power device, called the distributionstatic compensator (DSTATCOM), injects currentat the point of common coupling (PCC) so that harmonicfiltering, power factor correction, and load balancing can beachieved. The DSTATCOM consists of a current-controlledvoltage-source inverter (VSI) which injects current at the PCCthrough the interface inductor. The operation of VSI is supportedby a dc storage capacitor with proper dc voltage acrossit. THE proliferation of power-electronics-based equipment,nonlinear and unbalanced loads, has aggravated thepower-quality (PQ) problems in the power distribution network.They cause excessive neutral currents, overheating ofelectrical apparatus, poor power factor, voltage distortion,high levels of neutral-to-ground voltage, and interference withcommunication systems [1], [2]. The literature records theevolution of different custom power devices to mitigate theabove power-quality problems by injecting voltages/currents or both into the system.One important aspect of the compensation is the extractionof reference currents. Various control algorithms are available in literature [3], [4] to compute the reference compensator currents.However, due to the simplicity in formulation and no confusionregarding the definition of powers, the control algorithmbased on instantaneous symmetrical component theory [5] ispreferred.

For the DSTATCOM compensating unbalanced and nonlinearloads, the transient performance of the compensator isdecided by the computation time of average load power andlosses in the compensator. In most DSTATCOM applications,losses in the VSI are a fraction of the average load power.Therefore, the transient performance of the compensatormostly depends on the computation of Plavg. In this paper,Plavgis computed by using a moving average filter (MAF) toensure fast dynamic response. The settling time of the MAF is ahalf-cycle period in case of odd harmonics and one cycle periodin case of even harmonics presence in voltages and currents.Although the computation of Pdcis generally slow and updatedonce or twice in a cycle, being a small value compared to Plavg,it does not play a significant role in transient performance ofthe compensator.

II.Design of DSTATCOM:

A DSTATCOM is a device which is used in an AC distribution system where, harmonic current mitigation,

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reactive current compensation and load balancing are necessary. The building block of a DSTATCOM is a voltage source converter (VSC) consisting of self-commutating semiconductor valves and a capacitor on the DC bus (Singh et al, 2008). The device is shunt connected to the power distribution network through a coupling inductance that is usually realized by the transformer leakage reactance. In general, the DSTATCOM can provide power factor correction, harmonics compensation and load balancing.

The major advantages of DSTATCOM compared with a conventional static VAR compensator (SVC) include the ability to generate the rated current at virtually any network voltage, better dynamic response and the use of a relatively small capacitor on the DC bus. The size of the capacitor does not play an important role in steady-state reactive power generation, which results in a significant reduction of the overall compensator size and cost (Ghosh et al, 2002; Padiyar, 2008). Fig. 1 shows the schematic diagram of a DSTATCOM connected to a three phase AC mains feeding three phase loads.

Three phase loads may be a lagging power factor load or an unbalanced load or non-linear loads or mixed of these loads. For reducing ripple in compensating currents, interfacing inductors (Lf) are used at AC side of the voltage source converter (VSC).A small series connected capacitor (Cf) and resistor (Rf) represent the ripple filter installed at PCC in parallel with the loads and the compensator to filter the high frequency switching noise of the voltage at PCC.

The harmonics/reactive currents (iCabc) are injected by the DSTATCOM to cancel the harmonics /reactive power component of the load currents so that the source currents are harmonic free (reduction in harmonics) and load reactive power is also compensated. The rating of the switches is based on the voltage and current rating of the required compensation.

For considered load of 35kVA, compensator data are given in Appendix, the rating of the VSC for reactive power compensation/harmonics elimination is found to be 25kVA (15% more reactive current from rated value). The selection of the DC bus voltage, DC bus capacitor, AC inductors and the ripple filter of DSTATCOM are given as,

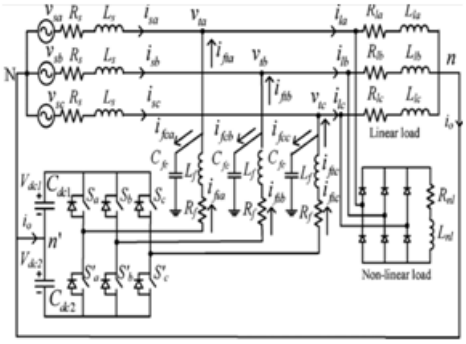

Fig 1: Circuit diagram of the DSTATCOM

III.CONTROL STRATEGY:

Generationof Reference Terminal Voltages:

Reference terminal voltages are generated such that, at nominal load, all advantages of CCM operation are achieved while DSTATCOM is operating in VCM. Hence, the DSTATCOM will inject reactive and harmonic components of load current.To achieve this, first the fundamental positive-sequence component of load currents is computed. Then, it is assumed that these currents come from the source and considered as reference source currents at nominal load. With these source currents and for UPF at the PCC, the magnitude of the PCC voltage is calculated. Let three-phase load currents ila(t),ilb(t), and ilc(t) be represented by the following equations:

$$i_{lj}(t) = \sum_{n=1}^{m} \sqrt{2}\, I_{lj\,n} \sin\left(n\,\omega t + \phi_{lj\,n}\right)$$

Where j = a, b, c represent three phases, n is the harmonic number, and m is the maximum harmonic order. ϕlan Represents the phase angle of the nth harmonic with respect to reference in phase- and is similar to other phases. Using instantaneous symmetrical component theory, instantaneous zero-sequence ilao(t), positive-sequence ila+(t), and negative-sequence ila-(t) current components are calculated as follows:

$$\begin{bmatrix} i_{la}^{0}(t) \\ i_{la}^{+}(t) \\ i_{la}^{-}(t) \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & \alpha & \alpha^2 \\ 1 & \alpha^2 & \alpha \end{bmatrix} \begin{bmatrix} i_{la}(t) \\ i_{lb}(t) \\ i_{lc}(t) \end{bmatrix}$$

Whereα is a complex operator.
The fundamental positive-sequence component of load current I+la1, calculated by finding the complex Fourier coefficient, is expressed as follows

$$\bar{I}_{la1}^{+} = \frac{\sqrt{2}}{T} \int_{0}^{T} i_{la}^{+}(t)\, e^{-j(\omega t - 90^{\circ})}\, dt$$

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I+la1is a complex quantity, contains magnitude and phase angle information.

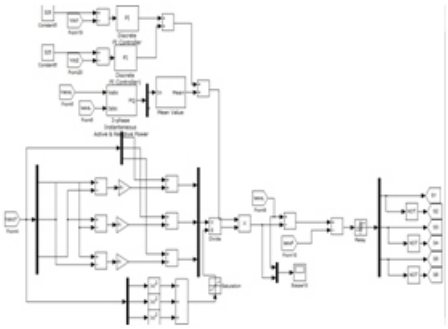

Fig 2: simulation circuit of control strategy

The fundamental positive-sequence component of load currents must be supplied by the source at nominal load. Hence, it will be treated as reference source currents. For UPF at nominal operation, the nominal load angle is used. By knowing, fundamental positive-sequence currents in phases and can be easily computed by providing a phase displacement of -2π/3 and 2π/3, respectively, and are given as

$$i^*_{sa} = i^+_{la1}(t) = \sqrt{2}\,|\bar{I}^+_{la1}|\sin(\omega t - \delta_0)$$
$$i^*_{sb} = i^+_{lb1}(t) = \sqrt{2}\,|\bar{I}^+_{la1}|\sin\left(\omega t - \frac{2\pi}{3} - \delta_0\right)$$
$$i^*_{sc} = i^+_{lc1}(t) = \sqrt{2}\,|\bar{I}^+_{la1}|\sin\left(\omega t + \frac{2\pi}{3} - \delta_0\right)$$

When reference source currents derived are supplied by the source, three-phase terminal voltages can be computed using the following equations:

$$v_{tj}(t) = v_{sj}(t) - L_s\frac{di^*_{sj}}{dt} - R_s i^*_{sj}$$

Let the rms value of reference terminal and source voltages be V*tand V, respectively. For UPF, the source current and terminal voltage will be in phase. However, to obtain the expression of V* independent of δo, we assume the PCC voltage as a reference phasor for the time-being. Hence, phase-a quantities, by considering UPF at the PCC, will be

$$v_{ta}(t) = \sqrt{2}\,V^*_t\,\sin\,\omega t$$
$$i^*_{sa} = \sqrt{2}\,|\bar{I}^+_{la1}|\sin\omega t$$
$$v_{sa}(t) = \sqrt{2}\,V\,\sin(\omega t + \delta_0)$$

The phasor equation will be

$$V^*_t\angle 0 = V\angle\delta_0 - (R_s + jX_s)\,|\bar{I}^+_{la1}|\angle 0$$

Simplifying the above equation

$$V^*_t = V\cos\delta_0 + jV\sin\delta_0 - |\bar{I}^+_{la1}|R_s - j|\bar{I}^+_{la1}|X_s$$

The expression for reference load voltage magnitude will be

$$v^*_{ta}(t) = \sqrt{2}\,V^*_t\,\sin(\omega t - \delta)$$
$$v^*_{tb}(t) = \sqrt{2}\,V^*_t\,\sin\left(\omega t - \frac{2\pi}{3} - \delta\right)$$
$$v^*_{tc}(t) = \sqrt{2}\,V^*_t\,\sin\left(\omega t + \frac{2\pi}{3} - \delta\right)$$

IV.SIMULATION RESULTS:

The load compensator with H-bridge VSI topology as shown in Fig. 3 is realized by digital simulation by using MATLAB.The load and the compensator are connected at the PCC. The acload consists of a three-phase unbalanced load and a three-phasediode bridge rectifier feeding a highly inductive R-L load. Adc load is realized by an equivalent resistance as shownin the figure. The dc load forms 50% of the total power requirement.

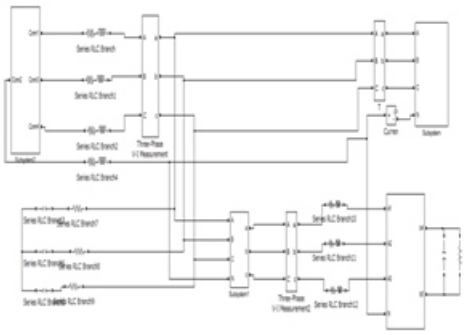

Fig 3: simulation diagram of proposed system:

By monitoring the load currents and PCC voltages, theaverage load power is computed. At every zero crossing ofphase voltage, is generated by using the dc-link voltagecontroller. The state-space equations are solved to compute theactual compensator currents and dc-link voltage. These actualcurrents are compared with the reference currents given by(1) using hysteresis current control. Based on the comparison,switching signals are generated to compute the actual state variablesby solving the state-space model given in (2). Theload currents have total harmonic distortions of 8.9%, 14.3%,and 21.5% in phases a, b and c, respectively. The unbalancein load currents results in neutral current as illustrated in the figure.

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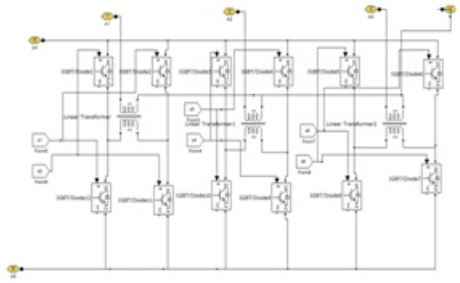

Fig 4: converter simulation design

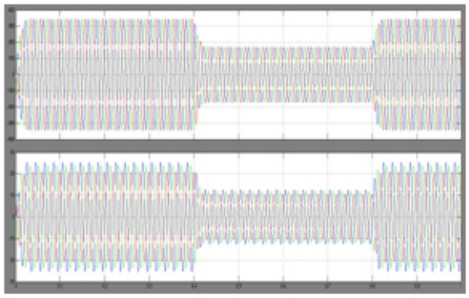

Fig 5: source voltage and source current

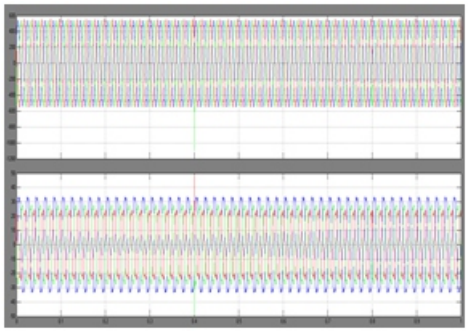

Fig 5: Load voltage and Load current

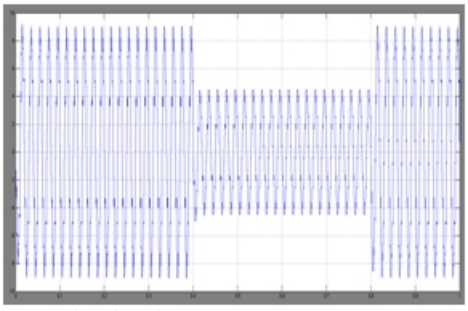

Fig 6: Line neutral current

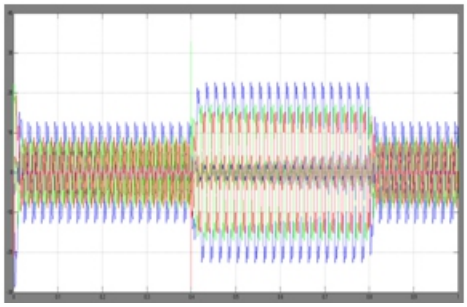

Fig 7: compensated currents

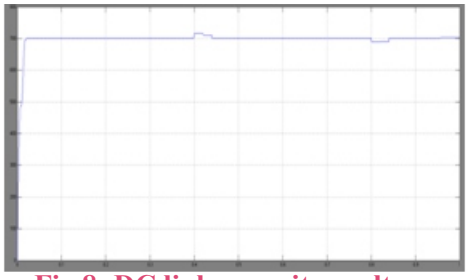

Fig 8: DC link capacitor voltage

V.CONCLUSION:

A VSI topology for DSTATCOM compensating ac unbalancedand nonlinear loads and a dc load supplied by the dc linkof the compensator is presented.In comparison with existing voltage control loops based on a voltage-reactive power droop characteristic, the proposed control ensures an accurate voltage regulation to a predefined voltage set point provided that the DSTATCOM rated power and the impedance of the ac network are large enough.The efficacy of the proposed controllerover the conventional dc-link voltage controller is establishedthrough the MATLAB simulation.

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