ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Design of PLL Using Multi Modulus Devide By 32/33 Prescaler in CMOS 45-Nm Technology

M.Mounika
M.Tech VLSI,
Department of ECE,
CMR Institute of Technology.

Mrs B.V. Krishnaveni M.Tech
Associate Professor,
Department of ECE,
CMR Institute of Technology.

Mr P. Raveen
Assistant Professor,
Department of ECE,
CMR Institute of Technology.

Abstract:

Today CMOS technology is widely used in Digital Electronic Devices. One of such Electronic devices is Phase-locked loop. A Wide range phase locked loop (PLL) is widely employed in wire-line and wireless communication systems. While realizing a PLL at higher frequencies static circuits cannot operate and dynamic circuits are required. A True Single Phased Clock (TSPC) divider is widely used to realize as a prescaler for this PLL.

A dual modulus prescaler contains logic gates and flip-flops. To fulfill the need of high frequency and low voltage circuit suitable flip flops must be selected. After realizing through prescaler, frequency division is done for PLL using pulse-swallow topology.

Normally prescalers will be of n/n+1 type. Divide-by-2/3 prescaler is implemented by TSPC and differential type of flip-flops. 32/33 prescaler is implemented by choosing various combinations of 2/3 prescaler and flip-flops. The main objective of this design is to implement a multi modulus prescaler and the flexible frequency counter in CMOS 45-nm technology.

Index Terms:

Phase locked loop, Frequency synthesizer, Self-Healing prescaler, VCO, Leakage current, Multimodulus prescaler.

I.INTRODUCTION:

Complementary-metal-oxide-semiconductor(CMOS) [1] is a technology for constructing integrated circuits. CMOS technology is used for analog [1] highly integrated transceivers for many types of communications. Two important characteristics of CMOS devices are high noise immunity and low static power consumption.

A phase locked loop [4] is a control system that generates an output signal whose phase is related to the phase of an input signal. PLL is a feedback system that combines a voltage controlled oscillator (VCO) [4] and a phase comparator so connected that the oscillator maintains a constant phase angle relative to a reference signal. PLLs are used to generate a stable output high frequency signals from a fixed low frequency signal. When a CMOS technology approaches to a nanometer scale the non-idealities such as variability and leakage current, may significantly affect the circuit performances. The process variability leads to the large variations to degrade the device matching and performances. It may result in a few dies on a wafer to meet the target performance specifications.

The undesired leakage currents also degrade the accuracy and resolution of the circuits. A phase locked loop (PLL) is widely employed in wire-line and wireless communication systems. The poor device matching and leakage current [5], [7] vary the common-mode voltage of a ring based voltage-controlled oscillator (VCO) over wide frequency range. It may limit the oscillation frequency range of a VCO [6] and causes a VCO not o oscillate in a worst case. To realize a wide range PLL, the divider following a VCO should be operate between the highest and lowest frequencies.There are many applications that require the synthesis of frequencies above 3GHz. However, this range is generally beyond the maximum frequency range that PLL devices can directly accept. By using an external prescaler [3], the range of PLL can be extended. When a PLL works at a higher frequency which the static circuits cannot operate, dynamic circuits are needed.

II.EXISTING CIRCUIT DESCRIPTION:

A.Self-Healing Divide-by-4/5 Dual-Modulus Prescaler:

Fig. 2(a) shows a conventional divide-by-4/5 dual-modulus prescaler using TSPC DFFs [3]. The undesired leakage current [2] may charge or discharge to alter the states of the nodes A, B, AND Qbar in this TSPCDFF.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

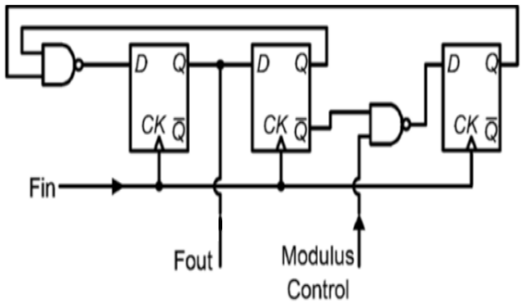


Fig.1. Conventional self-healing divide by 4/5 dual modulus prescaler.

The DFF is designed by using a method True Single Phase Clocking (TSPC) approach. TSPC is a dynamic CMOS approach to designing low power circuits. A TSPC prescaler must work over a wide frequency range to cover the process and temperature variations. For a TSPC prescaler, the undesired leakage currents may limit its frequency range or alter the original states of the floating nodes to have a malfunction.

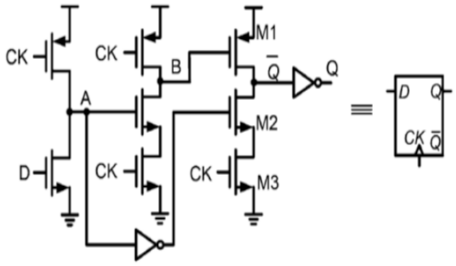


Fig. 1(a) internal circuit of TSPC DFF.

To detect and heal the above issues occurred at the nodes A and Qbar, the self-healing circuit is used. This self-healing circuit consists of a detector and three compensators. By using a self-healing circuit, the timing diagrams of a TPSC DFF with and without a malfunction are shown below.

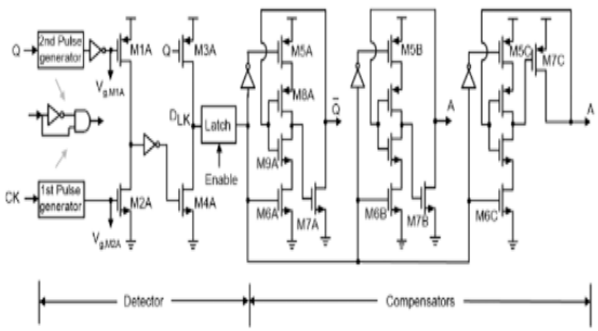


Fig. 1(b) self-healing circuit for prescaler.

B.Self-Healing VCO:

A self-healing VCO is realized by four gain stages, a bottom-level detector, and a current compensator. Fig. 2 shows a bottom-level detector, a current compensator, and a gain stage. The cross-coupled pail, M5 and M6, enhances the output swing of this VCO. The output common-mode voltage and the output swing of the VCO are altered by the leakage currents, the total tail currents and the resistance of M3 and M4The bottom-level detector is shown in Fig. 2 and it detects the bottom-level of the VCO's output swing. A self-biased buffer enlarges the output of a VCO into a rail-to-rail swing. So, the output, Vbuf, of this self-biased buffer and Vout+ have the same polarity. When Vout+ goes high and Vbuf is high, the NOR gate will enable MB1 and disable MB2, respectively. The current of the transistor MB1 will charge the capacitor, CH, to increase VBL. The capacitor CH is used to track the bottom level of the VCO swing. The current compensators enables he tail currents when the bottom level is higher than the target swing voltage.

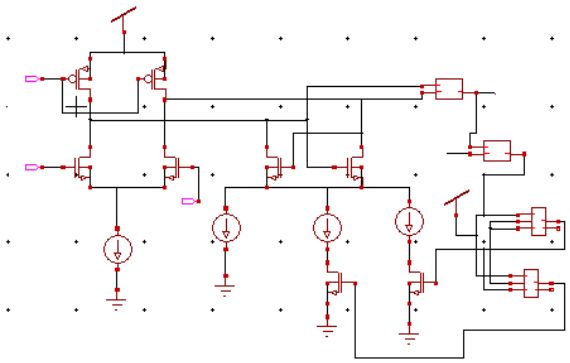


Fig. 2 gain stage of Voltage Controlled Oscillator.

For the current compensator a reference voltage Vsw represents the target bottom level of the VCO's swing and it is compared with Vbl, by a comparator. When the VCO's bottom level is smaller than the target one or the output common mode voltage of this VCO is high enough, Vbl is larger than Vsw. Then, the output of the comparator goes high and enables Q1. The current compensator enables the auxiliary tail current I1 to lower the output common-mode voltage. Then, it reduces the VCO's bottom level to be lower than Vsw. If the above case is not true, Q2 will be enabled and turn on the auxiliary tail current I2. It further lowers the VCO's bottom level.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

C.Phase locked loop:

The PLL [8] is composed of a phase-frequency detector (PFD), a digital-controlled CP, a lock detector (LD), a time-to-digital converter (TDC) [8] with a 4-bit encoder, a self-healing VCO, a programmable divider, and a second-order passive loop filter. The programmable divider is composed of a 5-bit counter, a 3-bit swallow counter, a modulus control, and a self-healing divide-by-4/5 prescaler. The division ratio is from 4 to 131.

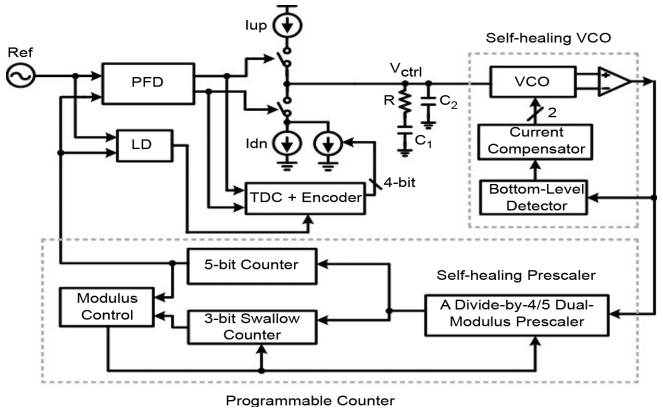


Fig. 3 The existing PLL.

D.Counter:

The programmable counter consists of a self-healing divide by 4/5 prescaler with fractional counter those are 5-bit counter and 3-bit swallow counter.

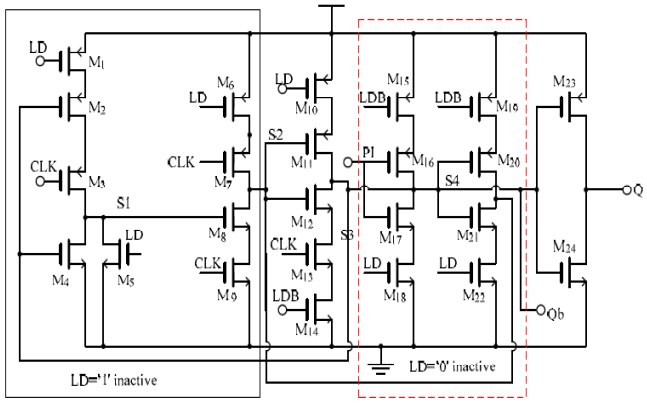


Fig. 4 Basic building block of programmable counter.

The basic cell is a CMOS circuit having LD, LDbar, CLK and PI signals as shown in fig. 4. These counters are used to get the division ratios from 4 to 131. The 5-bit p-counter consists of 5 basic cells and swallow counter having three basic cells.

Table 1 Operation of the basic cell:

Load(LD)	Programmable input(PI)	Output(Q)
0	0	CLK/2
0	1	CLK/2
1	0	0
1	1	1

When LD signal is low then the cell operates in divide by 2 mode otherwise output follows the programmable input.Once the programmable input (PI) of the each reloadable FF is loaded with a value and LD signal goes low, the P-counter begins to count down. Under this condition, theright hand side of the reloadable DFF as highlighted in Fig.4.4 is deactivated and transistor M5 is turned-off such that the FF acts as a divide-by-2 circuit where node S3 is complimentary of the divide-by-2 output. The FF remains in the divide-by-2 mode until the counter reaches the state "0000010". When LD='1', the first two stages of the reloadable FF is deactivated and node S1 always remains at logic '0' since the transistor M5 is turned-on. Since node S1 is at logic '0', node S2 should be at logic '1'.

However, node S2 is overridden by the complimentary value of node S4. Under this condition (LD='1'), if the programmable input PI='0', nodes S4 and S2 switch to logic '1' and '0' respectively. The value at node S2 is latched to the output node Q on the next rising edge of the clock. Similarly, if PI='1', the output Q switches to '1' on the clock rising edge.However when LD='0', the bit-cell acts as a divide-by-2 circuit irrespective of the PI value. The VCO operating range of the existing PLL is 60 to 1489MHz.s and the ref. frequency of this VCO is 15MHz.

We can increase the operating frequencies of this VCO and then we get high frequencies by using prescaler. In order to get very wide ranges or the frequencies used for IEEE applications we go for multimodulus prescalers. The proposed multimodulus prescaler having division ratios of divide by 32/33/47/48. In this I used divide by 2/3 dual-modulus prescaler as a basic block.

III.PROPOSED MULTIMODULUS PRESCALER:

The block diagram of proposed PLL

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

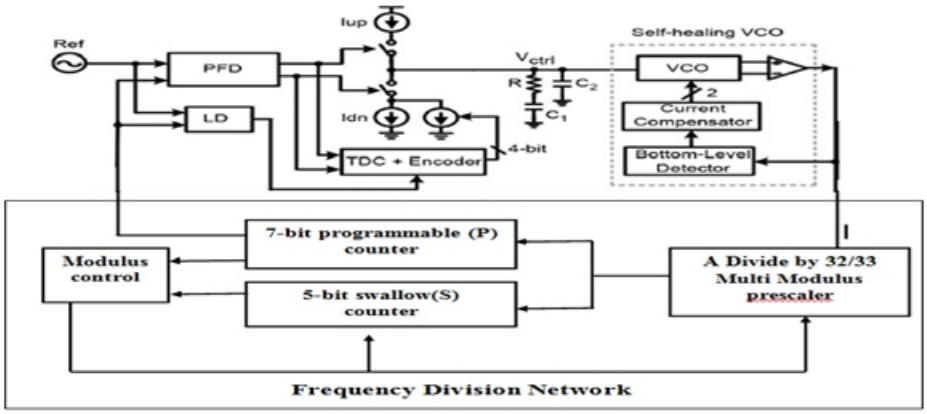
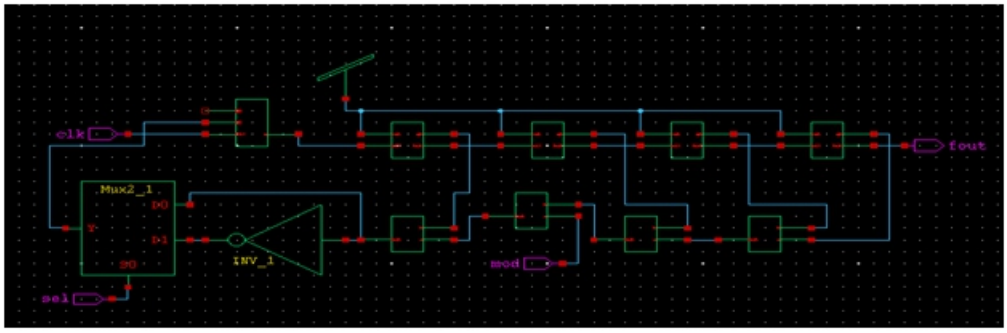


Fig5. Proposed PLL

The schematic diagram of Prescaler is shown in below fig.



IV.EXPERIMENTAL RESULTS:

When this PLL locks, the LD (Lock Detector) is enabled to turn on the TDC and an encoder. A 4-bit TDC digitizes this static phase error to reflect the amount of the cur-rent mismatching. Then, the digital code of this TDC is used to calibrate the charge pump. The CP calibration can be finished quickly due to this digital calibration.Once the calibration is completed, the digital code is fixed and the TDC is power-downed to save a power.

The input and output waveforms of multi modulus prescaler is shown below.

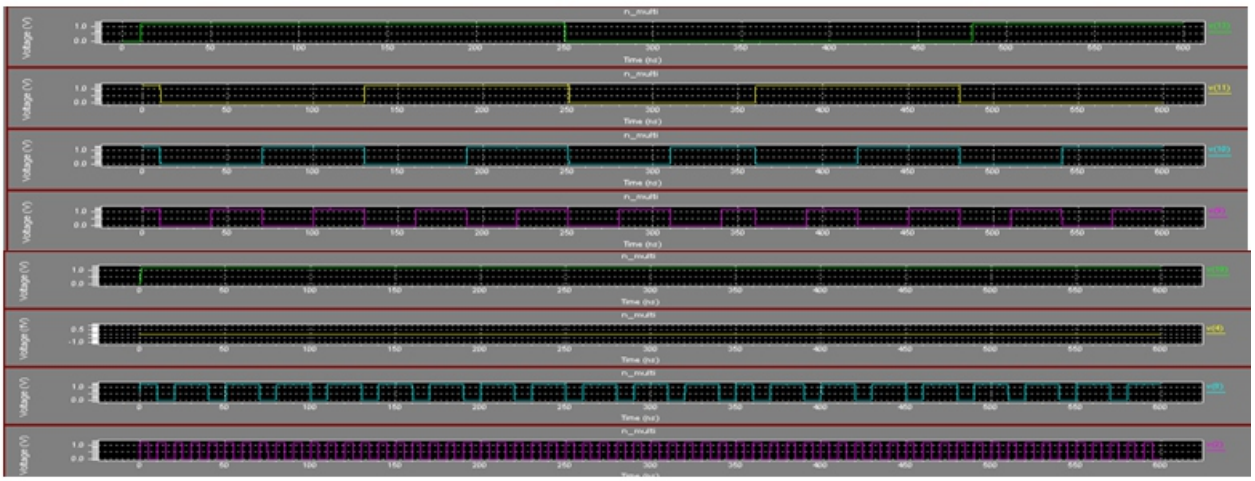


Fig.6. Waveforms of multi modulus prescaler.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

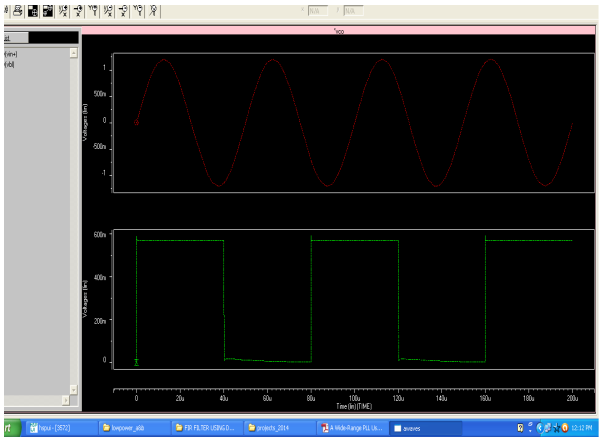


Fig. 7. The simulation result of VCO gain stage.

The VCO gain stage converts the analog signal to digital. Which is act as a CLK to the prescaler.

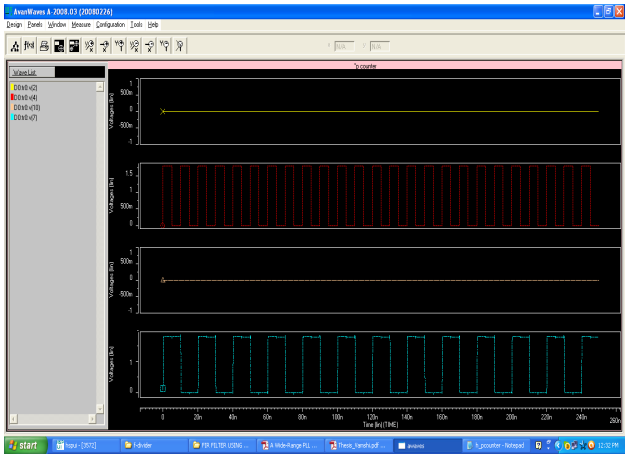


Fig.8.Simulation result of counter basic cell when LD=0 and PI=0.

The non-idealities such as leakage current [2] and process variations can alter the VCO [6] gain in order to rectify those problems current compensators are used.As shown in Fig. 10 we know that when the LD=0 and PI is either 0 or 1 the output of the counter will be CLk divided by 2. Divided by 2 operation takes place here. These types of operations takes place in both programmable and swallow counters.In the proposed PLL [9] we have fully programmable multimodulus prescaler as shown in Fig. 5. In this we have a basic building block as TSPC divide by 2/3 dual modulus prescaler [10] as shown in Fig. 6. The simulation result of this divide by 2/3 prescaler is shown in Fig. 11. The average power consumed for this divide by 2/3 dual modulus prescaler [10] is 3.6µW when we simulate this in CMOS 45nm technology.

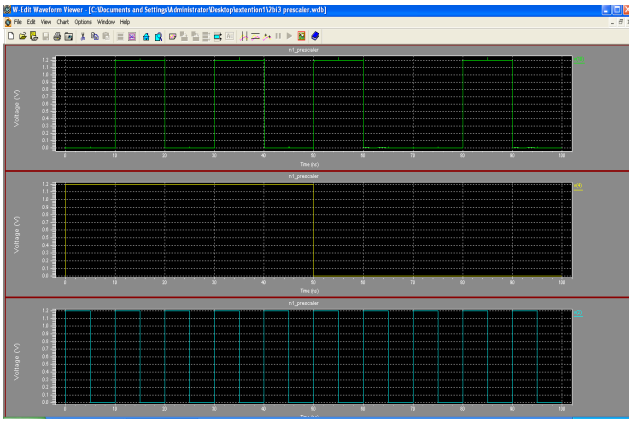


Fig.9. Simulation result of divide by 2/3 TSPC dual modulus prescaler.

Fig. 12 shows the simulation result of the proposed fully programmable multimodulus prescaler. This multimodulus prescaler is used to extend the frequencies up to 6 GHz. Here the proposed multimodulus prescaler [11] is a CMOS fully programmable 1 MHz resolution divider for Zigbee and IEEE 802.15.4 applications is implemented based on pulse swallow topology.

The range of P values among 74 to 77 then the P-counter can produce 2.4 GHz frequency which is used for Zigbee application. In this the multimodulus prescaler acts as divide by 32/33 dual modulus prescaler [11].For IEEE 802.15.4 application the multimodulus prescaler can be operating in divide by 47/48 dual modulus prescaler [9], [10].

Here also the programmable counter will have 1MHz resolution signal can be applied to P-counter. P values ranging from 105 to 122. It can generate frequency ranges from 5.1 GHz to 5.82 GHz.The fully programmed multimodulus prescaler [9] can consume an average power of 18.09µW when we simulate this in CMOS 45nm technology. The simulation result is shown in Fig 12.

We can extend the divide ratios by altering the P-values and S-values. Thus we can achieve more high frequencies from this low frequency PLL.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

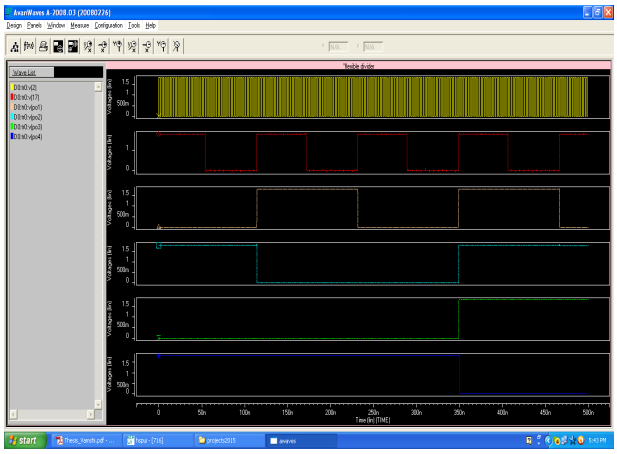


Fig. 10. Simulation result of fully programmed multi-modulus prescaler.

V.CONCLUSION:

A wide-range PLL is designed in a 45-nm CMOS process. The Multi modulus 32/33 prescaler has maximum operating frequency of 6.2 GHz, the values of P- and S-counters can actually be programmed to divide over the whole range of frequencies from 1 to 6.2 GHz and the multiband flexible divider also uses an improved loadable bit-cell for Swallow S-counter and consumes a power of 0.96 and 2.2 mw in 2.3- and 5-GHz bands, respectively.

VI.ACKNOWLEDGMENT:

I am greatly indebted to my advisor Mrs B.V. Krishnaveni for her valuable guidance, consistent encouragement and emphasis on the quality of the research contribution. Finally, and most importantly i would like to thank my family and friends for their support and unconditional love i have enjoyed throughout my life.

VII.REFERENCES:

[1] L. L. Lewyn, T. Ytterdal, C. Wulff, and K. Martin, "Analog circuit design in nanoscale CMOS technologies," Proc. IEEE, vol. 18, no. 11, pp. 1687–1714, Oct. 2009.

[2] R. Holzer, "A 1 V CMOS PLL designed in high-leakage CMOS process operating at 10–700 MHz," in Proc. IEEE Int. Solid-State Circuits Conf., 2002, pp. 272–273.

[3] C. Y. Yang, G. K. Dehng, J. M. Hsu, and S. I. Liu, "New dynamic flip-flops for high-speed dual modulus prescaler," IEEE J. Solid-State Circuits, vol. 33, no. 10, pp. 1568–1571, Oct. 1998.

[4] C. N. Chuang and S. I. Liu, "A 1 V phase locked loop with leakage compensation in 0.13 m CMOS technology," IEICE Trans. Electron., vol. E89-C, pp. 295–299, Mar. 2006.

[5] C. C. Hung and S. I. Liu, "A leakage-suppression technique for phase locked systems in 65 nm CMOS technology," in Proc. IEEE Int. Solid- State Circuits Conf., 2009, pp. 400–401.

[6] N. Fong, J. Plouchart, N. Zamdmer, D. Liu, L. Wagner, C.Plett, and N. Tarr, "Design of wide-band CMOS VCO for multiband wireless LAN applications", IEEE J. Solid-State Circuits (JSSC), vol. 38, no.8, pp. 1333-1342, Aug. 2003.

[7] P. Andreani, "A low phase noise, low phase error 1.8-GHz quadrature CMOS VCO", Proc. Of 2002 IEEE ISSCC, pp. 290-291, Feb. 2006.

[8] Won-Hyo Lee, Jun-Dong Cho and Sung-Dae Lee, "A high speed and low power phase frequency detector and charge pump", in Proc. IEEE Biomedical Circuits & Systems Conf., pp. 187-190, Nov 2007.

[9] Xinhua He, "Low Phase Noise CMOS PLL Frequency synthesizer Analysis and Design", Ph.D. Thesis, Graduate Studies of the University of Maryland, 2007.

[10] V. Manassewitsch, Frequency Synthesizers, Theory and Design, Wiley, 1987. Ultra Low Power CMOS Phase-Locked Loop Synthesizers.

[11] M.Vamshi Krishna, M.A. Do, K.S. Yeo, C.C. Boon and W.M. Lim, "Design and Analysis of Ultra Low Power True Single Phase Clock CMOS 2/3 Prescaler", IEEE Trans. Circuits & Systems-I: Reg. Papers, vol. 57, no.1, pp. 72-82, Jan. 2010.