ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

3-Weight Pattern Generation for 0, 1 And 0.5 Weights Based on Accumulator

Machireddy Sukumar Reddy
Dept of VLSI & ESD,
SKR College of Engineering & Technology,
Konduru Satram [V], Manubolu [M], S.P.S.R.
Nellore [Dt], Andhra Pradesh, India.

Mr. Goni Mahendra
Associate Professor
Dept of VLSI Systen Design,
SKR College of Engineering & Technology,
Konduru Satram [V], Manubolu [M], S.P.S.R.
Nellore [Dt], Andhra Pradesh, India.

Abtract:

Weighted pseudorandom built-in self test (BIST) schemes have been utilized in order to drive down the number of vectors to achieve complete fault coverage in BIST applications. Weighted sets comprising three weights, namely 0, 1, and 0.5 have been successfully utilized so far for test pattern generation, since they result in both low testing time and low consumed power. In this paper an accumulator-based 3-weight test pattern generation scheme is presented; the proposed scheme generates set of patterns with weights 0, 0.5, and 1. Since accumulators are commonly found in current VLSI chips, this scheme can be efficiently utilized to drive down the hardware of BIST pattern generation, as well. Comparisons with previously presented schemes indicate that the proposed scheme compares favourably with respect to the required hardware.

Index Terms:

Built-in self test (BIST), test per clock, VLSI testing, weighted test pattern generation.

1.INTRODUCTION:

This chapter discusses about the basic idea about Built-In Self Test(BIST) and its applications and limitations. Also discusses about the literature survey which focuses on the evolution and developments of BIST mechanisms. It also discusses about the objective of the implemented BIST mechanism and software tools used to implement the design.

1.1 Built In Self Test:

With the ever increasing need for system integration, the trend today is to include in the same VLSI device a large number of functional blocks, and to package such devices, often, in Multi-Chip Modules (MCMs) that comprise complex systems. This leads to difficult testing problems in the manufacturing process and in the field . An attractive approach to solve these problems is to use a multi-level integrated Built-In Self-Test (BIST) strategy. This strategy assumes that BIST is used at each level of manufacturing test, and it is reused at all consecutive levels, i.e. device, MCM, board, system. Boundary-Scan standard to realize self testing at different levels. This strategy can only be realized if the appropriate BIST features are included in devices.Linear feedback shift registers (LFSRs) are commonly used as test pattern generators (TPGs) in low overhead built-in self-test (BIST) schemes. This is due to the fact that an LFSR can be built with little area overhead. A

ttainment of high fault coverage with sequences of practical lengths has traditionally been the main objective of BIST techniques. Even though this still remains the main objective, reducing heat dissipated during test application is becoming another important objective. The correlation between consecutive random patterns generated by an LFSR is low; this is a well-known property of LFSR-generated patterns. On the other hand, a significant correlation exists between consecutive vectors applied to the inputs of a circuit during its normal operation. Hence, switching activity in a circuit can be significantly higher during self-test than that during its normal operation. To reduce the test complexity and reduce the test cost the BIST techniques are widely used in chip design In BIST,

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

the linear feedback shift register (LFSR) is commonly used as test pattern generator (TPG). However, an LFSR TPG may generate unacceptability long test sequences to attain high fault coverage (FC) and these random patterns may cause as many nodes switching as possible during testing. Hence, Power and energy consumption of digital systems become much higher in test mode than that in its normal mode of operation. The increased power consumption mill limit the system performances, and the extra power consumption due to test application can also raise severe hazards to circuit reliability. In this work, a New BIST structure for low power testing is implemented. The inputs of CUT are divided into two groups. The inputs which transition will cause more transitions at internal nodes than those at other inputs are called 'heavy inputs' .After calculating to select the CUT's heavy inputs, a modified LFSR structure is presented. Using the implemented structure, experiments to compare the power dissipation in the test are done. Built-in self-test (BIST) involves performing test pattern generation and output response analysis using on-chip circuitry. The most economical BIST techniques are based on pseudorandom pattern testing. There are two well-known problems with pseudo-random BIST: low fault coverage and high power dissipation. Low fault coverage arises due to the presence of random pattern resistant (R.P.R.)

faults, which have low detection probabilities. Solutions to this problem involve either modifying the circuit-under-test (CUT) by inserting test points to increase the detection probabilities, or by modifying the test pattern generator so that it generates patterns that detect the R.P.R. faults.The problem of high power dissipation comes from the fact that pseudo-random patterns cause much greater switching activity in the CUT than what occurs during normal functional operation. This can result in overheating, as the chip package may only be capable of handling the power dissipation that occurs during functional operation. Moreover, for portable electronics where BIST is used out in the field, it is desirable that the BIST use a minimal amount of energy to preserve battery life. The problem of low fault coverage for pseudo-random BIST has been studied for a long time and quite a number of solutions have been implemented. One of the most attractive involves adding weight logic to bias the pseudo-random patterns towards those that detect the R.P.R. faults. A number of weight selection algorithms have been implemented for finding a minimal number of weight sets to achieve a desired fault coverage.

The paper [2] exploits a advancement of reference [1] which further decreases the power consumption and remains random pattern resistant faults undetected. A simple method is employed in paper [3] to detect random pattern resistant faults, which employs weights on the pseudo random sequence generated by LFSR. The weights vary continuously from 0 to 1, to improve fault coverage. Reference[4] represents another method which yields same performance of [3] by changing the weights at discrete levels of '0','0.5'and '1' instead of changing the weights continuously. The paper[6] exploits a new method combining principles of [4] and [5] in which pseudo random sequences are generated to detect easy to detect faults during phase I. Patterns generated during phase II are used to detect the faults that are undetected by pseudo random sequence. This suffers from area over head, considerably less power dissipation and improved fault coverage. The new approach similar to [6] is carried out here, which further reduces power consumption by employing Bit-Swapping LFSR [2].The pseudo random patterns generated by the Bit Swapping LFSR are used to detect easy to detect faults and employs accumulator principle discussed in reference [4] is to detect random pattern resistant faults, which improves the fault coverage. This approach gives a optimum performance by considering area overhead, power consumption and improved fault coverage. The paper[3] reveals the standard benchmark circuits which are utilized here as circuit under test(CUT's).The faults has been injected in this CUT's and those faults will be detected with the principle approach discussed in [6] [4][5].

1.2 Objective:

The main objective of this thesis is to design and implementation of a Built In Self Test test pattern generator. Which is a combination of LT-RTPG and Accumulator Based 3-weight Pattern Generator.LT-RTPG is used to detect easy-to-detect faults and Accumulator Based 3-weight Pattern Generator is used to detect random pattern resistant faults? The main motto of this work is

1. To reduced power consumption.
2. To improve fault coverage.

1.3 Methodology:

This work proposes a new BIST TPG for Low power dissipation and High fault coverage. This BIST TPG comprised of two TPGs: 1.Low Transition-RTPG 2.Accumulator Based 3-Weight PG.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Low Transition-RTPG is used to detect easy-to- detect faults and for low power consumption and Accumulator Based 3-weight PG is used for high fault coverage. Here Modelsim is used for logical verification, and further synthesizing it on Xilinx-XST tool.This chapter discusses about the architecture of existing BIST mechanism, which is a combination of two test pattern generators namely Low transition random test pattern generator and 3-weighted BIST. It also discuss about the ISCAS 89'and benchmark circuits, such as S27 circuits and their functionality in which faults are injected and detected by using existing techniques. It also concentrates on the drawbacks of the existing system.

2. EXISTING MEATHODOLOGY:

2.2 Existing Test Pattern Generator:

The existing BIST is comprised of two TPGs: Low transition random test pattern generator (LT-RTPG) and a 3-weighted random BIST. The multiplexer, which drives the input of scan chain, selects a test pattern source between the LT-RTPG and the 3-weight WRBIST. In the first test session, test patterns generated by the LT-RTPG are selected and scanned into the scan chain to detect easy-to-detect faults.

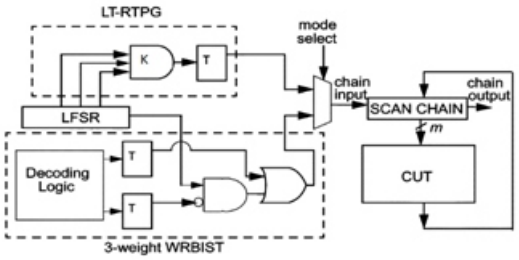


Fig2.1: Block Diagram of Existing System.

In the second session, test patterns that are generated by the 3-weight WRBIST are selected to detect the faults that remain undetected after the first session. Considering the fact that an LT-RTPG can be implemented with very little hardware overhead (only one T flip-flop and one AND gate in addition to an LFSR), overall hardware overhead to implement the TPG is determined by hardware overhead for the decoding logic of the 3-weight WRBIST.

2.3 Types of BIST TPG's:

Existing System comprised of two Test Pattern Generators, namely LT-RTPG[4] using basic Linear Feedback Shift Register (LFSR) which is used to detect easy to detect faults and 3-Weighted Random Built-In-Self Test[5] is used to detect random pattern resistant faults(RPRF).

2.3.1 3-Weighted Random Built-In-Self Test:

In 3-Weighted Random Built-In-Self Test, the sequential CUT has 'm' primary and state inputs, and employs full-scan. Even though the implemented BIST TPG is applicable to scan designs with multiple scan chains, The all primary and state inputs are driven by a single scan chain unless stated otherwise (application to multiple scan chains is discussed separately in Section V) only for clarity and convenience of illustration. A test cube is a test pattern that has unspecified inputs. The detection probability of a fault is defined as the probability that a randomly generated test pattern detects the fault [6]. In the 3-weight WRBIST[5] scheme, fault coverage for a random pattern resistant circuit is enhanced by improving detection probabilities of RPRFs, the detection probability of an RPRF is improved by fixing some inputs of the CUT to the values specified in a deterministic test cube for the RPRF. A generator or weight set is a vector that represents weights that are assigned to inputs of the circuit during 3-weight WRBIST. Inputs that are assigned weight 1 (0) are fixed to 1 (0) and inputs that are assigned weight 0.5 are driven by outputs of the pseudorandom pattern generator, such as an LFSR and a CA. A generator is calculated from a set of deterministic test cubes for RPRFs[5].Pseudo-random pattern sequences generated by an LFSR and a CA are modified (fixed) by controlling the AND and OR gates with overriding signals S0 and S1; fixing a random value to a '0' is achieved by setting 'S0' to a '1' and 'S1' to a' 0' and fixing a random value to a '1' is achieved by setting 'S1' to a '1' Overriding signals 'S0' and 'S1' are driven by the outputs of T flip-flops,TF0 and TF1 The inputs of TFO and TF1 are in turn driven by the outputs of the decoding logic 'D0' and 'D1' respectively, which are generated by the outputs of the shift counter and the generator counter as inputs. Hence, hardware overhead for implementing a 3-weight WRBIST[3] is incurred only by the decoding logic and the fixing logic, which includes two toggle flip-flops, an AND and an OR gate. Since the fixing logic can be implemented with very little hardware, overall hardware overhead for implementing the serial fixing 3-weight WRBIST is determined by hardware overhead for the decoding logic.

2.4 Circuits considered:

Testing sequential circuits has been one of the most challenging areas in digital circuits. Automating test generation for large sequential circuits without Design for Testability (DFT) logic has met with marginal success.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

By using above implemented system all ISCAS 89'benchmark circuits will be tested. ISCAS 89' benchmark circuits will consist of both sequential circuits and combinational circuits. Here three familiar circuits are selected for fault injection and detection.The circuit diagram of ISCAS 89' S-27 benchmark circuit and generalized sequential circuits are shown in Fig 4.6 and Fig 4.7 respectively. The position of fault injected in S-27 and sequential circuit are discussed under 4.5.1, 4.5.2 respectively.

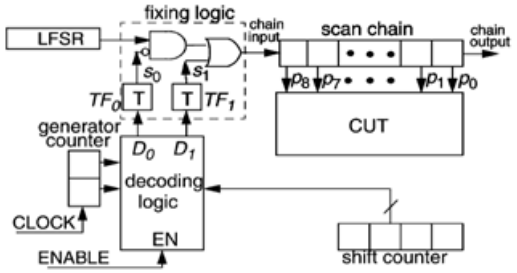


Fig 2.2: 3-Weight Weighted Random BIST

2.4 Circuits considered:

Testing sequential circuits has been one of the most challenging areas in digital circuits. Automating test generation for large sequential circuits without Design for Testability (DFT) logic has met with marginal success. By using above implemented system all ISCAS 89'benchmark circuits will be tested. ISCAS 89' benchmark circuits will consist of both sequential circuits and combinational circuits.

Here three familiar circuits are selected for fault injection and detection.The circuit diagram of ISCAS 89' S-27 benchmark circuit and generalized sequential circuits are shown in Fig 4.6 and Fig 4.7 respectively. The position of fault injected in S-27 and sequential circuit are discussed under 4.5.1, 4.5.2 respectively.

2.5 Drawbacks of Existing System:

Following are the major drawbacks of existing system

1. Consumes more power
2. It will detect limited amount of faults
3. Less operating speeds

To overcome above drawbacks a new BIST mechanism has been implemented .The
Implemented system is discussed in the next chapter.

2.6 Summary:

This chapter discussed about the architecture of existing BIST mechanism, which is a combination of two test pattern generators namely Low transition random test pattern generator and 3-weighted BIST. It also discuss about the ISCAS 89'and benchmark circuits, such as S27 circuits and their functionality in which faults are injected and detected by using existing techniques. It also concentrates on the drawbacks of the existing system.

3. IMPLEMENTED BUILT IN SELF TEST SYSTEM:

The implemented BIST is comprised of two TPGs: an LT-RTPG[4] and a Accumulator 3-weight pattern generator[2]. The multiplexer, which drives the input of scan chain, selects a test pattern source between the LT-RTPG and the Accumulator 3-weight pattern generator. In the first test session, test patterns generated by the LT-RTPG are selected and scanned into the scan chain to detect easy-to-detect faults. In the second session, test patterns that are generated by the accumulator 3-weight pattern generator are selected to detect the faults that remain undetected after the first session. Considering the fact that an LT-RTPG can be implemented with very little hardware overhead (only one T flip-flop and one AND gate in addition to an LFSR), overall hardware overhead to implement the TPG is determined by hardware overhead for the fixing logic of the accumulator 3-weight pattern generator. In the first test session, test patterns generated by the LT-RTPG are selected and scanned into the scan chain to detect easy-to-detect faults. In the second session, test patterns that are generated by the Accumulator cell 3-weight PG[2] are selected to detect the faults that remain undetected after the first session.

3.1 Accumulator based 3-weight pattern generator:

Pseudorandom built-in self test (BIST) generators have been widely utilized to test integrated circuits and systems. The arsenal of pseudorandom generators includes, among others, linear feedback shift registers (LFSRs), cellular automata, and accumulators driven by a constant value. For circuits with hard-to-detect faults, a large number of random patterns have to be generated before high fault coverage is achieved. Therefore, weighted pseudo-random techniques have been implemented where inputs

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

are biased by changing the probability of a "0" or a "1" on a given input from 0.5 (for pure pseudorandom tests) to some other value. Weighted random pattern generation methods relying on a single weight assignment usually fail to achieve complete fault coverage using a reasonable number of test patterns, although the weights are computed to be suitable for most faults, some faults may require long test sequences to be detected with these weight assignments if they do not match their activation and propagation requirements. Multiple weight assignments have been suggested for the case that different faults require different biases of the input combinations applied to the circuit, to ensure that a relatively small number of patterns can detect all faults.

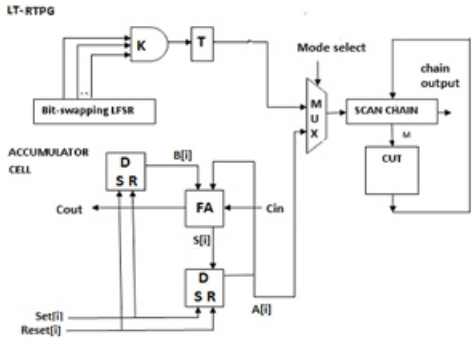


Fig3.1: Block Diagram of Implemented System

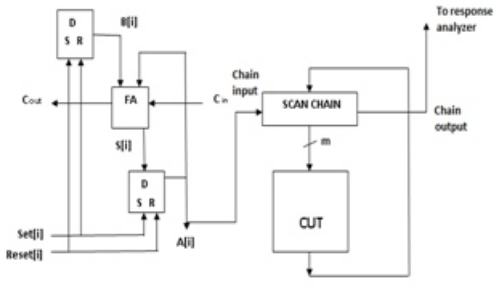


Fig 3.2: Accumulator cell with CUT:

Approaches to derive weight assignments for given deterministic tests are attractive since they have the potential to allow complete coverage with a significantly smaller number of test patterns. In order to minimize the hardware implementation cost, other schemes based on multiple weight assignments utilized weights 0, 1, and 0.5[3] [4]. This approach boils down to keeping some outputs of the generator steady (to either 0 or 1) and letting the remaining outputs change values (pseudo-) randomly (weight 0.5). approach, apart from reducing the hardware overhead has beneficial effect on the consumed power.

Current VLSI circuits, e.g., data path architectures, or digital signal processing chips commonly contain arithmetic modules [accumulators or arithmetic logic units (ALUs)]. This has fired the idea of arithmetic BIST (ABIST). The basic idea of ABIST is to utilize accumulators for built-in testing (compression of the CUT responses, or generation of test patterns) and has been shown to result in low hardware overhead and low impact on the circuit normal operating speed it was proved that the test vectors generated by an accumulator whose inputs are driven by a constant pattern can have acceptable pseudorandom characteristics, if the input pattern is properly selected. However, modules containing hard-to-detect faults still require extra test hardware either by inserting test points into the mission logic or by storing additional deterministic test patterns. In order to overcome this problem, an accumulator-based weighted pattern generation scheme was implemented. The scheme generates test patterns having one of three weights [4], namely 0, 1, and 0.5 therefore it can be utilized to drastically reduce the test application time in accumulator- based test pattern generation. However, the implemented scheme possesses three major drawbacks:

•It can be utilized only in the case that the adder of the accumulator is a ripple carry adder;
•It requires redesigning the accumulator; this modification, apart from being costly, requires redesign of the core of the data path, a practice that is generally discouraged in current BIST schemes; and
•It increases delay, since it affects the normal operating speed of the adder.

In this work, a novel scheme for accumulator-based 3-weight generation is presented. The implemented scheme copes with the inherent drawbacks of the scheme implemented. More precisely:
•It does not impose any requirements about the design of the adder (i.e., it can be implemented using any adder design);
•It does not require any modification of the adder, and hence,
•Does not affect the operating speed of the adder. I shall illustrate the idea of an accumulator-based 3-weight pattern Generation. I need some predefined test patterns schemes required to analyze the circuit .According to these schemes, a typical weight assignment procedure would involve separating the test set into two subsets, let, S1 and S2.
The weight assignments for these subsets is '-' denotes a weight assignment of 0.5, a "1" indicates that the input is constantly driven by the logic "1" value, and "0"

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

indicates that the input is driven by the logic "0" value. The above reasoning calls for a configuration of the accumulator, where the following conditions are met:

•An accumulator output can be constantly driven by "1" or "0" and

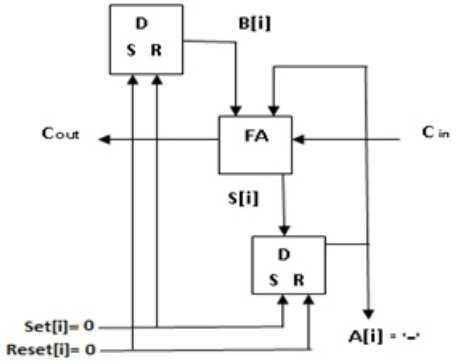
•An accumulator cell with its output constantly driven to "1" or "0" allows the carry input of the stage to transfer to its carry output unchanged. This latter condition is required in order to effectively generate pseudorandom patterns in the accumulator outputs whose weight assignment is "-".

Table 3.1: Test Set for S27 Benchmark circuit

Test vector	Input A[4:0]
T1	1011
T2	1111
T3	0100
T4	0110

3.4 Design Methodology of Accumulator Cell:\

The implementation of the weighted-pattern generation scheme is based on the full adder truth table, presented in Table 4.2. From Table 4.2 the lines #2, #3, #6, and #7 of the truth table, Cout = Cin. Therefore, in order to transfer the carry input to the carry output, it is enough to set A[I]=NOT(B[I]).. The implemented scheme is based on this observation. The implementation of the implemented weighted pattern generation scheme is based on the accumulator cell presented in Fig.3.2, which consists of a Full Adder (FA) cell and a D-type flip-flop with asynchronous set and reset inputs whose output is also driven to one of the full adder inputs. Without loss of generality, that the set and reset are active high signals. In the same figure the respective cell of the driving register B[i] is also shown. For this accumulator cell, one out of three configurations can be utilized, as shown in Fig. 3.3.



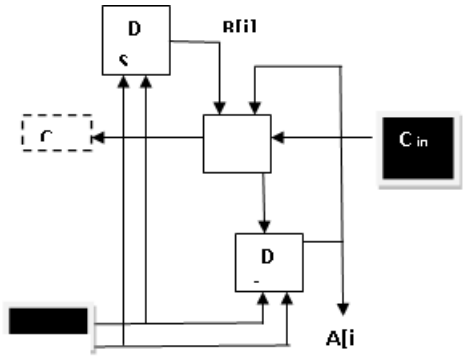


Fig 3.3: Accumulator cell

In Fig 3.4(a) the configuration that drives the CUT inputs When A[I]=1 is required. Set [I] = 1 and Reset [I] = 0 and hence A [I] = 1 and B [I] = 0.Then the output is equal to 1,and cin is transferred to cout

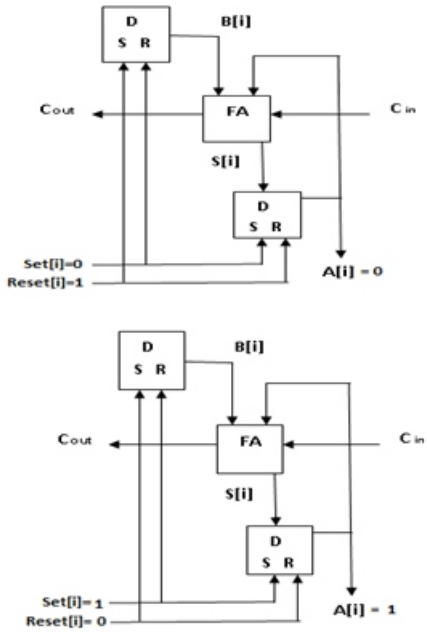


Fig 3.4 (a,b,c): Configurations of the accumulator cell of Fig 3.5

In Fig 3.4(b) the configuration that drives the CUT inputs When A[I]=0 is required. Set [I] = 0 and Reset [I] = 1 and hence A [I] = 0 and B [I] = 1.Then the output is equal to 0,and cin is transferred to cout.In Fig 3.4(c) the configuration that drives the CUT inputs When A[I]=" - " is required. Set [I] = 0 and Reset [I] = 0. The D input of the flip-flop of register B is driven by either 1 or 0, depending on the value that will be added to the accumulator inputs in order to generate satisfactorily random patterns to the inputs of the CUT.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

In Fig. 3.5, the general configuration of the implemented scheme is presented. The Logic module provides the Set[n-1:0] and Reset[n-1:0] signals that drive the S and R inputs of the Register A and Register B inputs. Note that the signals that drive the S inputs of the flip-flops of Register A, also drive the R inputs of the flip-flops of Register B and vice versa.

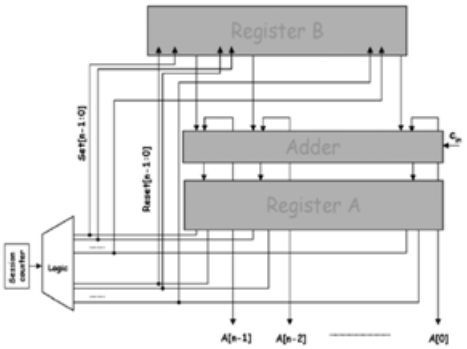


Fig 3.5: Accumulator 3-weight Pattern Generator.

3.5 Circuits considered:

Testing sequential circuits has been one of the most challenging areas in digital circuits. Automating test generation for large sequential circuits without Design for Testability (DFT) logic has met with marginal success. By using above implemented system all ISCAS 89' benchmark circuits will be tested. ISCAS 89' benchmark circuits will consist of both sequential circuits and combinational circuits Here three familiar circuits are selected for fault injection and detection.

3.5.1 S27 sequential circuit:

Here S27 circuit is selected, which belongs to ISCAS 89' benchmark circuit family and It is a purely sequential circuit with four inputs. The circuit has been tested by using Built In-Self Test. Initially faults are inserted into the circuit, in the above circuit faults are inserted at a2,a9,a4 and a10 locations.

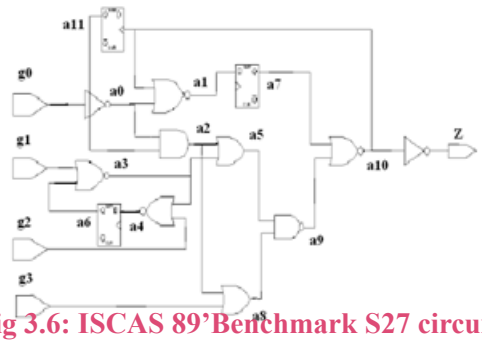


Fig 3.6: ISCAS 89'Benchmark S27 circuit

For each and every fault pseudorandom patterns are applied corresponding test vector will be taken for four faults four test vectors are taken. These vectors are divided into two sub groups for the reduction of transitions. As number of transitions are reduced the power consumption is reduced. The appropriate Set and Reset values has to be estimated from sub grouped test vectors these values will be applied to accumulator based 3-weight pattern generator if output value of faulty S27,and normal S27 circuits are different then fault has been covered.

3.5.2 Sequential circuit:

The below Fig 4.7 Sequential circuit, has been used for fault detection, faults has been injected at different positions a5,a7,a8 and detected by using LT-RTPG and Accumulator based 3-weight pattern generator.

3.6 Summary:

This chapter discussed about the architecture of implementing BIST mechanism, which is a combination of two test pattern generators namely Low transition random test pattern generator and Accumulator based 3-weight pattern generator. It also discuss about the ISCAS 89' benchmark circuits, such as S27 circuits and their functionality in which faults are injected and detected by using implemented techniques.

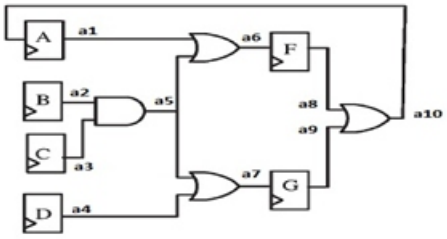


Fig 4.7: Sequential circuit

4. SIMULATION RESULTS:

This chapter discusses the simulation results which are executed with the help of modelsim, power results will be calculated with the help of xilinxs software tool. Also discusses about comparisons of the work , conclusion and future work.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

4.1 Simulated output of S27 circuit:

In the below simulation window, Fig 6.1 S27 circuit predefined test pattern output, The clock frequency is set to 10MHz.In order get random pattern resistant faults I need to have predefined test patterns of faulty S27 circuit. Normally 4 faults has been inserted into S27 circuit, The different test patterns generated by the LFSR are applied to S27 circuit then at each and every fault corresponding test vector is noted These patterns are the pre-defined test vectors of S27 circuit.

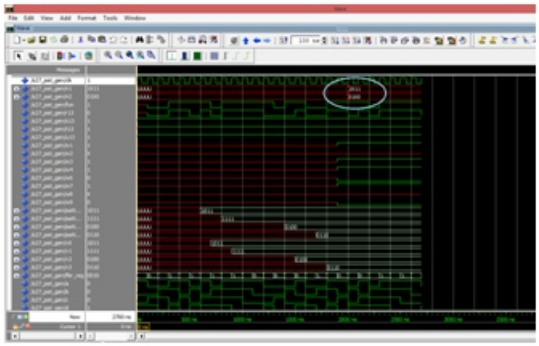


Fig 4.1: S27 circuit predefined test pattern output

Hence the 4 predefined test patterns from simulation outputs those are 1011,1111,0100,0110. These patterns are applied as set and reset values for Accumulator 3-weight pattern generator to detect faults present in the circuit.

4.2 Simulated output of Accumulator cell:

In the below simulation window, Fig 6.2 Accumulator 3-weight pattern generator output, The clock frequency is set to 10MHz.Predefined test patterns generated by the S27 circuit are applied as set and reset values then , fault signal become high hence fault has been covered. FUN is output of fault free circuit and FUN1 is an output of faulty circuit.

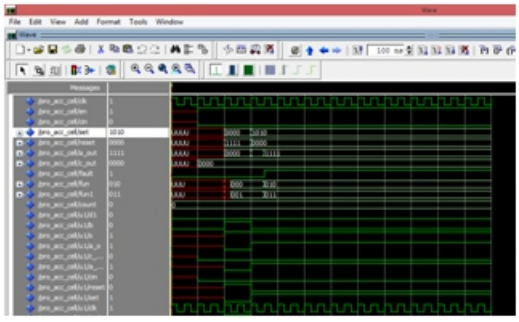


Fig 4.2: Accumulator 3-weight pattern generator output

Here FUN and FUN1 are different, hence the fault has been covered. The fault signal present in the simulation window becomes high when the predefined test patterns of S27 circuit are applied otherwise the fault signal becomes low.

4.2.1 Simulated output of Implemented system:

In the below simulation window, Fig 6.3 Complete Implemented system output,The clock frequency is set to 10MHz.Both easy to detect faults and random pattern resistant faults are detected .The fault signal is high ,the value of fault covered as 9. Hence the fault coverage is improved to 25%.

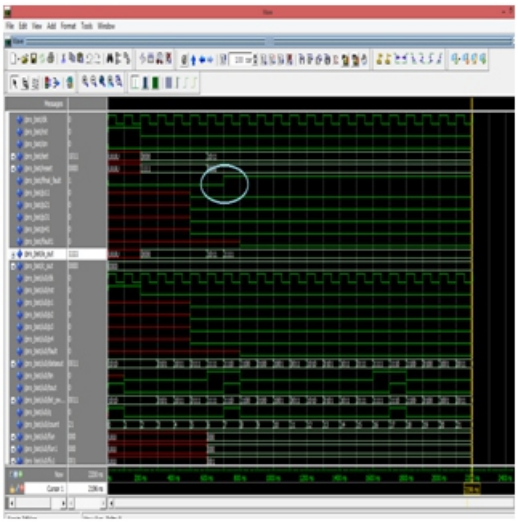


Fig 4.3: Implemented system output

This window consist of lfsr generated patterns which will be labeled as lfsr_reg. After applying S27 circuit predefined patterns 1000,1001 as set, reset values the final_ fault becomes high ,for 0000,1111 values final_fault signal is low. Hence the fault_final signal will be high only for the predefined test patterns of S27 circuit

4.3 Power Results

4.3.1 Power analysis report for 3-weight BIST:

The below Fig 4.4 Accumulator 3-Weight BIST Power Output using LFSR power output shows a power consumption of LFSR.As seen from figure the power consumed by LFSR is around 74mW which include total quiescent power of 25mW and total dynamic power around 50mW.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

The below Fig 4.5 3-Weight WRBIST Power Output using LFSR power output shows a power consumption of LFSR.As seen from figure the power consumed by LFSR is around 82mW which include total quiescent power of 25mW and total dynamic power around 58mW.

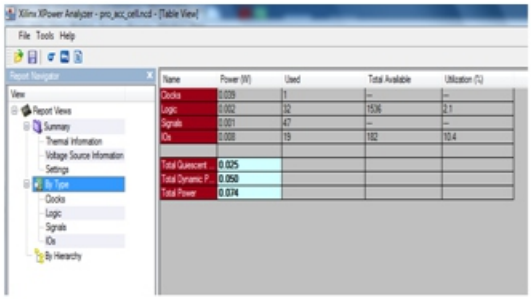


Fig 4.4: Accumulator Based 3-WT Pattern Generator Power Output

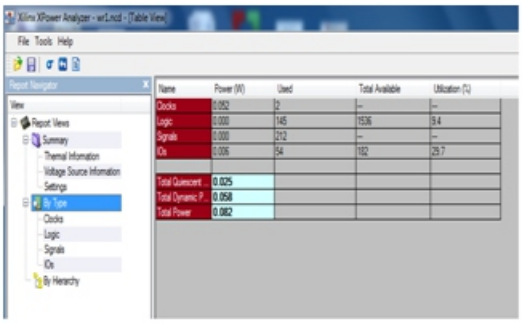


Fig4.5: 3-Weight WRBIST Power Output.

The above figures reveals the fact Accumulator Based 3-WT Pattern Generator Power Output consumes less power when compared with 3-Weight WRBIST Power Output.

4.3.2 Power analysis report for Implemented system

The below Fig 4.6 Implemented system Power Output using accumulator based 3-weight pattern generator. Which shows around 25mW.

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		25
Vccint 1.80V:	10	18
Vcco33 3.30V:	2	7
Clocks:	0	0
Inputs:	0	0
Logic:	0	0
Outputs:		
Vcco33	0	0
Signals:	0	0
Quiescent Vccint 1.80V:	10	18
Quiescent Vcco33 3.30V:	2	7

Fig 4.6: Implemented System Power Output

4.3.3 Thermal Summary:

The thermal summary of the implemented system is as shown in the following table (Fig 4.7)

Thermal summary:	
Estimated junction temperature:	26C
Ambient temp:	25C
Case temp:	26C
Theta J-A range:	32 - 33C/W

Fig4.7: Implemented System Thermal Summary

4.4 Synthesis Results

4.4.1 Gate count for implemented system

The below figure shows gate count report for implemented system, Total equivalent gate count for the design is 560.Additional JTAG gate count for IOBs is 432 gates.

CONCLUSION:

In the implemented thesis a low hardware overhead TPG for scan-based BIST that can reduce switching activity in CUTs during BIST and also achieve very high fault coverage with a reasonable length of test sequence. Unacceptably long test sequences are often required to attain high fault coverage with pseudorandom test patterns for circuits that have many random pattern resistant faults. The main objective of most recent BIST techniques has been the design of TPGs that achieve high fault coverage at acceptable test lengths for such circuits. While this objective still remains important, reducing heat dissipation during test application is also becoming an important objective. Since the correlation between consecutive patterns applied to a circuit during BIST is significantly lower, switching activity in the circuit can be significantly higher during BIST than that during its normal operation.

Excessive switching activity during test application can cause several problems. The designed TPG reduces the number of transitions that occur at scan inputs during scan shifting by scanning in the test patterns where neighboring bits are highly correlated. The implemented BIST is comprised of two TPGs: LT-RTPG and Accumulator 3-weight PG. Test sequences generated by the LT-RTPG detect easy-to-detect faults. Faults that escape LT-RTPG test sequences are detected by test patterns generated by the Accumulator 3-weight PG.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

The number of weight sets (generators) is minimized by guiding the ATPG with cost functions that reflect the number of conflicting inputs to be incurred by setting an input to a binary value. An algorithm to design the Accumulator 3-weight PG that requires minimal hardware overhead and whose patterns cause minimal number of transitions during scan shift cycles is presented. Hardware overhead for the designed TPG is further reduced by identifying compatible scan chains in multiple scan chain designs. Experimental results for ISCAS'89 benchmark circuits demonstrate that the implemented BIST can significantly reduce switching activity during BIST while achieving 100% fault coverage for all benchmark circuits. Larger reduction in switching activity is achieved for large circuits, which have long scan chains. The implemented BIST structure does not require modification of mission logic which can cause performance degradation. Experimental results for large industrial circuits demonstrate that the designed TPG can significantly improve fault coverage of LFSR generated test sequences with low hardware overhead.

FUTURE SCOPE:

Presently technology used towards the area occupation and improved speed which is very important in certain applications. Hopefully the present architecture may lead to the advanced technology in minimizing the area and increasing the speed.

BIBLIOGRAPHY:

[1] B. Koenemann, "LFSR-Coded Test Patterns for Scan Design", Proc. of European Test Conference, Munich, Germany, April 1991,pp. 237-242.

[2] Abdallatif S abu-issa, "Bit-Swapping LFSR and scan chain ordering," in Proc. 11th IEEE VTS Nov. 2010. P. H. Bardell, W. H. McAnney, and J. Savir, Built-In Test for VLSI: Pseudorandom Techniques. New York: Wiley, 2010.

[3] Irith Pomeranz,"3-Weight Pseudo-Random Test Generation Based on a Deterministic Test Set for Combinational and Sequential Circuit,"in proc IEEE vol,.12.no.7 july 2002.

[4] Antonis Paschalis, "Accumulator Based 3-Weight Pattern Generator," in IEEE VTS, Nov. 2010 S. Hellebrand, J. Rajski, S. Tarnick, S. Venkataraman, and B. Courtois, "Built-In test for circuits with scan based on reseeding of multiple-polynomial linear feedback shift registers," IEEE Trans. Comput., vol. 44, no. 2, pp. 223–233, Feb. 2009.

[5] S. Wang and S. K. Gupta, "LT-RTPG: A new test-per-scan BIST TPG for low heat dissipation," IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst., vol. 25, no. 8, pp. 1565–1574, Aug. 2006.

[6] Seongmoon Wang ,"A BIST TPG for Low Power Dissipation and High Fault Coverage", IEEE transactions on very large scale integration (vlsi) systems, vol. 15, no. 7, july 2007

[7]S. Wang, "Low hardware overhead scan based 3-weight weighted random BIST," in Proc. IEEE Int. Test Conf., 2001, pp. 868–877.

[8] M. Chatterjee and D. K. Pradhan, "A new pattern biasing technique for BIST," in Proc. LSITS,1995,pp.417–425.

[9]N. Tamarapalli and J. Rajski, "Constructive multiphase test point in-sertion for scan-based BIST," in Proc. IEEE Int. Test Conf., 1996, pp. 649–658.

[10] Y. Savaria, B. Lague, and B. Kaminska, "A pragmatic approach to the design of self-testing circuits," in Proc. IEEE Int. Test Conf., 1989, pp. 745–754.

[11]J. Hartmann and G. Kemnitz, "How to do weighted random testing for BIST," in Proc. IEEE Int. Conf. Comput.-Aided Design, 1993, pp. 568–571.

[12] J. Waicukauski, E. Lindbloom, E. Eichelberger, and O. Forlenza, "A method for generating weighted random test patterns," IEEE Trans. Comput., vol. 33, no. 2, pp. 149–161, Mar. 1989.

[13] H.-C. Tsai, K.-T. Cheng, C.-J. Lin, and S. Bhawmik, "Efficient test-point selection for scan-based BIST," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 6, no. 4, pp. 667–676, Dec. 1998.

[14] W. Li, C. Yu, S. M. Reddy, and I. Pomeranz, "A scan BIST generation method using a markov source and partial BIST bit-fixing," in Proc. IEEE-ACM Design Autom. Conf., 2003, pp. 554–559.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

[15]N. Z. Basturkmen, S. M. Reddy, and I. Pomeranz, "Pseudo random patterns using markov sources for scan BIST," in Proc. IEEE Int. Test Conf., 2002, pp. 1013–1021.

[16]Y. Zorian, "A distributed BIST control scheme for complex VLSI devices," in Proc. VLSI Testing Symp., 1993, pp. 4–9.

[17]S. W. Golomb, Shift Register Sequences. Laguna Hills, CA: Aegean Park, 1982.

[18] C.-Y. Tsui, M. Pedram, C.-A. Chen, and A. M. Despain, "Low power state assignment targeting two-and multi-level logic implementation," in Proc. IEEE Int. Conf. Comput.-Aided Des., 1994, pp. 82–87.

[19]P. Girard, L. Guiller, C. Landrault, and S. Pravossoudovitch, "A test vector inhibiting technique for low energy BIST design," in Proc. VLSI Test. Symp., 1999, pp. 407–412.

[20]V. Dabholkar, S. Chakravarty, I. Pomeranz, and S. Reddy, "Techniques for minimizing power dissipation in scan and combinational circuits during test application," IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst., vol. 17, no. 12, pp. 1325–1333, Dec. 1998.

Author's Details:

1.Machireddy Sukumar Reddy Was Born In Manubolu [M], S.P.S.R.Nellore [Dt], Andhra Pradesh, India. He Received The B.Tech Degree In Electronics And Communication Engineering From Jnt University, Anantapur In 2013 And Pursuing M.Tech Degree In Vlsi & Esd From Jnt University, Anantapur. He Completed His B.Tech Degree In Priyadarshini Institute Of Technology, Kanuparthipadu [V], Nellore [T], [M], S.P.S.R.Nellore [Dt], Andhra Pradesh, India, And M.Tech Degree In Skr College Of Engineering & Technology, Konduru Satram [V], Manubolu [M], S.P.S.R.Nellore [Dt], Andhra Pradesh, India. He Can Be Reachable At Sukumarreddy1991@Gmail.Com.

2. Mr. Goni Mahendra Was Born In Andhra Pradesh, India. He Received The B.Tech Degree In Elecronics And Communication Engineering And M.Tech Degree In Vlsi System Design From P.B.R.Visvodaya Institute Of Technology & Science, Kavali - 524201, S.P.S.R.Nellore [Dt], Andhrapradesh From Jnt University, Anantapur. He Had Working As An Associate Professor In Dept. Of Electronics And Communication Engineering And Vlsi System Design From Skr College Of Engineering & Technology, Konduru Satram [V], Manubolu [M], S.P.S.R Nellore [Dt], Andhra Pradesh, India. He Can Be Reachable At Mahendra.Goni @Gmail.Com.